19-3444; Rev 0; 10/04

MAXIM

+5V Multiprotocol, 3Tx/3Rx, Software-Selectable Clock/Data Transceivers

General Description

The MXL1543B is a three-driver/three-receiver multiprotocol transceiver that operates from a +5V single supply. The MXL1543B, along with the MXL1544/MAX3175 and the MXL1344A, form a complete software-selectable data terminal equipment (DTE) or data communication equipment (DCE) interface port that supports the V.28 (RS-232), V.10/V.11 (RS-449/V.36, EIA-530, EIA-530A, X.21), and V.35 protocols. The MXL1543B transceivers carry the high-speed clock and data signals while the MXL1544/MAX3175 carry the control signals. The MXL1543B can be terminated by the MXL1344A software-selectable resistor termination network or by discrete termination networks.

An internal charge pump and a proprietary low-dropout transmitter output stage allow V.11- , V.28- , and V.35-compliant operation from a +5V single supply. A no-cable mode is entered when all mode pins (M0, M1, and M2) are pulled high or left unconnected. In no-cable mode, supply current decreases to 0.5µA and all transmitter and receiver outputs are disabled (high impedance). Short-circuit current limiting and thermal shutdown circuitry protect the drivers against excessive power dissipation.

Applications

Data Networking

CSU and DSU

Data Routers

PCI Cards

Telecommunications Equipment

Features

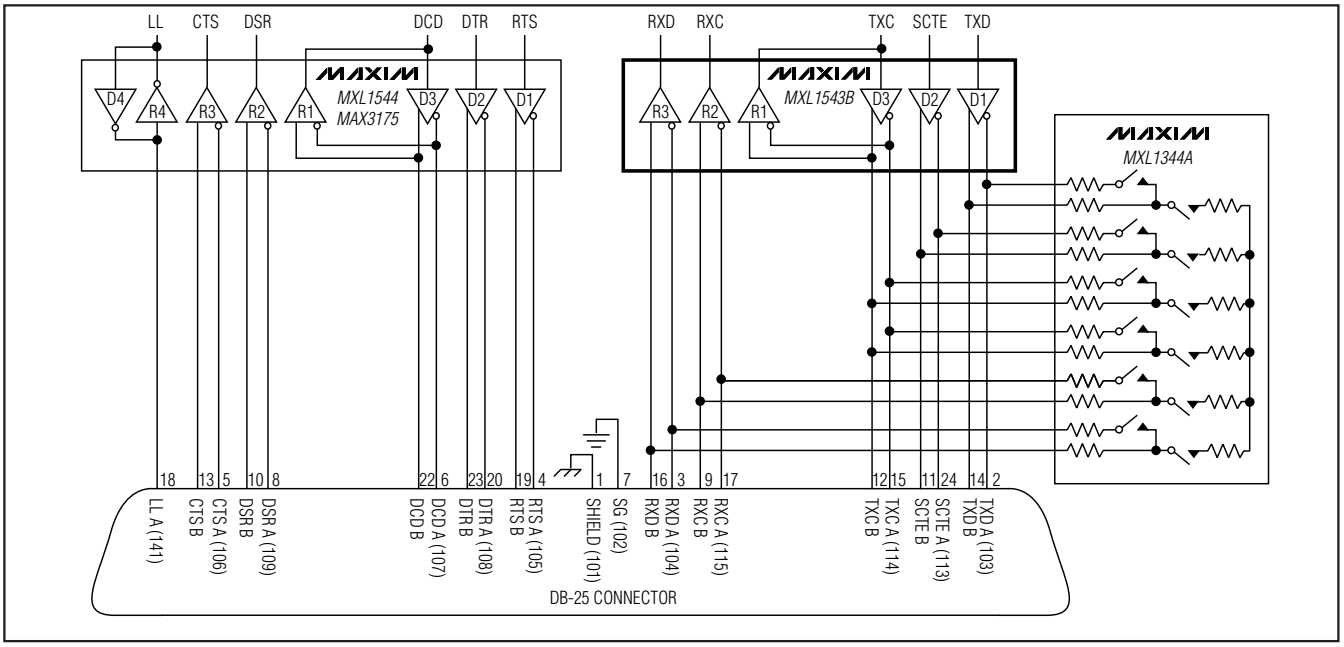
- **MXL1543B, MXL1544/MAX3175, and MXL1344A Chipset Is Pin Compatible with LTC1543, LTC1544, and LTC1344A**
- **Supports RS-232, RS-449, EIA-530, EIA-530A, V.35, V.36, and X.21**
- **Software-Selectable Cable Termination Using the MXL1344A**
- **Complete DTE or DCE Port with MXL1544/MAX3175, and MXL1344A**
- **+5V Single-Supply Operation**
- **0.5µA No-Cable Mode**
- **TUV-Certified NET1/NET2 and TBR1/TBR2-Compliant**

Ordering Information

PART	TEMP RANGE	PIN-PACKAGE
MXL1543BCAI	0° to +70°C	28 SSOP

Pin Configuration appears at end of data sheet.

Typical Operating Circuit



+5V Multiprotocol, 3Tx/3Rx, Software-Selectable Clock/Data Transceivers

ABSOLUTE MAXIMUM RATINGS

All Voltages Referenced to GND Unless Otherwise Noted.
Supply Voltages
V_{CC} .....-0.3V to +6V
V_{DD} .....-0.3V to +7.3V
V_{EE} .....+0.3V to -6.5V
V_{DD} to V_{EE} (Note 1).....13V
Logic Input Voltages
M0, M1, M2, DCE/$\overline{DTE}$, T_IN.....-0.3V to +6V
Logic Output Voltages
R_OUT.....-0.3V to (V_{CC} + 0.3V)
Transmitter Outputs
T_OUT_, T3OUT_/R1IN_.....-15V to +15V
Short-Circuit Duration.....Continuous
Receiver Input
R_IN_T3OUT_/R1IN_.....-15V to +15V
R_IN A to R_IN B.....-15V to 0V or 0V to +15V
Continuous Power Dissipation (T_A = +70°C)
28-Pin SSOP (derate 9.5mW/°C above +70°C) 762mW
Operating Temperature Range
MXL1543BCAI .....0°C to 70°C
Junction Temperature .....150°C
Storage Temperature Range .....-65°C to +150°C
Lead Temperature (soldering, 10s) .....+300°C

Note 1: V_{DD} and V_{EE} absolute difference cannot exceed 13V.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(V_{CC} = +5.0V, C1 = C2 = C4 = 1µF, C3 = C5 = 4.7µF, (Figure 10), T_A = T_{MIN} to T_{MAX}. Typical values are at T_A = +25°C, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
DC CHARACTERISTICS						
V_{CC} Operating Range	V_{CC}		4.75		5.25	V
Supply Current (DCE Mode) (Digital Inputs = GND or V_{CC}) (Transmitter Outputs Static)	I_{CC}	RS-530, RS-530A, X.21, no load		13		mA
		RS-530, RS-530A, X.21, full load		100	130	
		V.35 mode, no load		20		
		V.35 mode, full load		126	170	
		V.28 mode, no load		20		
		V.28 mode, full load		40	75	
		No-cable mode		0.5	10	µA
Internal Power Dissipation (DCE Mode)	P_D	RS-530, RS-530A, X.21, full load		230		mW
		V.35 mode, full load		600		
		V.28 mode, full load		140		
Positive Charge-Pump Output Voltage	V_{DD}	Any mode (except no-cable mode), no load	6.4	6.8		V
		V.28 mode, with load	6.4	6.8		
		V.28, V.35 modes, with load, I_{DD} = 10mA	6.4	6.8		
Negative Charge-Pump Output Voltage	V_{EE}	V.28, V.35, no load		-5.6		V
		V.28 mode, full load		-5.6	-5.4	
		V.35 mode, full load		-5.6	-5.4	
		RS-530, RS-530A, X.21, full load		-5.6	-5.4	
Supply Rise Time	t_r	No-cable mode or power-up to turn on		500		µs
LOGIC INPUTS (M0, M1, M2, DCE/$\overline{DTE}$, T1IN, T2IN, T3IN)						
Input High Voltage	V_{IH}		2.0			V
Input Low Voltage	V_{IL}				0.8	
Logic Input Current	I_{IN}	T1IN, T2IN, T3IN			±10	µA
		M0, M1, M2, DCE/$\overline{DTE}$ = GND	-100	-50	-30	
		M0, M1, M2, DCE/$\overline{DTE}$ = V_{CC}			±10	

ELECTRICAL CHARACTERISTICS (continued)

(V_{CC} = +5.0V, C1 = C2 = C4 = 1µF, C3 = C5 = 4.7µF, (Figure 10), T_A = T_{MIN} to T_{MAX}. Typical values are at T_A = +25°C, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
LOGIC OUTPUTS (R1OUT, R2OUT, R3OUT)						
Output High Voltage	V_{OH}	I_{SOURCE} = 4mA	3	4.5		V
Output Low Voltage	V_{OL}	I_{SINK} = 4mA		0.3	0.8	V
Output Short-Circuit Current	I_{SC}	0 ≤ V_{OUT} ≤ V_{CC}			±50	mA
Output Pullup Current	I_L	V_{OUT} = 0, no-cable mode		70		µA
V.11 TRANSMITTER						
Open-Circuit Differential Output Voltage	V_{ODO}	Open circuit, R = 1.95kΩ (Figure 1)			±5	V
Loaded Differential Output Voltage	V_{ODL}	R = 50Ω (Figure 1), T_A = +25°C	0.5 × V_{ODO}		0.67 × V_{ODO}	V
		R = 50Ω (Figure 1)	±2			
Change in Magnitude of Output Differential Voltage	ΔV_{OD}	R = 50Ω (Figure 1)			0.2	V
Common-Mode Output Voltage	V_{OC}	R = 50Ω (Figure 1)			3.0	V
Change in Magnitude of Output Common-Mode Voltage	ΔV_{OC}	R = 50Ω (Figure 1)			0.2	V
Short-Circuit Current	I_{SC}	V_{OUT} = GND			150	mA
Output Leakage Current	I_Z	-0.25V ≤ V_{OUT} ≤ +0.25V, power-off or no-cable mode		±1	±100	µA
Rise or Fall Time	t_r, t_f	(Figures 2, 6)	2	10	25	ns
Transmitter Input to Output Delay	t_{PHL} , t_{PLH}	(Figures 2, 6)		40	80	ns
Data Skew	$\lvert t_{PHL} - t_{PLH} \rvert$	(Figures 2, 6)		2	12	ns
Output to Output Skew	t_{SKEW}	(Figures 2, 6)		3		ns
V.11 RECEIVER						
Differential Threshold Voltage	V_{TH}	-7V ≤ V_{CM} ≤ 7V	-200		200	mV
Input Hysteresis	ΔV_{TH}	-7V ≤ V_{CM} ≤ 7V		15	40	mV
Receiver Input Current	I_{IN}	-10V ≤ $V_{A, B}$ ≤10V			±0.66	mA
Receiver Input Resistance	R_{IN}	-10V ≤ $V_{A, B}$ ≤ 10V	15	30		kΩ
Rise or Fall Time	t_r, t_f	(Figures 2, 7)		15		ns
Receiver Input to Output Delay	t_{PHL},t_{PLH}	(Figures 2, 7)		50	80	ns
Data Skew	$\lvert t_{PHL} - t_{PLH} \rvert$	(Figures 2, 7)		2	16	ns
V.35 TRANSMITTER						
Differential Output Voltage	V_{OD}	Open circuit (Figure 3)			±7	V
		With load, -4V ≤ V_{CM} ≤ 4V (Figure 3)	±0.44	±0.55	±0.66	
Output High Current	I_{OH}	$V_{A,B}$ = 0	-13	-11	-9	mA
Output Low Current	I_{OL}	$V_{A,B}$ = 0	9	11	13	mA

+5V Multiprotocol, 3Tx/3Rx, Software-Selectable Clock/Data Transceivers

ELECTRICAL CHARACTERISTICS (continued)

(V_{CC} = +5.0V, C1 = C2 = C4 = 1µF, C3 = C5 = 4.7µF, (Figure 10), T_A = T_{MIN} to T_{MAX}. Typical values are at T_A = +25°C, unless otherwise noted.)

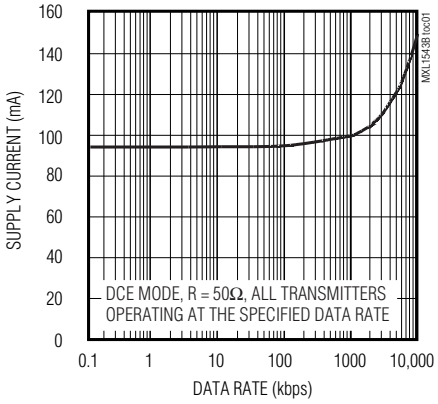
PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Output Leakage Current	I_Z	-0.25V ≤ V_{OUT} ≤ +0.25V, power-off or no-cable mode		±1	±100	µA
Rise or Fall Time	t_r, t_f	(Figures 3, 6)		5		ns
Transmitter Input to Output Delay	t_{PHL}, t_{PLH}	(Figures 3, 6)		35	80	ns
Data Skew	$\lvert t_{PHL} - t_{PLH} \rvert$	(Figures 3, 6)		2	16	ns
Output-to-Output Skew	t_{SKEW}	(Figures 3, 6)		4		ns
V.35 RECEIVER						
Differential Input Voltage	V_{TH}	-2V ≤ V_{CM} ≤ 2V (Figure 3)	-200		200	mV
Input Hysteresis	ΔV_{TH}	-2V ≤ V_{CM} ≤ 2V (Figure 3)		15	40	mV
Receiver Input Current	I_{IN}	-10V ≤ $V_{A,B}$ ≤ 10V			±0.66	mA
Receiver Input Resistance	R_{IN}	-10V ≤ $V_{A,B}$ ≤ 10V	15	30		kΩ
Rise or Fall Time	t_r, t_f	(Figures 3, 7)		15		ns
Receiver Input to Output Delay	t_{PHL}, t_{PLH}	(Figures 3, 7)		50	80	ns
Data Skew	$\lvert t_{PHL} - t_{PLH} \rvert$	(Figures 3, 7)		2	16	ns
V.28 TRANSMITTER						
Output Voltage Swing (Figure 4)	V_O	Open circuit			±7	V
		R_L = 3kΩ	±5	±6		
Short-Circuit Current	I_{SC}				±150	mA
Output Leakage Current	I_Z	-0.25V ≤ V_{OUT} ≤ +0.25V, power-off or no-cable mode		±1	±100	µA
Output Slew Rate	SR	R_L = 3kΩ, C_L = 2500pF (Figures 4, 8)	4		30	V/µs
Transmitter Input to Output Delay	t_{PHL}	R_L = 3kΩ, C_L = 2500pF (Figures 4, 8)		1.5	2.5	µs
Transmitter Input to Output Delay	t_{PLH}	R_L = 3kΩ, C_L = 2500pF (Figures 4, 8)		1.5	3	µs
V.28 RECEIVER						
Input Threshold Low	V_{IL}		0.8	1.2		V
Input Threshold High	V_{IH}			1.2	2.0	V
Input Hysteresis	V_{HYST}			0.05	0.3	V
Input Resistance	R_{IN}	-15V ≤ V_{IN} ≤ +15V	3	5	7	kΩ
Rise or Fall Time	t_r, t_f	(Figures 5, 9)		15		ns
Receiver Input to Output Delay	t_{PHL}	(Figures 5, 9)		60	100	ns
Receiver Input to Output Delay	t_{PLH}	(Figures 5, 9)		160	250	ns

+5V Multiprotocol, 3Tx/3Rx, Software-Selectable Clock/Data Transceivers

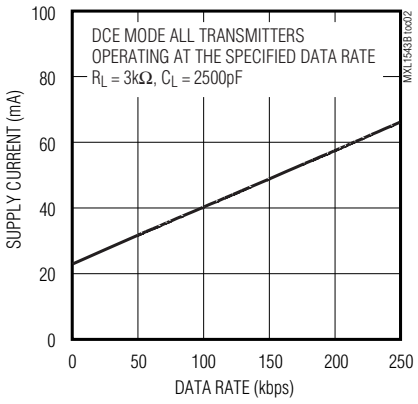
Typical Operating Characteristics

(V_{CC} = +5.0V, C1 = C2 = C4 =1µF, C3 = C5 = 4.7µF, (Figure 10), T_A = T_{MIN} to T_{MAX}, T_A = +25°C, unless otherwise noted.)

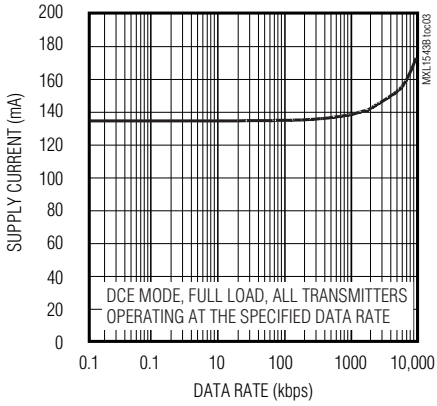
V.11 SUPPLY CURRENT vs. DATA RATE



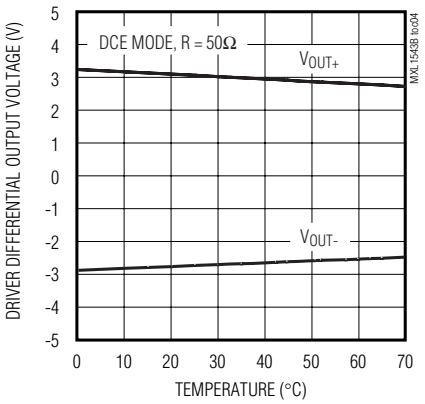
V.28 SUPPLY CURRENT vs. DATA RATE



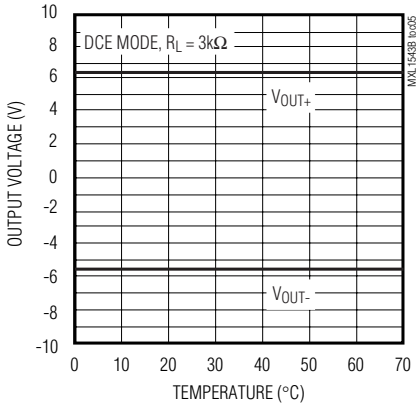
V.35 SUPPLY CURRENT vs. DATA RATE



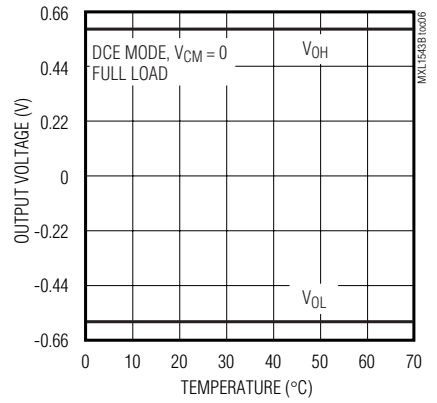
V.11 DRIVER DIFFERENTIAL OUTPUT VOLTAGE vs. TEMPERATURE



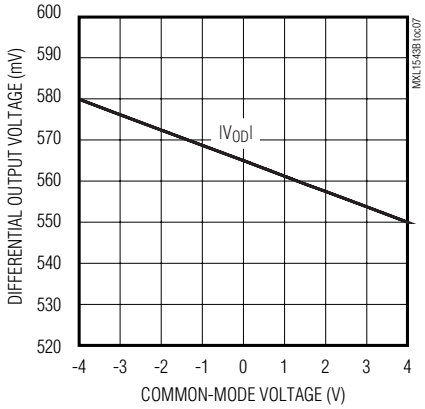
V.28 OUTPUT VOLTAGE vs. TEMPERATURE



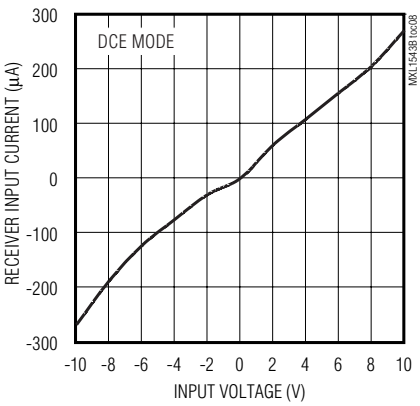
V.35 OUTPUT VOLTAGE vs. TEMPERATURE



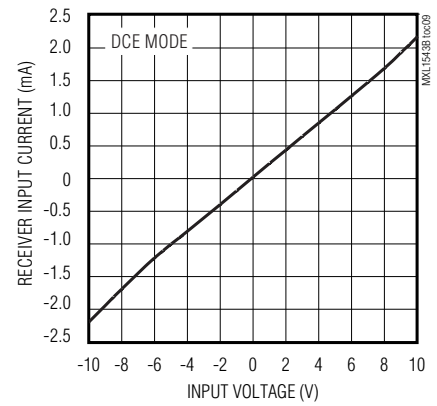
V.35 DIFFERENTIAL OUTPUT VOLTAGE vs. COMMON-MODE VOLTAGE



V.11/V.35 RECEIVER INPUT CURRENT vs. INPUT VOLTAGE



V.28 RECEIVER INPUT CURRENT vs. INPUT VOLTAGE

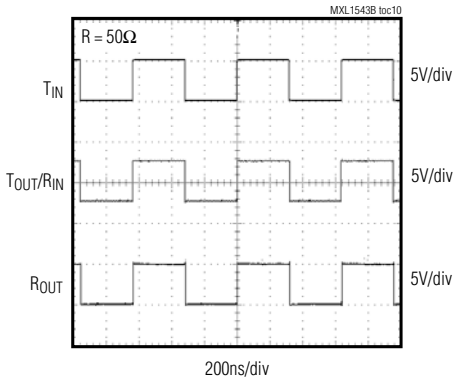


+5V Multiprotocol, 3Tx/3Rx, Software-Selectable Clock/Data Transceivers

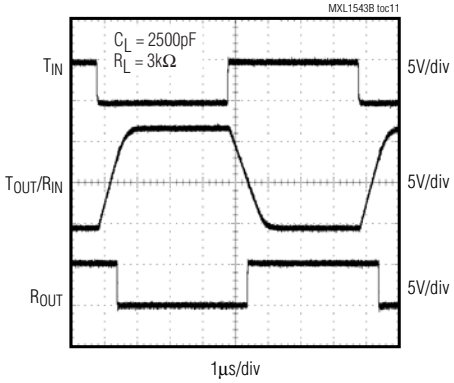
Typical Operating Characteristics (continued)

(V_{CC} = +5.0V, C1= C2 = C4 =1µF, C3 = C5 = 4.7µF (Figure 10), T_A = +25°C, unless otherwise noted.)

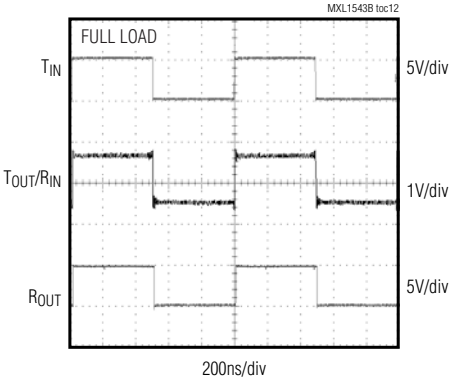
V.11 LOOPBACK OPERATION



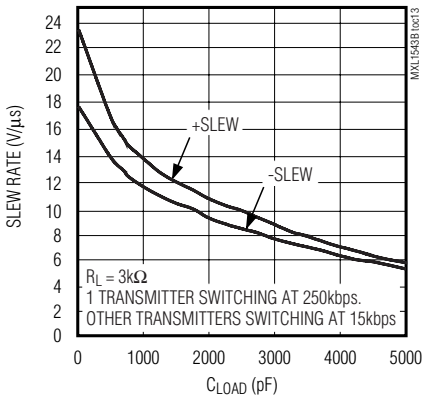
V.28 LOOPBACK OPERATION



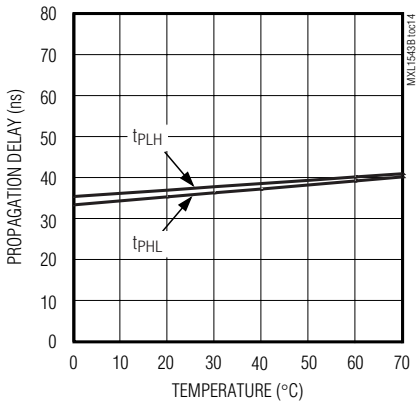
V.35 LOOPBACK OPERATION



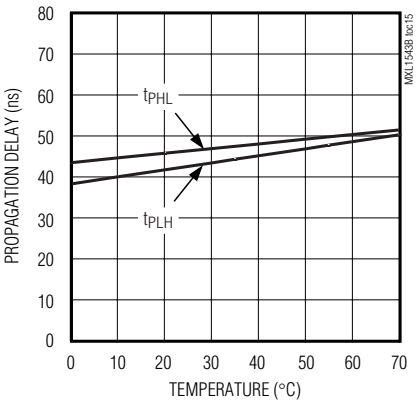
V.28 SLEW RATE vs. C_{LOAD}



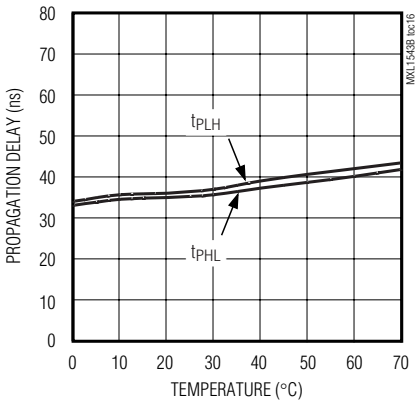
V.11 TRANSMITTER PROPAGATION DELAY vs. TEMPERATURE



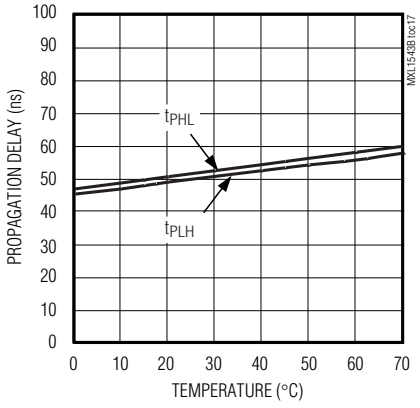
V.11 RECEIVER PROPAGATION DELAY vs. TEMPERATURE



V.35 TRANSMITTER PROPAGATION DELAY vs. TEMPERATURE



V.35 RECEIVER PROPAGATION DELAY vs. TEMPERATURE



Test Circuits

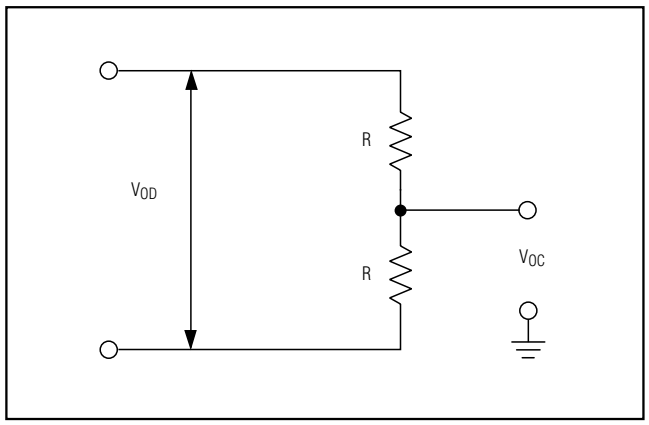


Figure 1. V.11 DC Test Circuit

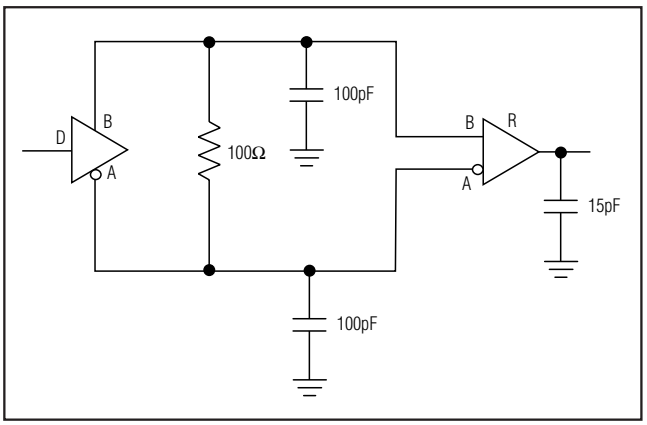


Figure 2. V.11 AC Test Circuit

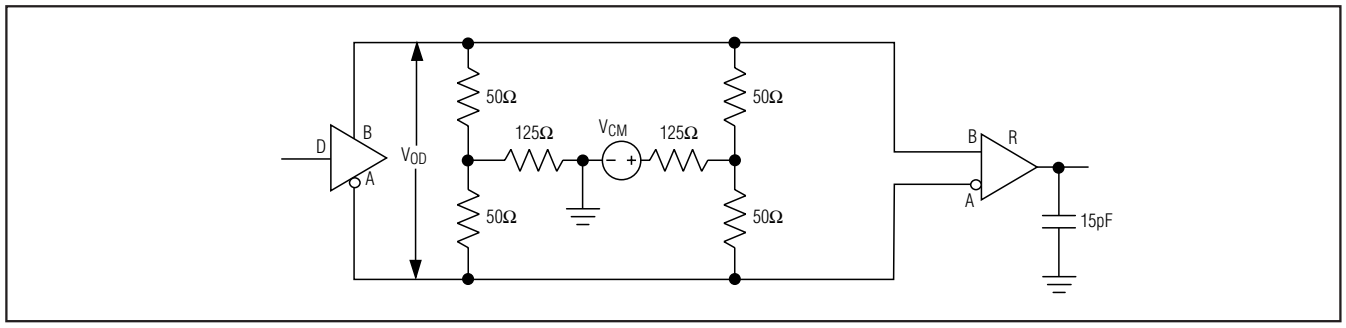


Figure 3. V.35 Transmitter/Receiver Test Circuit

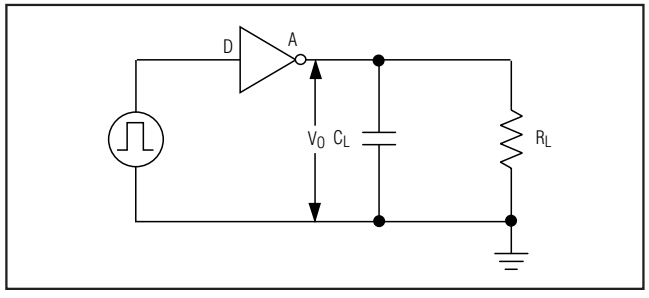


Figure 4. V.28 Driver Test Circuit

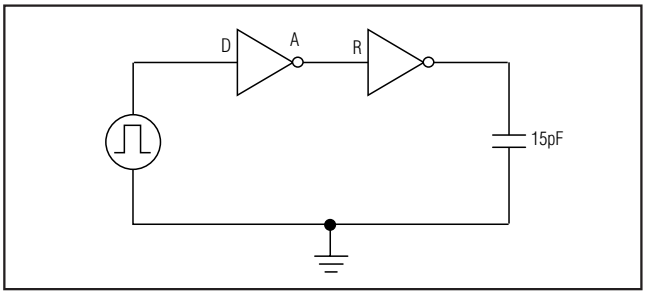


Figure 5. V.28 Receiver Test Circuit

+5V Multiprotocol, 3Tx/3Rx, Software-Selectable Clock/Data Transceivers

Timing Diagrams

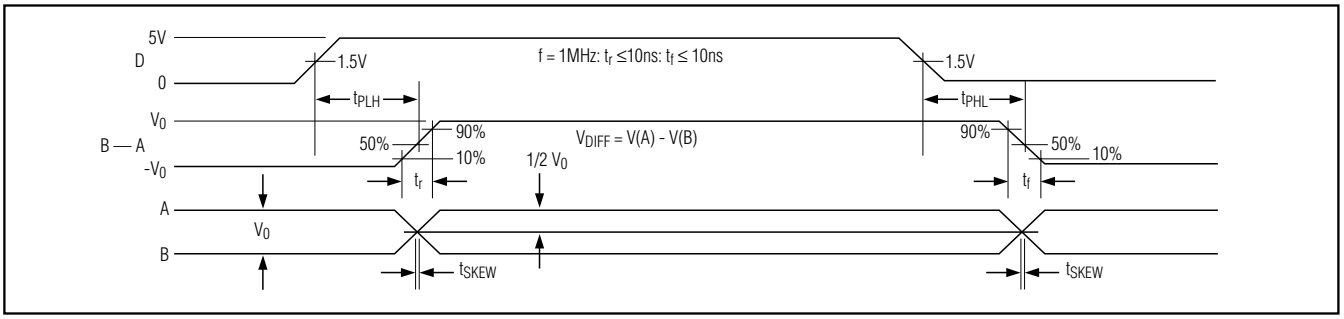


Figure 6. V.11, V.35 Driver Propagation Delays

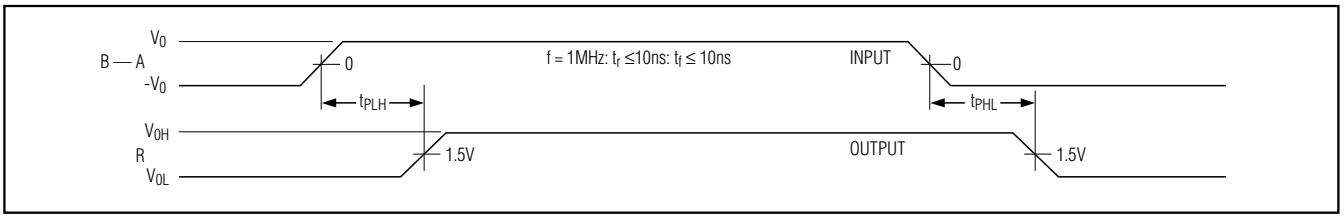


Figure 7. V.11, V.35 Receiver Propagation Delays

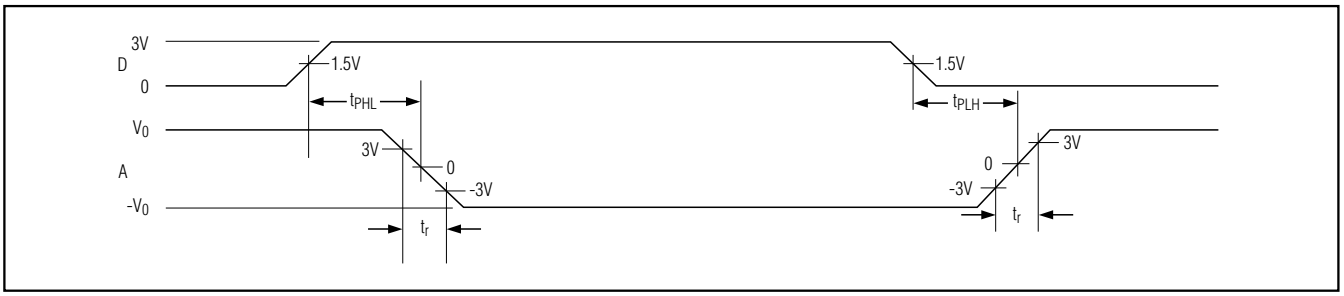


Figure 8. V.28 Driver Propagation Delays

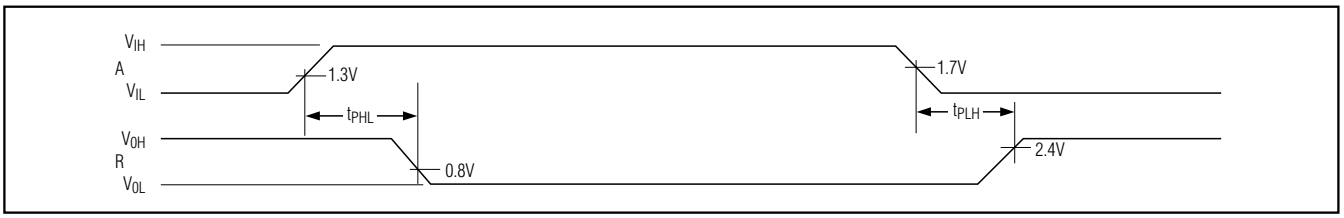


Figure 9. V.28 Receiver Propagation Delays

Pin Description

PIN	NAME	FUNCTION
1	C1-	Capacitor C1 Negative Terminal. Connect a 1µF ceramic capacitor between C1+ and C1-.
2	C1+	Capacitor C1 Positive Terminal. Connect a 1µF ceramic capacitor between C1+ and C1-.
3	V_{DD}	Generated Positive Supply. Connect a 4.7µF ceramic capacitor to ground.
4	V_{CC}	+5V Supply Voltage (±5%). Decouple with a 1µF capacitor to ground.
5	T1IN	Transmitter 1 TTL-Compatible Input
6	T2IN	Transmitter 2 TTL-Compatible Input
7	T3IN	Transmitter 3 TTL-Compatible Input
8	R1OUT	Receiver 1 CMOS Output
9	R2OUT	Receiver 2 CMOS Output
10	R3OUT	Receiver 3 CMOS Output
11	M0	Mode-Select Pin with Internal Pullup to V_{CC}
12	M1	Mode-Select Pin with Internal Pullup to V_{CC}
13	M2	Mode-Select Pin with Internal Pullup to V_{CC}
14	DCE/$\overline{DTE}$	DCE/DTE Mode-Select Pin with Internal Pullup to V_{CC}
15	R3INB	Noninverting Receiver Input
16	R3INA	Inverting Receiver Input
17	R2INB	Noninverting Receiver Input
18	R2INA	Inverting Receiver Input
19	T3OUTB/R1INB	Noninverting Transmitter Output/Noninverting Receiver Input
20	T3OUTA/R1INA	Inverting Transmitter Output/Inverting Receiver Input
21	T2OUTB	Noninverting Transmitter Output
22	T2OUTA	Inverting Transmitter Output
23	T1OUTB	Noninverting Transmitter Output
24	T1OUTA	Inverting Transmitter Output
25	GND	Ground
26	V_{EE}	Generated Negative Supply. Connect a 4.7µF ceramic capacitor to ground.
27	C2-	Capacitor C2 Negative Terminal. Connect a 1µF ceramic capacitor between C2+ and C2-.
28	C2+	Capacitor C2 Positive Terminal. Connect a 1µF ceramic capacitor between C2+ and C2-.

Detailed Description

The MXL1543B is a three-driver/three-receiver, multiprotocol transceiver that operates from a single +5V supply. The MXL1543B, along with the MXL1544/MAX3175 and MXL1344A, form a complete software-selectable DTE or DCE interface port that supports the V.28 (RS-232), V.10/V.11 (RS-449/V.36, EIA-530, EIA-530A, X.21), and V.35 protocols. The MXL1543B transceivers carry the high-speed clock and data signals, while the MXL1544/MAX3175 transceivers carry serial interface control signaling. The MXL1543B can be terminated by the MXL1344A software-selectable resistor termination network or by a discrete termination network. The MXL1543B features a 0.5µA no-cable mode, true fail-safe operation, and thermal shutdown circuitry. Thermal shutdown protects the drivers against excessive power dissipation. When activated, the thermal shutdown circuitry places the driver outputs into a high-impedance state.

Mode Selection

The state of the mode-select pins M0, M1, and M2 determines which serial interface protocol is selected (Table 1). The state of the DCE/$\overline{DTE}$ input determines whether the transceiver will be configured as a DTE or DCE serial port. When the DCE/$\overline{DTE}$ input is logic HIGH, driver T3 is activated and receiver R1 is disabled. When the DCE/$\overline{DTE}$ input is logic LOW, driver T3 is disabled and receiver R1 is activated. M0, M1, M2,

+5V Multiprotocol, 3Tx/3Rx, Software-Selectable Clock/Data Transceivers

Table 1. Mode Selection

MXL1543B MODE NAME	M2	M1	M0	DCE/$\overline{\text{DTE}}$	T1	T2	T3	R1	R2	R3
Not Used (Default V.11)	0	0	0	0	V.11	V.11	Z	V.11	V.11	V.11
RS-530A	0	0	1	0	V.11	V.11	Z	V.11	V.11	V.11
RS-530	0	1	0	0	V.11	V.11	Z	V.11	V.11	V.11
X.21	0	1	1	0	V.11	V.11	Z	V.11	V.11	V.11
V.35	1	0	0	0	V.35	V.35	Z	V.35	V.35	V.35
RS-449/V.36	1	0	1	0	V.11	V.11	Z	V.11	V.11	V.11
V.28/RS-232	1	1	0	0	V.28	V.28	Z	V.28	V.28	V.28
No Cable	1	1	1	0	Z	Z	Z	Z	Z	Z
Not Used (Default V.11)	0	0	0	1	V.11	V.11	V.11	Z	V.11	V.11
RS-530A	0	0	1	1	V.11	V.11	V.11	Z	V.11	V.11
RS-530	0	1	0	1	V.11	V.11	V.11	Z	V.11	V.11
X.21	0	1	1	1	V.11	V.11	V.11	Z	V.11	V.11
V.35	1	0	0	1	V.35	V.35	V.35	Z	V.35	V.35
RS-449/V.36	1	0	1	1	V.11	V.11	V.11	Z	V.11	V.11
V.28/RS-232	1	1	0	1	V.28	V.28	V.28	Z	V.28	V.28
No Cable	1	1	1	1	Z	Z	Z	Z	Z	Z

and DCE/$\overline{\text{DTE}}$ are internally pulled up to V_{CC} to ensure a logic HIGH if left unconnected.

No-Cable Mode

The MXL1543B will enter no-cable mode when the mode-select pins are left unconnected or connected high (M0 = M1 = M2 = 1). In this mode, the multiprotocol drivers and receivers are disabled and the supply current drops to 0.5µA. The receivers' outputs enter a high-impedance state in no-cable mode, which allow these output lines to be shared with other receivers' outputs (the receivers' outputs have internal pullup resistors to pull the outputs HIGH if not driven). Also, in no-cable mode, the transmitter outputs enter a high-impedance state so that these output lines can be shared with other devices.

Dual Charge-Pump Voltage Converter

The MXL1543B's internal power supply consists of a regulated dual charge pump that provides positive and negative output voltages from a +5V supply. The charge pump operates in discontinuous mode. If the output voltage is less than the regulated voltage, the charge pump is enabled. If the output voltage exceeds the regulated voltage, the charge pump is disabled. Each charge pump requires a flying capacitor (C1, C2) and a reservoir capacitor (C3, C5) to generate the V_{DD} and V_{EE} supplies. Figure 10 shows charge-pump connections.

Fail-Safe Receivers

The MXL1543B guarantees a logic-high receiver output when the receiver inputs are shorted or open, or when they are connected to a terminated transmission line with all the drivers disabled. This is done by setting the receivers' threshold between -25mV and -200mV in the V.11 and V.35 modes. If the differential receiver input

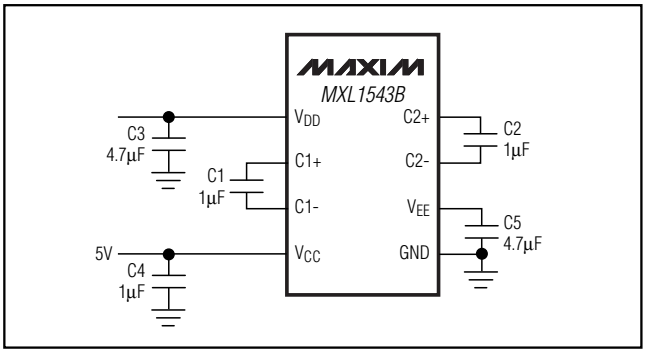


Figure 10. Charge Pump

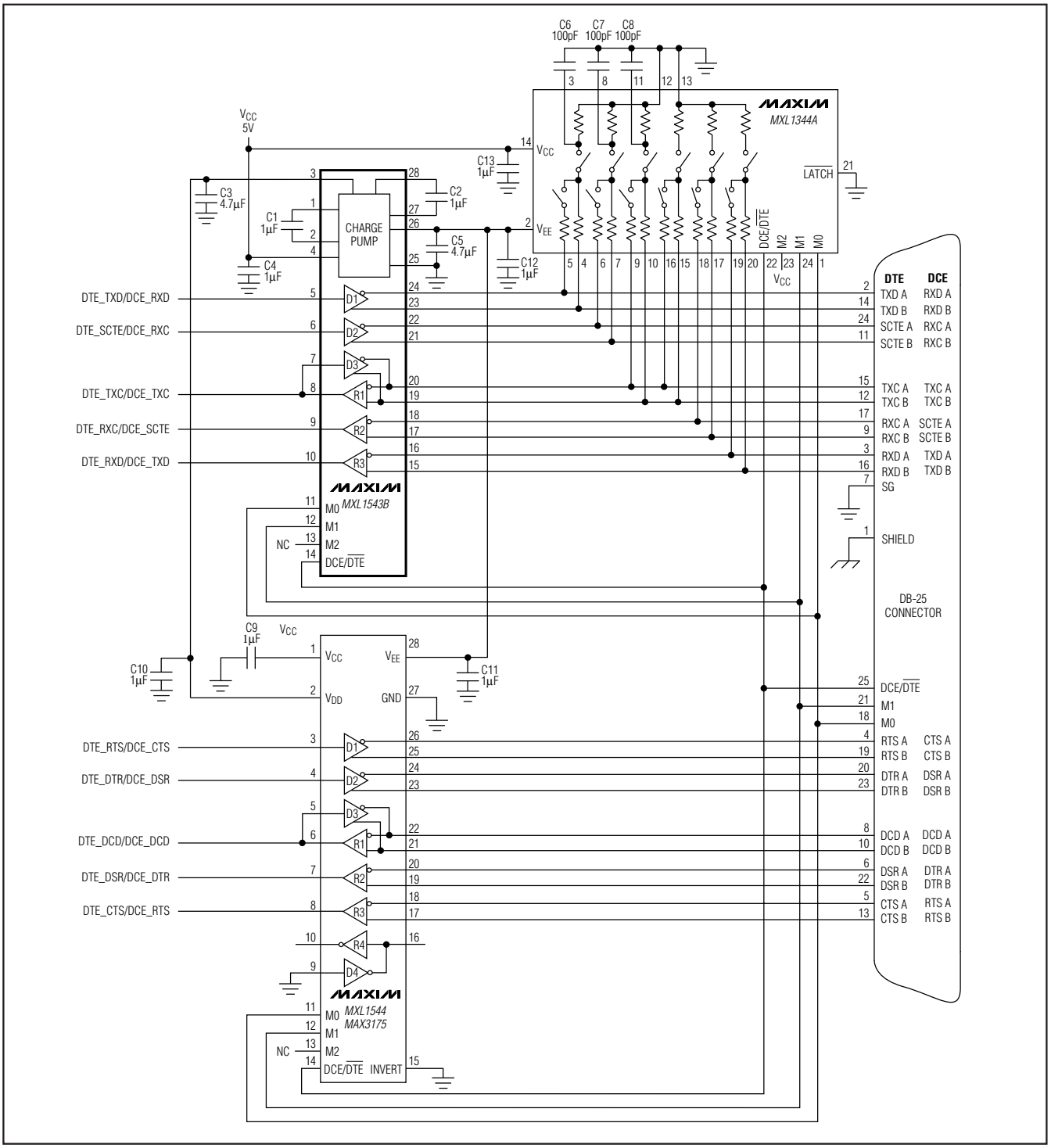


Figure 11. Cable-Selectable Multiprotocol DTE/DCE Port

+5V Multiprotocol, 3Tx/3Rx, Software-Selectable Clock/Data Transceivers

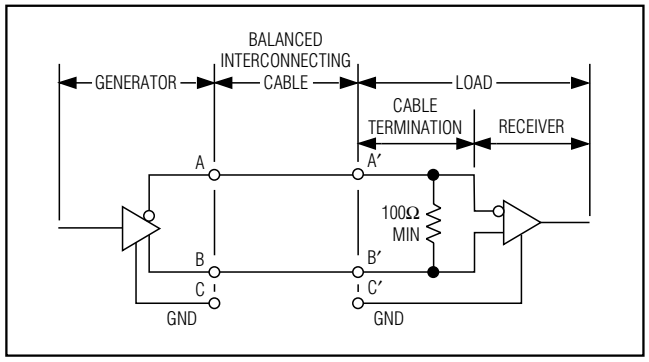


Figure 12. Typical V.11 Interface

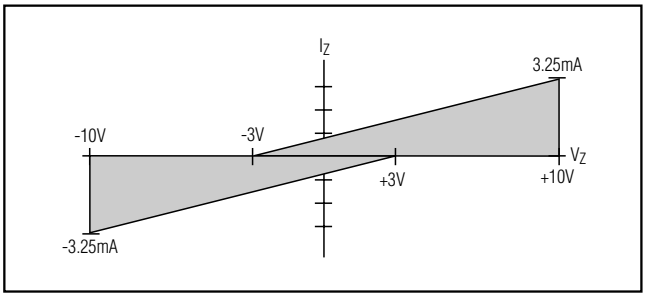


Figure 13. Receiver Input Impedance

voltage (B - A) is ≥ -25mV, R_OUT is logic HIGH. If (B - A) is ≤ -200mV, R_OUT is logic LOW. In the case of a terminated bus with all transmitters disabled, the receiver's differential input voltage is pulled to zero by the termination. With the receiver thresholds of the MXL1543B, this results in a logic HIGH with a 25mV minimum noise margin.

Applications Information

Capacitor Selection

The capacitors used for the charge pumps, as well as for supply bypassing, should have a low equivalent series resistance (ESR) and low temperature coefficient. Multilayer ceramic capacitors with an X7R dielectric offer the best combination of performance, size, and cost. The flying capacitors (C1, C2) and the bypass capacitor (C4) should have a value of 1µF, while the reservoir capacitors (C3, C5) should have a minimum value of 4.7µF (Figure 10). To reduce the ripple present on the transmitter outputs, capacitors C3, C4, and C5 can be increased. The values of C1 and C2 should not be increased.

Cable Termination

The MXL1344A software-selectable resistor network is designed to be used with the MXL1543B. The MXL1344A multiprotocol termination network provides V.11- and V.35-compliant termination, while V.28 receiver termination is internal to the MXL1543B. These cable termination networks provide compatibility with V.11, V.28, and V.35 protocols. Using the MXL1344A termination networks provide the advantage of not having to build expensive termination networks out of resistors and relays, manually changing termination modules, or building custom termination networks

Cable-Selectable Mode

A cable-selectable multiprotocol interface is shown in Figure 11. The mode control lines M0, M1, and DCE/$\overline{\text{DTE}}$ are wired to the DB-25 connector. To select the serial interface mode, the appropriate combination of M0, M1, and DCE/$\overline{\text{DTE}}$ are grounded within the cable wiring. The control lines that are not grounded are pulled high by the internal pullups on the MXL1543B. The serial interface protocol of the MXL1543B, MXL1544/MAX3175, and MXL1344A is selected based on the cable that is connected to the DB-25 interface.

V.11 Interface

As shown in Figure 12, the V.11 protocol is a fully balanced differential interface. The V.11 driver generates a minimum of ±2V between nodes A and B when a 100Ω (min) resistance is presented at the load. The V.11 receiver is sensitive to ±200mV differential signals at receiver inputs A' and B'. The V.11 receiver rejects common-mode signals developed across the cable (referenced from C to C') of up to ±7V, allowing for error-free reception in noisy environments. The receiver inputs must comply with the impedance curve shown in Figure 13.

For high-speed data transmission, the V.11 specification recommends terminating the cable at the receiver with a 100Ω resistor. This resistor, although not required, prevents reflections from corrupting transmitted data. In Figure 14, the MXL1344A is used to terminate the V.11 receiver. Internal to the MXL1344A, S1 is closed and S2 is open to present a 100Ω minimum differential resistance. The MXL1543B's internal V.28 termination is disabled by opening S3.

V.35 Interface

Figure 15 shows a fully-balanced, differential standard V.35 interface. The generator and the load must both present a 100Ω ±10Ω differential impedance and a 150Ω ±15Ω common-mode impedance as shown by the resistive T networks in Figure 15. The V.35 driver generates a current output (±11mA, typ) that develops an output voltage of ±550mV across the generator and load termination networks. The V.35 receiver is sensitive to ±200mV differential signals at receiver inputs A' and B'. The V.35 receiver rejects common-mode sig-

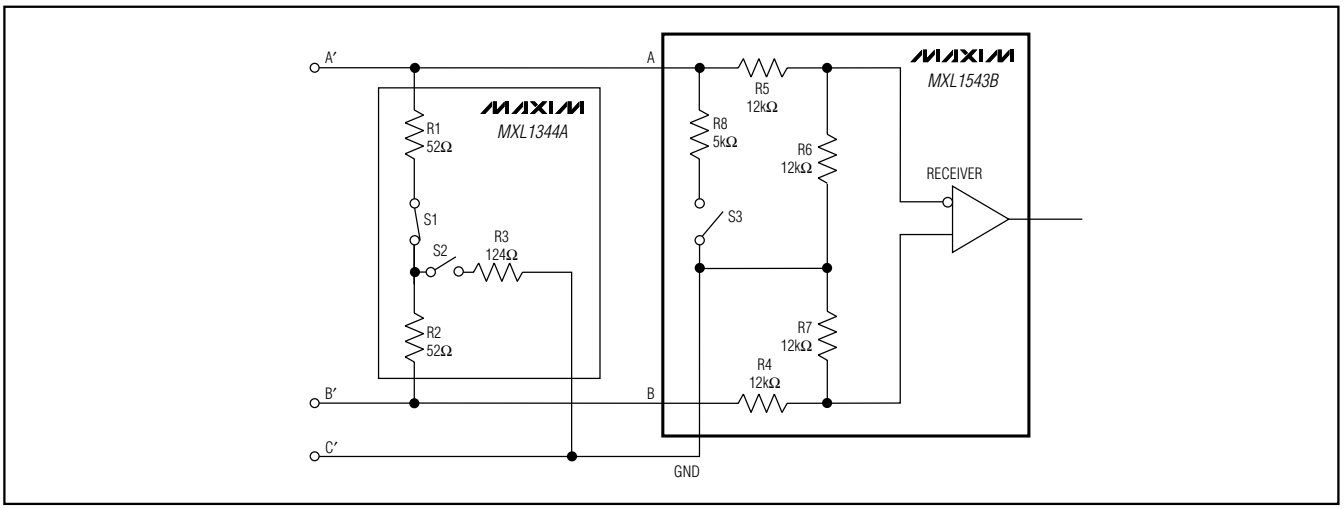


Figure 14. V.11 Termination and Internal Resistance Networks

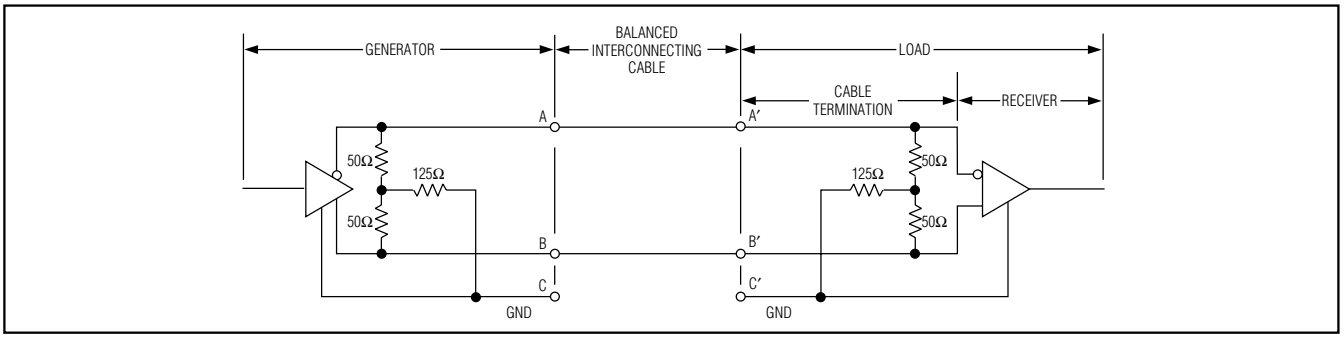


Figure 15. Typical V.35 Interface

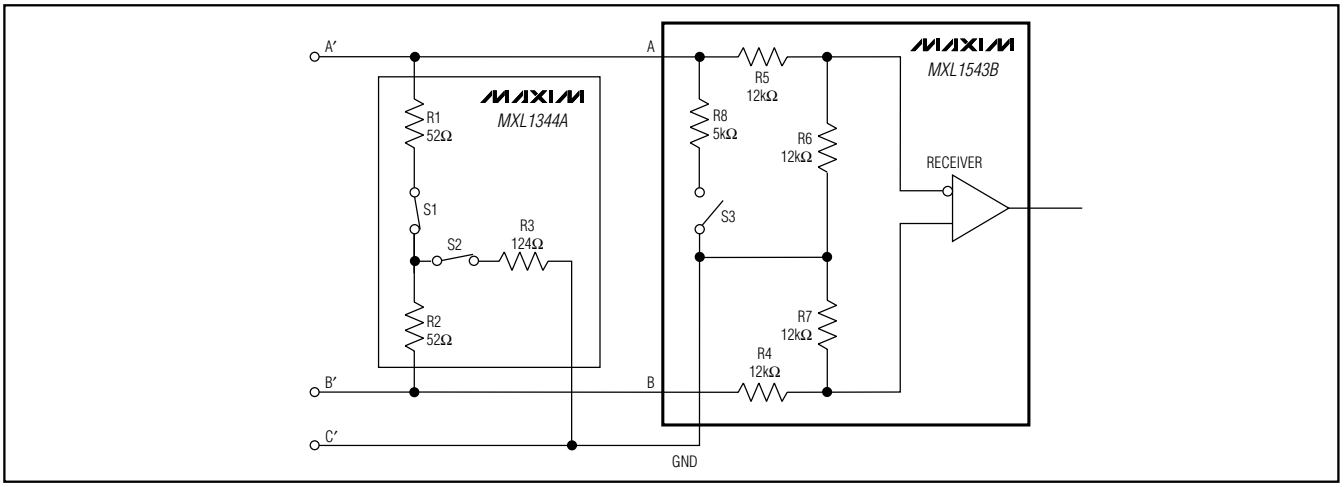


Figure 16. V.35 Termination and Internal Resistance Networks

+5V Multiprotocol, 3Tx/3Rx, Software-Selectable Clock/Data Transceivers

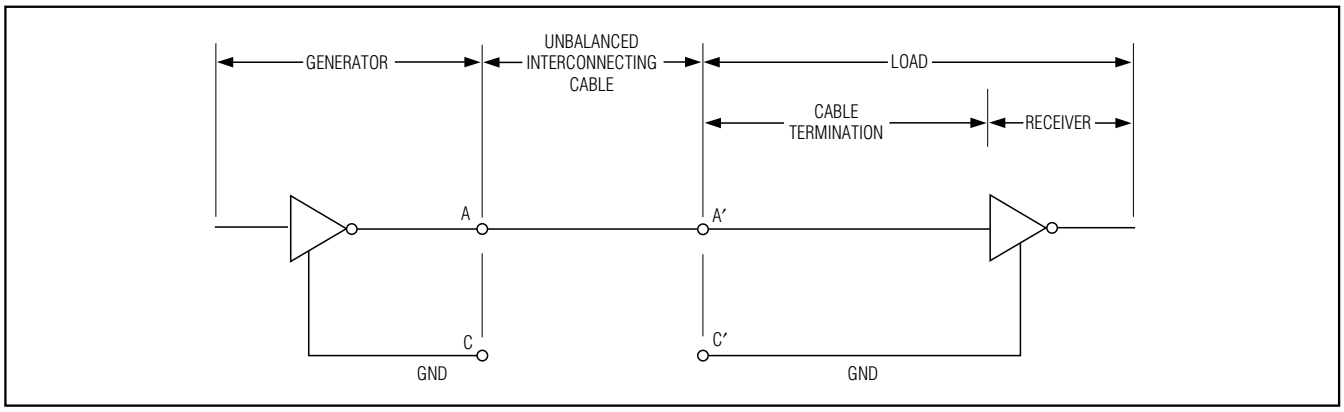


Figure 17. Typical V.28 Interface

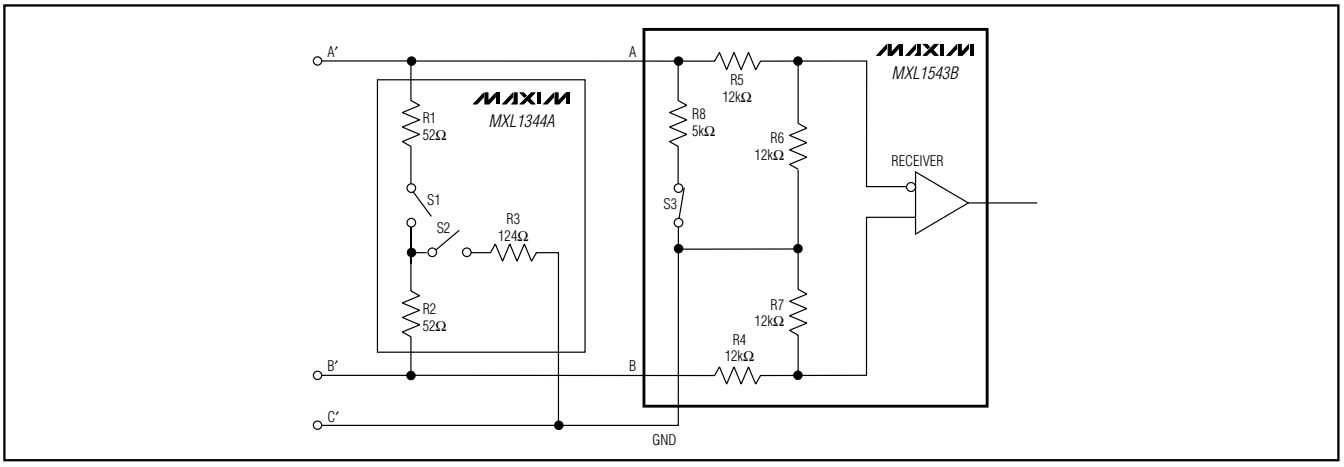


Figure 18. V.28 Termination and Internal Resistance Networks

nals developed across the cable (referenced from C to C') of up to ±4V, allowing for error-free reception in noisy environments.

In Figure 16, the MXL1344A is used to implement the resistive T network that is needed to properly terminate the V.35 driver and receiver. Internal to the MXL1344A, S1 and S2 are closed to connect the T-network resistors to the circuit. The V.28 termination resistor (internal to the MXL1543B) is disabled by opening S3 to avoid interference with the T-network impedance.

V.28 Interface

The V.28 interface is an unbalanced single-ended interface (Figure 17). The V.28 driver generates a minimum of ±5V across a 3kΩ load impedance between A' and C'. The V.28 receiver has a single-ended input. To aid in rejecting system noise, the MXL1543B's V.28 receiver has a typical hysteresis of 0.05V.

Figure 18 shows the MXL1344A's termination network disabled by opening S1 and S2. The MXL1543B's internal 5kΩ V.28 termination is enabled by closing S3.

DTE vs. DCE Operation

Figure 19 shows a DCE or DTE controller-selectable interface. DCE/$\overline{\text{DTE}}$ (pin 14) switches the port's mode of operation. See Table 1.

This application requires only one DB-25 connector, but separate cables for DCE or DTE signal routing. See Figure 19 for complete signal routing in DCE and DTE modes.

Complete Multiprotocol X.21 Interface

A complete DTE-to-DCE interface operating in X.21 mode is shown in Figure 20. The MXL1543B is used to generate the clock and data signals, and the MXL1544/MAX3175 generate the control signals and

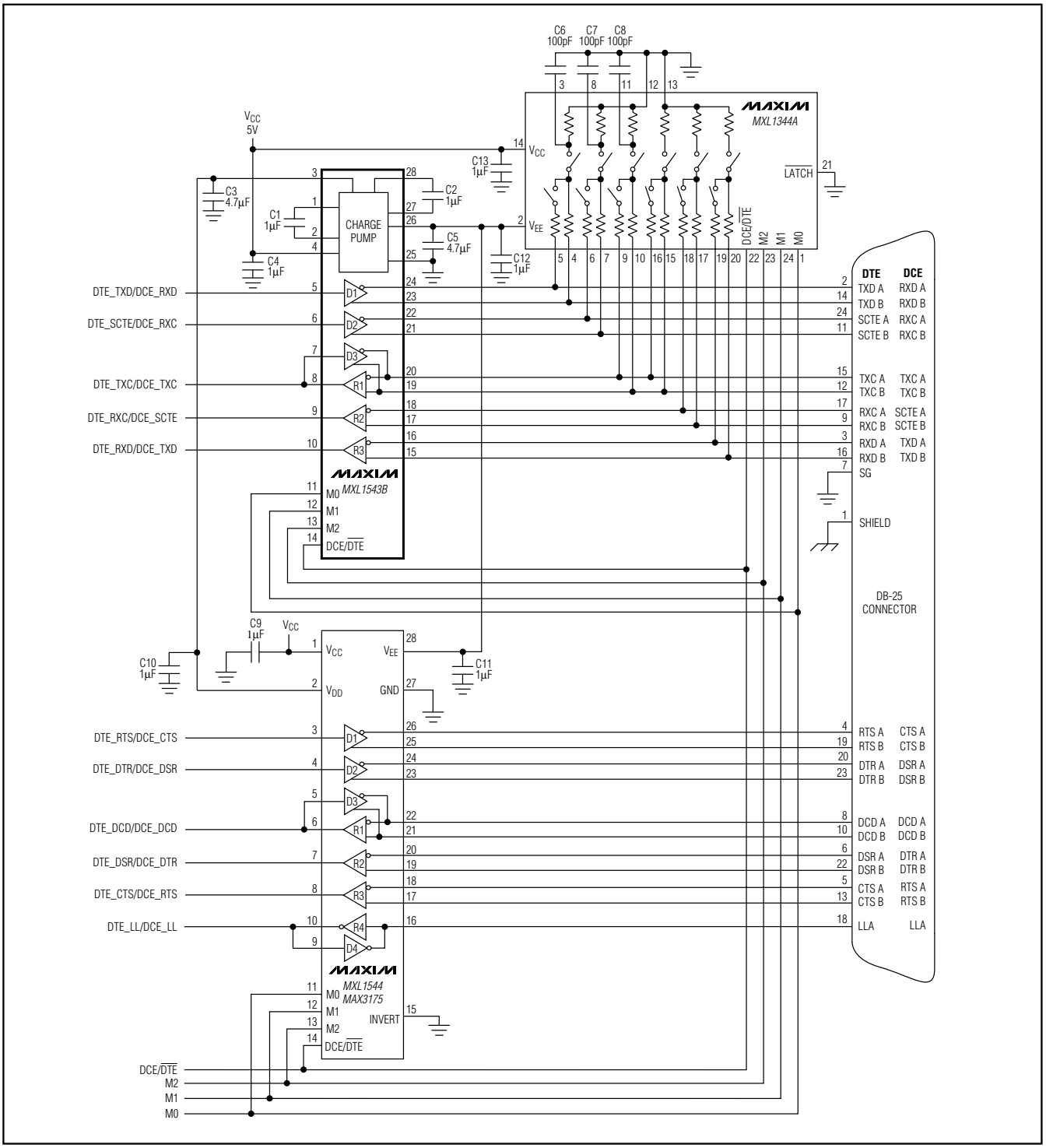


Figure 19. Multiprotocol DCE/DTE Port

+5V Multiprotocol, 3Tx/3Rx, Software-Selectable Clock/Data Transceivers

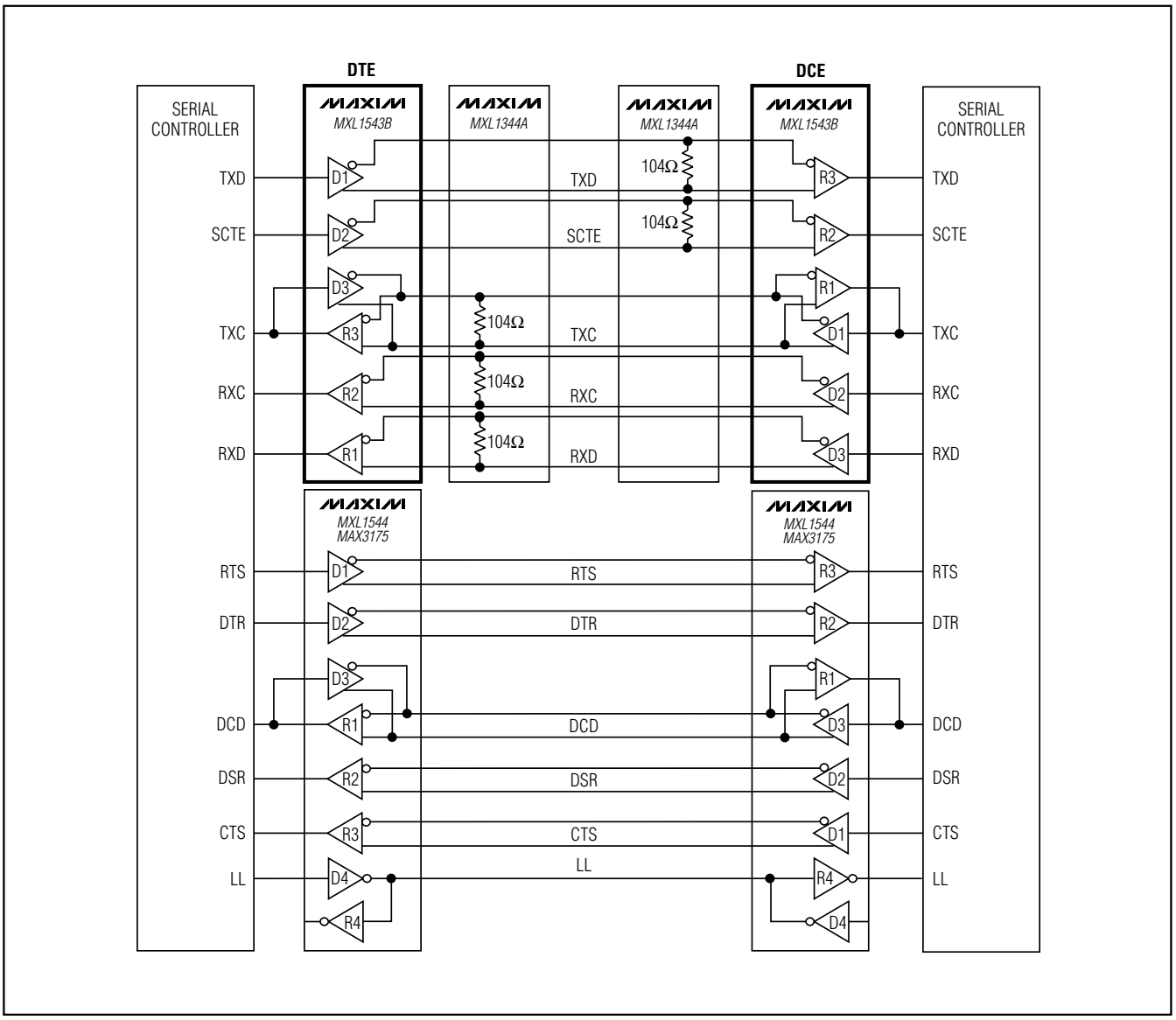


Figure 20. DCE-to-DTE X.21 Interface

local loopback (LL). The MXL1344A is used to terminate the clock and data signals to support the V.11 protocol for cable termination. The control signals do not need external termination.

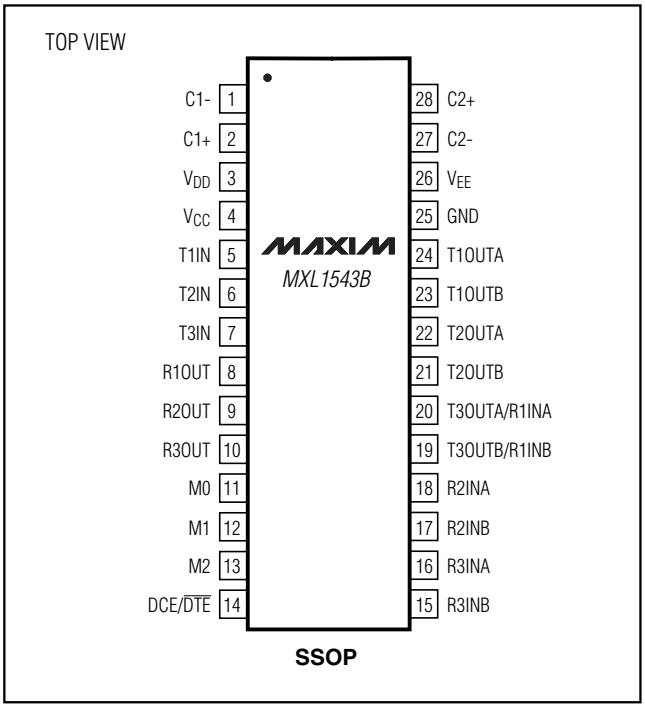
Compliance Testing

A European Standard EN 45001 test report is pending for the MXL1543B/MXL1544/MXL1344A chipset. A copy of the test report will be available from Maxim upon completion.

Chip Information

TRANSISTOR COUNT: 2619
PROCESS: BiCMOS

Pin Configuration

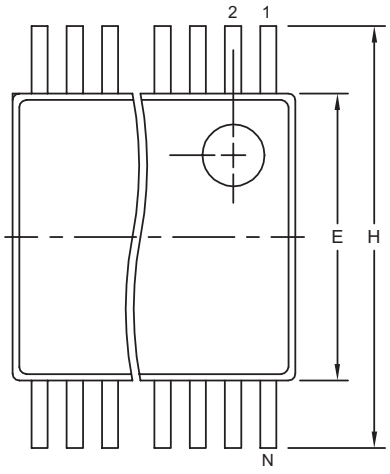


+5V Multiprotocol, 3Tx/3Rx, Software-Selectable Clock/Data Transceivers

Package Information

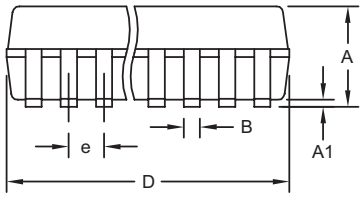
(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information, go to **www.maxim-ic.com/packages**.)

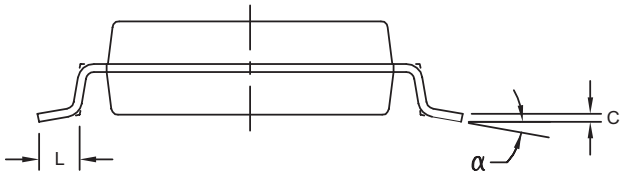
SSOP EPS



	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	0.068	0.078	1.73	1.99
A1	0.002	0.008	0.05	0.21
B	0.010	0.015	0.25	0.38
C	0.004	0.008	0.09	0.20
D	SEE VARIATIONS			
E	0.205	0.212	5.20	5.38
e	0.0256 BSC		0.65 BSC	
H	0.301	0.311	7.65	7.90
L	0.025	0.037	0.63	0.95
α	0∞	8∞	0∞	8∞

	INCHES		MILLIMETERS		
	MIN	MAX	MIN	MAX	N
D	0.239	0.249	6.07	6.33	14L
D	0.239	0.249	6.07	6.33	16L
D	0.278	0.289	7.07	7.33	20L
D	0.317	0.328	8.07	8.33	24L
D	0.397	0.407	10.07	10.33	28L





NOTES:
1. D&E DO NOT INCLUDE MOLD FLASH.
2. MOLD FLASH OR PROTRUSIONS NOT TO EXCEED .15 MM (.006").
3. CONTROLLING DIMENSION: MILLIMETERS.
4. MEETS JEDEC MO150.
5. LEADS TO BE COPLANAR WITHIN 0.10 MM.

DALLAS SEMICONDUCTOR MAXIM

PROPRIETARY INFORMATION

TITLE: PACKAGE OUTLINE, SSOP, 5.3 MM

APPROVAL	DOCUMENT CONTROL NO.	REV.	
	21-0056	C	1/1