# High Efficiency Audio Subsystem

## ISL99203

The ISL99203 is a fully integrated high efficiency class-D mono amplifier combined with a capfree headphone amplifier. It is designed to maximize performance for mobile phone applications while saving valuable board space. The application circuit requires a minimum requirement of external components and operates from a 2.4V to 5.5V input supply.

It is capable of delivering 1.5W of continuous output power with less than 10% THD+N driving a 8Ω load from a 5V supply. The speaker amplifier of the ISL99203 features a high-efficiency, low-noise modulation scheme. It operates with 85% efficiency at 400mW into 8Ω from 5V supply and has a signal-to-noise ratio (SNR) that is greater than 95dB. The architecture of the device allows it to achieve very low level pop and click. This minimizes voltage glitches at the output during turn-on and turn-off, thus reducing audible noise on activation and deactivation. EMI suppression is achieved by SRC (Slew Rate Control). The amplifier passes FCC Radiated Emissions Standards with 24 inches of Cable and achieves greater than 20dB margin under FCC limits.

The class-D amplifier is designed to operate without a low pass output filer thus saving cost and board space. The headphone amplifier is a GND-reference capfree amplifier. It can output up to 35mW into 32Ω at 3.3V.

## Features

- Operating Voltage 2.4V to 5.5V
- Low Quiescent Current
- Low Shutdown Current
- Low RFI Susceptibility
- Integrated Bypass Switch, $I^2C$ Controlled
- $I^2C$ Control Interface
- 40 Step Digital Volume Control
- 3 Independent Volume Channels
- 10 Distinct Output Modes
- Speaker Amp Class-D
- Protection for UV/TSD/OC
- Independent Gain Boost for Headphone and Speaker
- All Digital Interfaces 1.8V Compatible
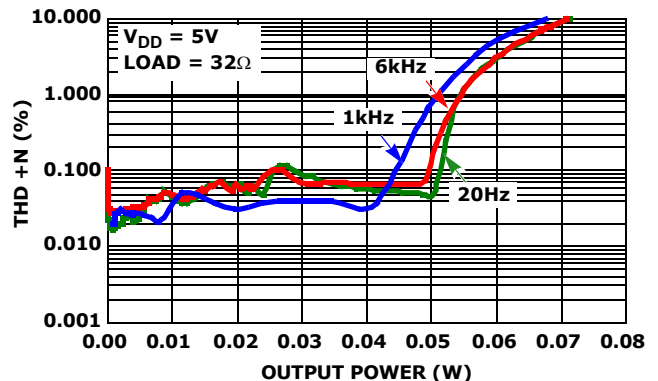- Exposed Pad at Ground Voltage

## Applications*(see page 15)

- Mobile Phones
- PDAs
- Portable Media Players
- Portable Gaming
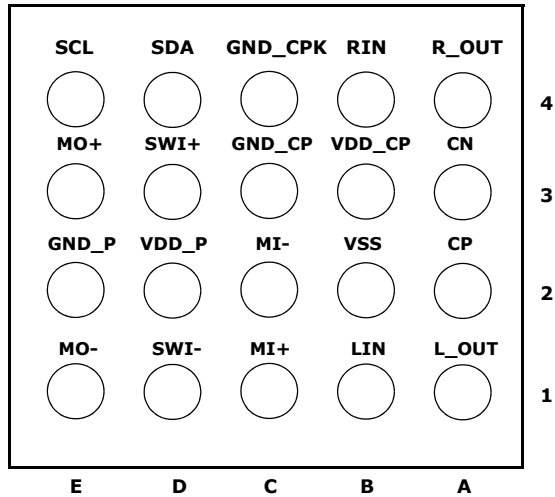
## Total Harmonic Distortion Plus Noise vs Power (Mono)



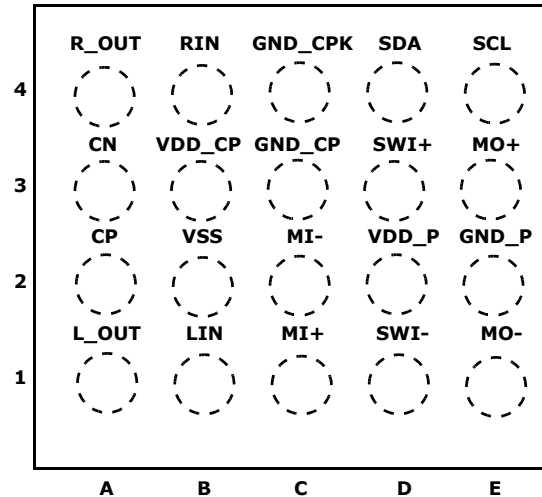## Total Harmonic Distortion Plus Noise vs Power (Headphone)

1
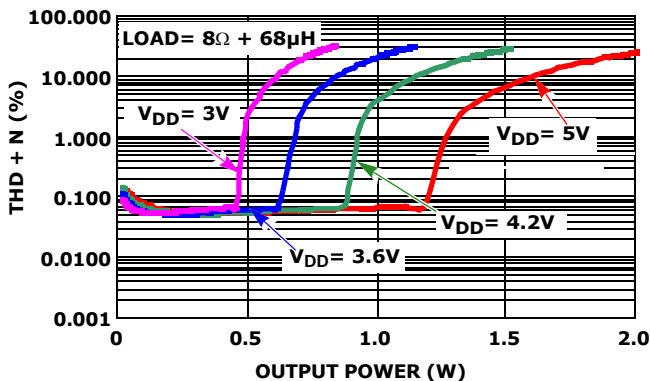
# Pin Configurations

**ISL99203**
**(20 BALL WLCSP)**
BOTTOM VIEW

| | SCL | SDA | GND_CPK | RIN | R_OUT | |
|---|---|---|---|---|---|---|
| | ○ | ○ | ○ | ○ | ○ | 4 |
| | MO+ | SWI+ | GND_CP | VDD_CP | CN | |
| | ○ | ○ | ○ | ○ | ○ | 3 |
| | GND_P | VDD_P | MI- | VSS | CP | |
| | ○ | ○ | ○ | ○ | ○ | 2 |
| | MO- | SWI- | MI+ | LIN | L_OUT | |
| | ○ | ○ | ○ | ○ | ○ | 1 |
| | E | D | C | B | A | |

**ISL99203**
**(20 BALL WLCSP)**
TOP VIEW

| | R_OUT | RIN | GND_CPK | SDA | SCL |
|---|---|---|---|---|---|
| 4 | ○ | ○ | ○ | ○ | ○ |
| | CN | VDD_CP | GND_CP | SWI+ | MO+ |
| 3 | ○ | ○ | ○ | ○ | ○ |
| | CP | VSS | MI- | VDD_P | GND_P |
| 2 | ○ | ○ | ○ | ○ | ○ |
| | L_OUT | LIN | MI+ | SWI- | MO- |
| 1 | ○ | ○ | ○ | ○ | ○ |
| | A | B | C | D | E |

# Pin Descriptions

| 20 BUMP CSP | PIN NAME | PIN DESCRIPTION |
|---|---|---|
| C4 | GND_CPK | Charge-Pump Ground |
| A1 | L_OUT | Left Headphone Out |
| B2 | VSS | Negative-Power Supply |
| A2 | CP | Charge-Pump Cap + |
| A3 | CN | Charge-Pump Cap - |
| A4 | R_OUT | Right Headphone Out |
| B4 | RIN | Right Input Channel |
| B3 | VDD_CP | Charge-Pump Power Supply |
| C3 | GND_CP | Charge-Pump Ground |
| D4 | SDA | $I^2C$ Data |
| D3 | SWI+ | Switch Input + |
| E4 | SCL | $I^2C$ Clock |
| E3 | MO+ | Mono O/P Positive |
| D2 | VDD_P | Power Supply |
| E2 | GND_P | Power Ground |
| E1 | MO- | Mono O/P Negative |
| D1 | SWI- | Switch Input - |
| C1 | MI+ | Mono Positive Input |
| C2 | MI- | Mono Negative Input |
| B1 | LIN | Left input Channel |

# Ordering Information

| PART NUMBER (Notes 1, 2, 3) | PART MARKING | TEMP RANGE (°C) | PACKAGE (Pb-free) | PKG. DWG. # |
|---|---|---|---|---|
| ISL99203IIZ-T | 203 | -40 to +85 | 20 Ball WLCSP | W4x5.20 |

NOTES:

1. Please refer to TB347 for details on reel specifications.

2. These Intersil Pb-free WLCSP and BGA packaged products employ special Pb-free material sets; molding compounds/die attach materials and SnAgCu - e1 solder ball terminals, which are RoHS compliant and compatible with both SnPb and Pb-free soldering operations. Intersil Pb-free WLCSP and BGA packaged products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J STD-020.

3. For Moisture Sensitivity Level (MSL), please see device information page for ISL99203. For more information on MSL please see tech brief TB363.

_intersil_

# Typical Application

intersil

# Block Diagram

*intersil*
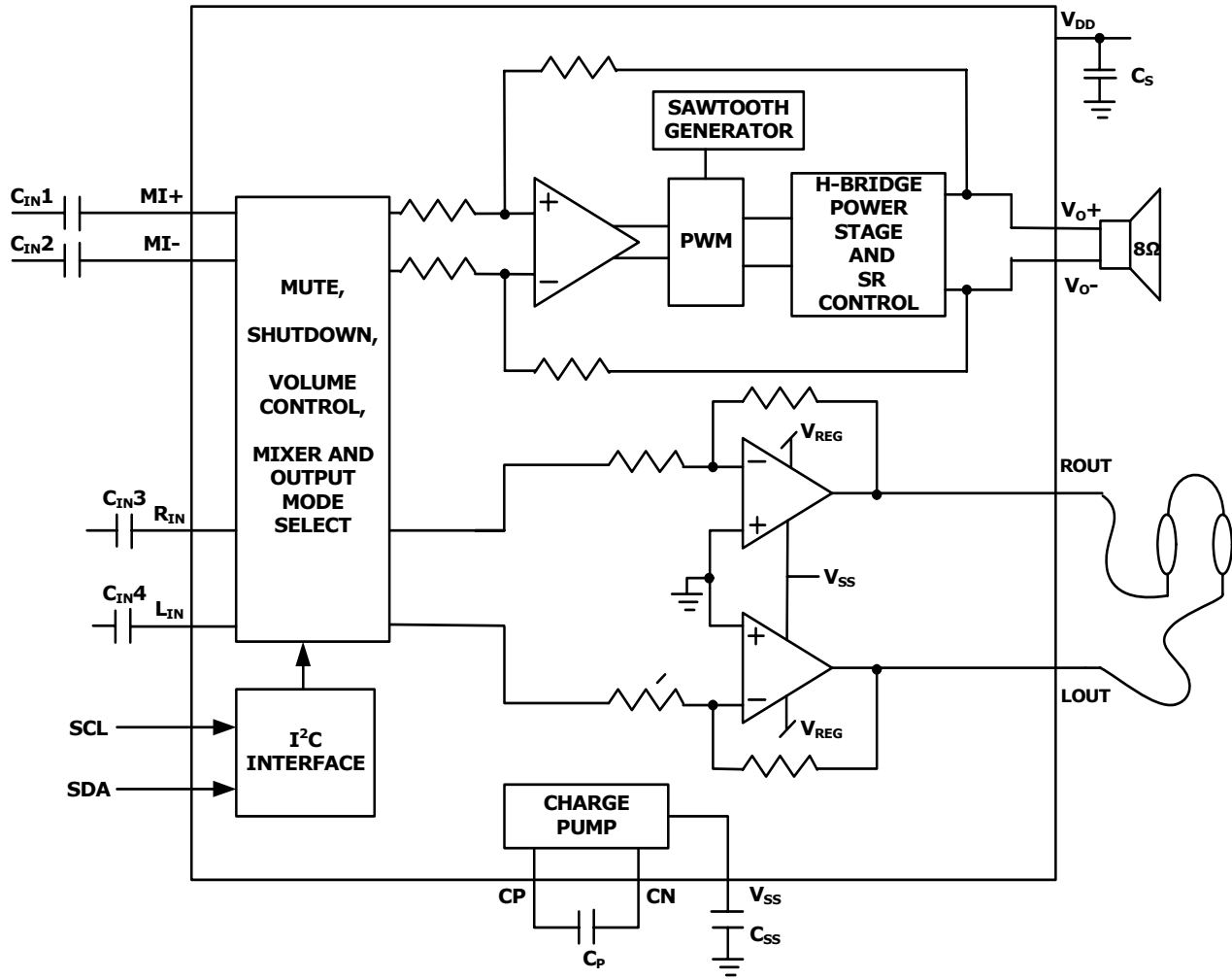
## Absolute Maximum Ratings (Reference to GND)

Supply Voltage . . . . . . . . . . . . . . . . . . . . . . . . . . -0.3V to 6V
LIN, RIN, MI+, MI -, SWI +, SWI - . . . . . -0.3V to $V_{DD}$+0.3V
ESD Ratings
   Human Body Model . . . . . . . . . . . . . . . . . . . . . . . . . 2kV
   Machine Model . . . . . . . . . . . . . . . . . . . . . . . . . . . 250V
   Charged Device Model . . . . . . . . . . . . . . . . . . . . 1500V

## Recommended Operating Conditions

Ambient Temperature Range . . . . . . . . . . . -40°C to +85°C
Operating Supply Voltage (VDD Pin). . . . . . . . . 2.4V to 5.5V

## Thermal Information

Thermal Resistance (Typical, Note 4)      $\theta_{JA}$ (°C/W)
   WLCSP Package . . . . . . . . . . . . . . . . . . . . .    71
Maximum Junction Temperature
(Plastic Package). . . . . . . . . . . . . . . . . . . . -65°C to +150°C
Maximum Storage Temperature Range . . . -65°C to +150°C
Dissipation Ratings
 Derating Factor
   20 Balls 4x5 Array WLCSP . . . . . . . . . . . . . . .10.1mW/°C
Power Rating $T_A$
   20 Balls 4x5 Array WLCSP
     +25°C . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . 1.76W
     +70°C . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . 1.12W
     +85°C. . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . .0.91W
Pb-Free Reflow Profile . . . . . . . . . . . . . . . . . . .see link below
       http://www.intersil.com/pbfree/Pb-FreeReflow.asp

*CAUTION: Do not operate at or near the maximum ratings listed for extended periods of time. Exposure to such conditions may adversely impact product reliability and result in failures not covered by warranty.*

NOTE:

4. $\theta_{JA}$ is measured with the component mounted on a high effective thermal conductivity test board in free air. See Tech Brief TB379 for details.

## Electrical Specifications

$V_{DD}$ = 3.6V. Typical Values Are Tested at $V_{DD}$ = 3.6V and the Ambient Temperature at +25°C. All Maximum and Minimum Values Are Established Under the Recommended Operating Supply Voltage Range and Ambient Temperature, Unless Otherwise Noted.
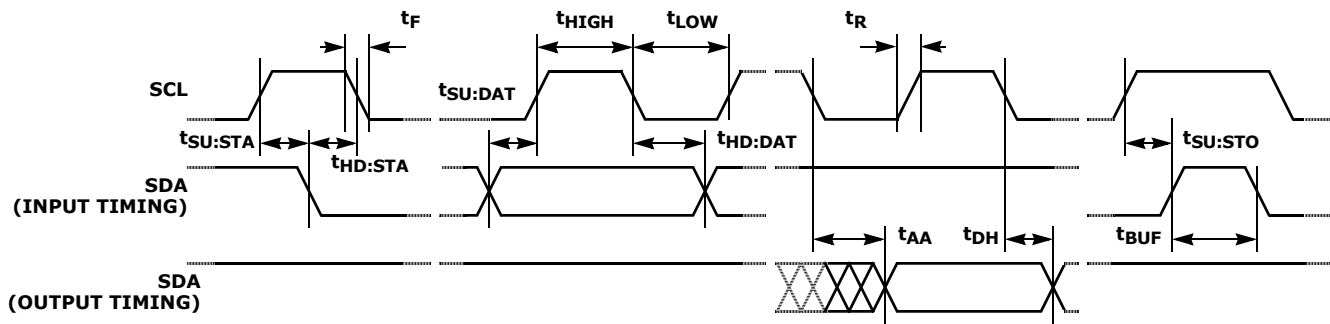
| PARAMETER | SYMBOL | TEST CONDITIONS | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|---|
| Output Power | $P_{OUT}$ | Mono, $R_L$ = 8Ω, THD = 1%, f = 1kHz, BTL, mode 1 | | 740 | | mW |
| | | Mono, $R_L$ = 8Ω, THD = 10%, f = 1kHz, BTL, mode 1 | | 925 | | mW |
| | | Headphone out $R_L$ = 32Ω, THD = 1%, f = 1kHz, mode 4 | | 47 | | mW |
| | | Headphone out $R_L$ = 32Ω, THD = 10%, f = 1kHz, mode 4 | | 62 | | mW |
| Total Harmonic Distortion | THD+N | A-weighted, grounded inputs and output referred | | | | |
| | | Mono, $R_L$ = 8Ω, f = 1kHz, BTL, $P_{OUT}$ = 500mW, mode 1 | | 0.05 | | % |
| | | Headphone out, $R_L$ = 32Ω, f = 1kHz, $P_{OUT}$ = 50mW, mode 4 | | 0.01 | | % |
| Output Offset Voltage | $V_{OS}$ | $V_{IN}$ = 0V, mode 1, Mono | | 2 | | mV |
| | | $V_{IN}$ = 0V, mode 4 Headphones | | 0.2 | | mV |
| Quiescent Current | $I_{qq}$ | O/P modes 2, 4, 6, $V_{IN}$ = 0V, no load | | 4.5 | 6 | mA |
| | | O/P modes 1, 3, 5, 7, $V_{IN}$ = 0V, no load | | 6.5 | 8 | mA |
| Shutdown Current | $I_{SD}$ | Output mode 0 | | 0.01 | 0.5 | µA |
| Digital Volume Control Range | | Max Gain | | 18 | | dB |
| HP Mute Attenuation | | | | 96 | | dB |
| Input Impedance (Mono and HP) | | | | 12.5 | | kΩ |
| Average Switching Frequency | $f_{SW}$ | Output mode 1. $V_{DD}$ = 3.6V | 250 | 325 | 400 | kHZ |
| Power Supply Rejection Ratio | PSRR-Mono | $V_{RIPPLE}$ = 200mV, f = 217Hz, $R_L$ = 8Ω, all inputs at GND, O/P mode 1 | | 75 | | dB |
| | PSRR-HP | $V_{RIPPLE}$ = 200mV, f = 217Hz, $R_L$ = 32Ω, all inputs at GND, O/P mode 4 | | 85 | | dB |
| Common Mode Rejection Ratio | CMRR | f = 217Hz, $V_{cm}$ = 1$V_{P-P}$, 0dB, mode 1, $R_L$ = 8Ω | | 61 | | dB |
| | | f = 217Hz, $V_{cm}$ = 1$V_{P-P}$, 0dB, mode 2, $R_L$ = 32Ω | | 66 | | dB |

**Electrical Specifications**  $V_{DD}$ = 3.6V. Typical Values Are Tested at $V_{DD}$ = 3.6V and the Ambient Temperature at +25°C. All Maximum and Minimum Values Are Established Under the Recommended Operating Supply Voltage Range and Ambient Temperature, Unless Otherwise Noted. **(Continued)**

| PARAMETER | SYMBOL | TEST CONDITIONS | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|---|
| **PROTECTION** | | | | | | |
| Thermal Shutdown | | | | 145 | | °C |
| Thermal Shutdown Hysteresis | | | | 30 | | °C |
| Overcurrent Shutdown | | Mono | | 1.3 | | A |
| | | HP | | 200 | | mA |
| Undervoltage Shutdown | | | | | 2.4 | V |
| Wake-up Time from Shutdown | $t_{WU}$ | | | 3.5 | | ms |
| **NOISE PERFORMANCE** | | | | | | |
| Output Voltage Noise | $e_n$ | Mono, mode 1 | | 33 | | µV |
| | | HP, mode 4, 7 | | 12 | | µV |

**Electrical Specifications**  $V_{DD}$ = 5V. Typical Values Are Tested at $V_{DD}$ = 5V and the Ambient Temperature at +25°C. All Maximum and Minimum Values Are Established Under the Recommended Operating Supply Voltage Range and Ambient Temperature, Unless Otherwise Noted.

| PARAMETER | SYMBOL | TEST CONDITIONS | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|---|
| Output Power | $P_{OUT}$ | Mono, $R_L$ = 8Ω, THD = 1%, f = 1kHz, BTL, Mode 1 | | 1 | | W |
| | | Mono, $R_L$ = 8Ω, THD = 10%, f = 1kHz, BTL, Mode 1 | | 1.375 | | W |
| | | Headphone out $R_L$=32Ω, THD = 1%, f = 1kHz, SE, Mode 4 | | 47 | | mW |
| | | Headphone out $R_L$=32Ω, THD = 10%, f = 1kHz, SE, Mode 4 | | 62 | | mW |
| Total Harmonic Distortion | THD+N | A-weighted, grounded inputs and output referred | | | | |
| | | Mono, $R_L$ = 8Ω, f = 1kHz, BTL, $P_{OUT}$ = 500mW, Mode 1 | | 0.05 | | % |
| | | Headphone out, $R_L$ = 32Ω, f = 1kHz, $P_{OUT}$ = 50mW, Mode 4 | | 0.01 | | % |
| Output Offset Voltage | $V_{OS}$ | $V_{IN}$ = 0V, mode 1, Mono | | 2 | | mV |
| | | $V_{IN}$ = 0V, mode 4 Headphones | | 0.2 | | mV |
| Quiescent Current | $I_{qq}$ | O/P modes 4 | | 5 | | mA |
| | | O/P modes 1 | | 5.5 | | mA |
| Shutdown Current | $I_{SD}$ | Output mode 0 | | 0.01 | | µA |
| Digital Volume Control Range | | Max Gain | | 18 | | dB |
| HP Mute Attenuation | | | | 96 | | dB |
| Input Impedance (Mono and HP) | | | | 12.5 | | kΩ |
| Power Supply Rejection Ratio | PSRR-Mono | $V_{Ripple}$ = 200mV, f = 217Hz, $R_L$ = 8Ω, all inputs at GND, O/P mode 1 | | 75 | | dB |
| | PSRR-HP | $V_{Ripple}$ = 200mV, f = 217Hz, $R_L$ = 32Ω, all inputs at GND, O/P mode 4, 7 | | 85 | | dB |
| Common Mode rejection Ratio | CMRR | f = 217Hz, $V_{cm}$ = 1V$_{P-P}$, 0dB, mode 1, $R_L$ = 8Ω | | 61 | | dB |
| | | f = 217Hz, $V_{cm}$ = 1V$_{P-P}$, 0dB, mode 2, $R_L$ = 32Ω | | 66 | | dB |

*intersil*

**Electrical Specifications**  $V_{DD}$ = 5V. Typical Values Are Tested at $V_{DD}$ = 5V and the Ambient Temperature at +25°C. All Maximum and Minimum Values Are Established Under the Recommended Operating Supply Voltage Range and Ambient Temperature, Unless Otherwise Noted. **(Continued)**

| PARAMETER | SYMBOL | TEST CONDITIONS | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|---|
| **PROTECTION** | | | | | | |
| Thermal Shutdown | | | | 145 | | °C |
| Thermal Shutdown Hysteresis | | | | 30 | | °C |
| Overcurrent Shutdown | | Mono | | 1.3 | | A |
| | | HP | | 200 | | mA |
| Undervoltage Shutdown | | | | | 2.4 | V |
| Wake-up Time from Shutdown | $t_{WU}$ | | | 3.5 | | ms |
| **NOISE PERFORMANCE** | | | | | | |
| Output Voltage Noise | $e_n$ | Mono, Mode 1 | | 33 | | µV |
| | | HP, Mode 4, 7 | | 12 | | µV |

# SDA vs SCL Timing



#### TABLE 1. CHIP ADDRESS

| | A7 | A6 | A5 | A4 | A3 | A2 | A1 | A0 |
|---|---|---|---|---|---|---|---|---|
| Chip Address | 1 | 1 | 1 | 1 | 1 | 0 | Pin Controlled | 0 |
| ID_ENB = 0 | 1 | 1 | 1 | 1 | 1 | 0 | 0 | 0 |
| ID_ENB = 1 | 1 | 1 | 1 | 1 | 1 | 0 | 1 | 0 |

#### TABLE 2. CONTROL REGISTERS

| | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|---|---|---|---|---|---|---|---|---|
| Mode Control | 0 | 0 | 0/1 | 0 | X/MC3 | MC2 | MC1 | MC0 |
| Boost Control | 0 | 1 | 1 | X | Amp BYP | GBM | GBHPL | GBHPR |
| Mono Volume Control | 1 | 0 | 0 | MVC4 | MVC3 | MVC2 | MVC1 | MVC0 |
| Extended Volume Control | 1 | 0 | 1 | 0 | 0 | RVC5 | LVC5 | MVC5 |
| Left Volume Control | 1 | 1 | 0 | LVC4 | LVC3 | LVC2 | LVC1 | LVC0 |
| Right Volume Control | 1 | 1 | 1 | RVC4 | RVC3 | RVC2 | RVC1 | RVC0 |

NOTE: GBM: Gain Boost on Mono Speaker; 0 = no boost, 1 = 3dB
      GBHP: Gain Boost on Headphone; 0 = no boost, 1 = 3dB
      Amp Bypass: 0 is no bypass (Switch OFF); 1 is bypass (Switch ON)

### TABLE 3. OUTPUT MODES

| OUTPUT MODE | MC3 | MC2 | MC1 | MC0 | SPEAKER OUTPUT | RIGHT HP OUTPUT | LEFT HP OUTPUT |
|---|---|---|---|---|---|---|---|
| 0 | 0 | 0 | 0 | 0 | SD | SD | SD |
| 1 | 0 | 0 | 0 | 1 | $G_M$ x M | SD | SD |
| 2 | 0 | 0 | 1 | 0 | SD | $G_M$ x M/2 | $G_M$ x M/2 |
| 3 | 0 | 0 | 1 | 1 | 2 x ($G_L$ x L + $G_R$ x R) | SD | SD |
| 4 | 0 | 1 | 0 | 0 | SD | $G_R$ x R | $G_L$ x L |
| 5 | 0 | 1 | 0 | 1 | 2 x ($G_L$ x L + $G_R$ x R) + $G_M$ x M | SD | SD |
| 6 | 0 | 1 | 1 | 0 | SD | $G_M$ x M/2 + $G_R$ x R | $G_M$ x M/2 + $G_L$ x L |
| 7 | 0 | 1 | 1 | 1 | 2 x ($G_L$ x L + $G_R$ x R) | $G_R$ x R | $G_L$ x L |
| 10 | 1 | 0 | 1 | 0 | 2 x ($G_L$ x L + $G_R$ x R) | $G_M$ x M/2 | $G_M$ x M/2 |
| 14 | 1 | 1 | 1 | 0 | 2 x ($G_L$ x L + $G_R$ x R) | $G_M$ x M/2 + $G_R$ x R | $G_M$ x M/2 + $G_L$ x L |

NOTE:
Power On Default Mode    0 0 0 0
M = Mono, Phone in
R = $R_{IN}$
L = $L_{IN}$
SD = Shutdown
GM = Mono Volume Control gain
GR = Right HP Volume Control Gain
GL = Left HP Volume Control gain

### TABLE 4. VOLUME CONTROL

| VOLUME STEP | VC5 | VC4 | VC3 | VC2 | VC1 | VC0 | GAIN (dB) |
|---|---|---|---|---|---|---|---|
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | -82 |
| 1 | 0 | 0 | 0 | 0 | 0 | 1 | -76 |
| 2 | 0 | 0 | 0 | 0 | 1 | 0 | -70 |
| 3 | 0 | 0 | 0 | 0 | 1 | 1 | -64.5 |
| 4 | 0 | 0 | 0 | 1 | 0 | 0 | -58.5 |
| 5 | 0 | 0 | 0 | 1 | 0 | 1 | -52 |
| 6 | 0 | 0 | 0 | 1 | 1 | 0 | -46.5 |
| 7 | 0 | 0 | 0 | 1 | 1 | 1 | -40.5 |
| 8 | 0 | 0 | 1 | 0 | 0 | 0 | -34.5 |
| 9 | 0 | 0 | 1 | 0 | 0 | 1 | -30 |
| 10 | 0 | 0 | 1 | 0 | 1 | 0 | -26.5 |
| 11 | 0 | 0 | 1 | 0 | 1 | 1 | -24 |
| 12 | 0 | 0 | 1 | 1 | 0 | 0 | -21 |
| 13 | 0 | 0 | 1 | 1 | 0 | 1 | -18 |
| 14 | 0 | 0 | 1 | 1 | 1 | 0 | -15 |
| 15 | 0 | 0 | 0 | 1 | 1 | 1 | -13.5 |
| 16 | 0 | 1 | 0 | 0 | 0 | 0 | -11.5 |
| 17 | 0 | 1 | 0 | 0 | 0 | 1 | -10 |
| 18 | 0 | 1 | 0 | 0 | 1 | 0 | -8.5 |
| 19 | 0 | 1 | 0 | 0 | 1 | 1 | -7 |
| 20 | 0 | 1 | 0 | 1 | 0 | 0 | -6 |

### TABLE 4. VOLUME CONTROL (Continued)

| VOLUME STEP | VC5 | VC4 | VC3 | VC2 | VC1 | VC0 | GAIN (dB) |
|---|---|---|---|---|---|---|---|
| 21 | 0 | 1 | 0 | 1 | 0 | 1 | -4.5 |
| 22 | 0 | 1 | 0 | 1 | 1 | 0 | -3 |
| 23 | 0 | 1 | 0 | 1 | 1 | 1 | -1.5 |
| 24 | 0 | 1 | 1 | 0 | 0 | 0 | 0 |
| 25 | 0 | 1 | 1 | 0 | 0 | 1 | 1.5 |
| 26 | 0 | 1 | 1 | 0 | 1 | 0 | 3 |
| 27 | 0 | 1 | 1 | 0 | 1 | 1 | 4.5 |
| 28 | 0 | 1 | 1 | 1 | 0 | 0 | 6 |
| 29 | 0 | 1 | 1 | 1 | 0 | 1 | 7.5 |
| 30 | 0 | 1 | 1 | 1 | 1 | 0 | 9 |
| 31 | 0 | 0 | 1 | 1 | 1 | 1 | 10.5 |
| 32 | 1 | 0 | 0 | 0 | 0 | 0 | 12 |
| 33 | 1 | 0 | 0 | 0 | 0 | 1 | 12.75 |
| 34 | 1 | 0 | 0 | 0 | 1 | 0 | 13.5 |
| 35 | 1 | 0 | 0 | 0 | 1 | 1 | 14.25 |
| 36 | 1 | 0 | 0 | 1 | 0 | 0 | 15 |
| 37 | 1 | 0 | 0 | 1 | 0 | 1 | 15.75 |
| 38 | 1 | 0 | 0 | 1 | 1 | 0 | 16.5 |
| 39 | 1 | 0 | 0 | 1 | 1 | 1 | 17.25 |
| 40 | 1 | 0 | 1 | 0 | 0 | 0 | 18 |

# Typical Performance Characteristics
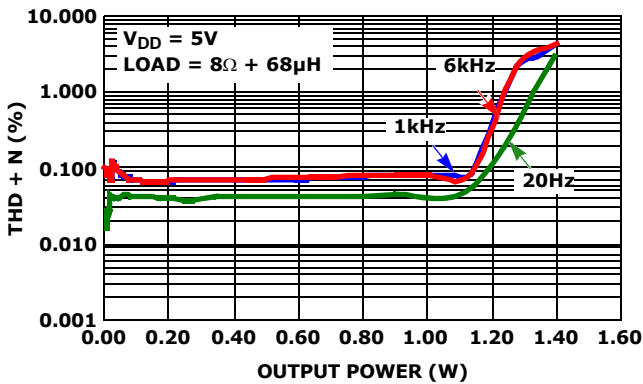


FIGURE 1. TOTAL HARMORNIC DISTORTION PLUS NOISE vs POWER (MONO)
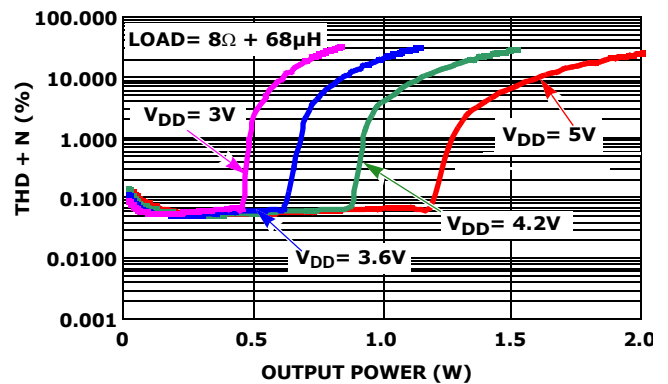


FIGURE 2. TOTAL HARMORNIC DISTORTION PLUS NOISE vs POWER (MONO)

# Typical Performance Characteristics (Continued)
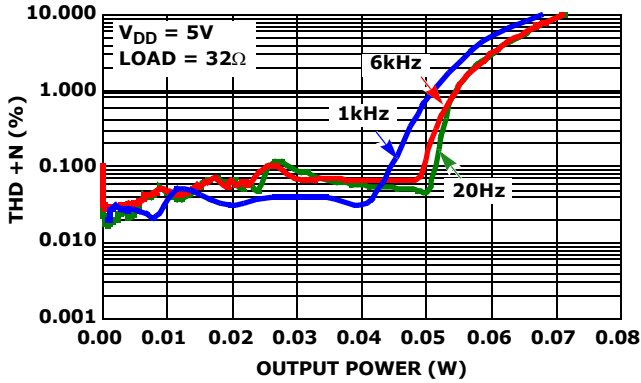


FIGURE 3. TOTAL HARMORNIC DISTORTION PLUS
NOISE vs POWER (HEADPHONE)
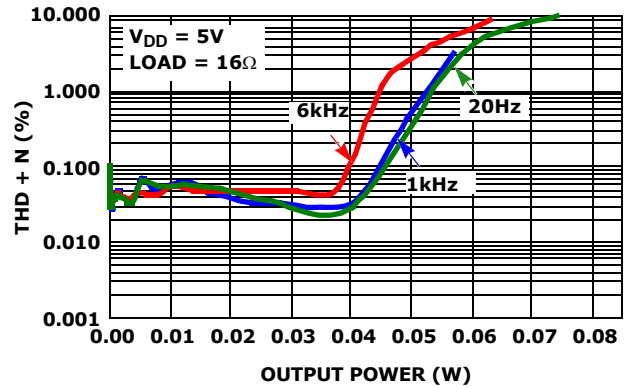


FIGURE 4. TOTAL HARMORNIC DISTORTION PLUS
NOISE vs POWER (HEADPHONE)
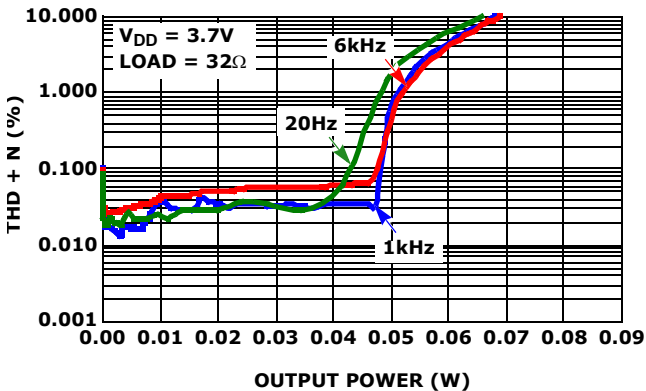


FIGURE 5. TOTAL HARMORNIC DISTORTION PLUS
NOISE vs POWER (HEADPHONE)
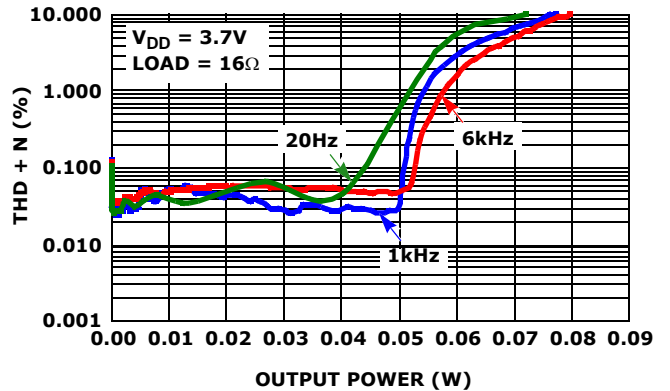


FIGURE 6. TOTAL HARMORNIC DISTORTION PLUS
NOISE vs POWER (HEADPHONE)
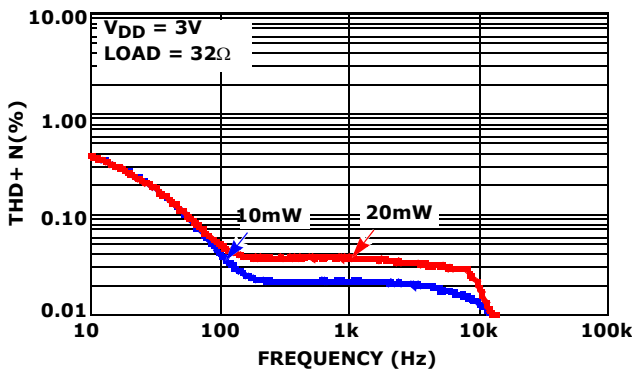


FIGURE 7. TOTAL HARMORNIC DISTORTION PLUS
NOISE vs FREQUENCY (HEADPHONE)
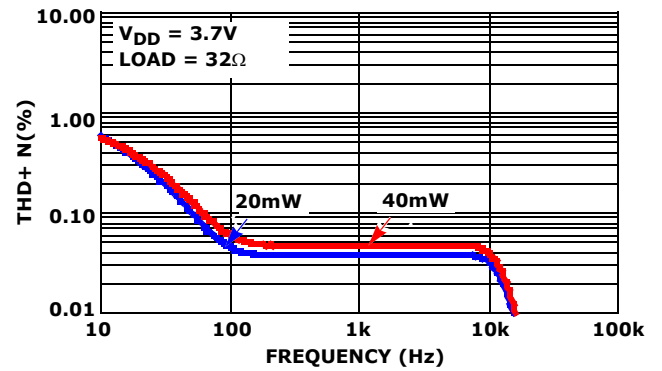


FIGURE 8. TOTAL HARMORNIC DISTORTION PLUS
NOISE vs FREQUENCY (HEADPHONE)

# Typical Performance Characteristics (Continued)
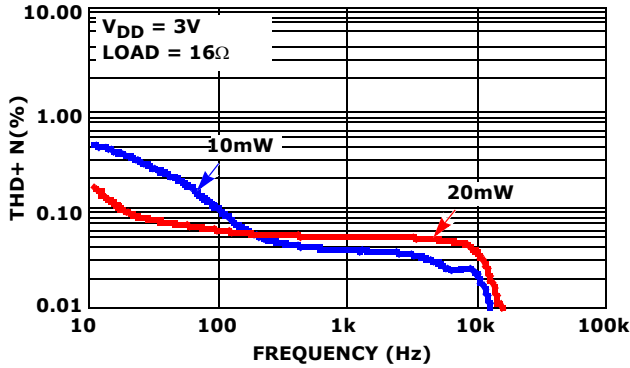


FIGURE 9. TOTAL HARMORNIC DISTORTION PLUS
NOISE vs FREQUENCY (HEADPHONE)
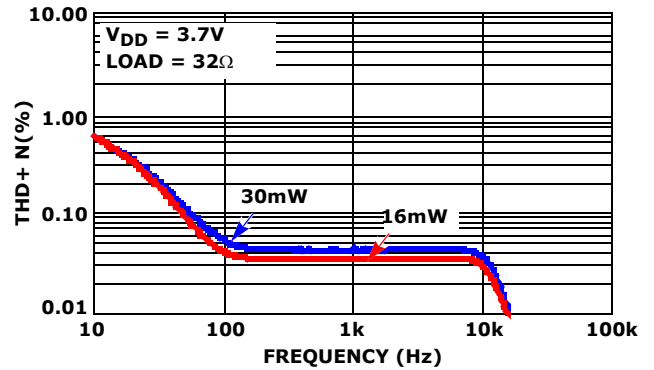


FIGURE 10. TOTAL HARMORNIC DISTORTION PLUS
NOISE vs FREQUENCY (HEADPHONE)
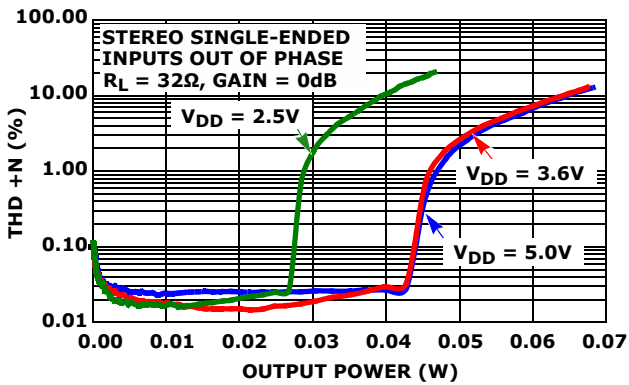


FIGURE 11. TOTAL HARMONIC DISTORTION + NOISE
vs OUTPUT POWER
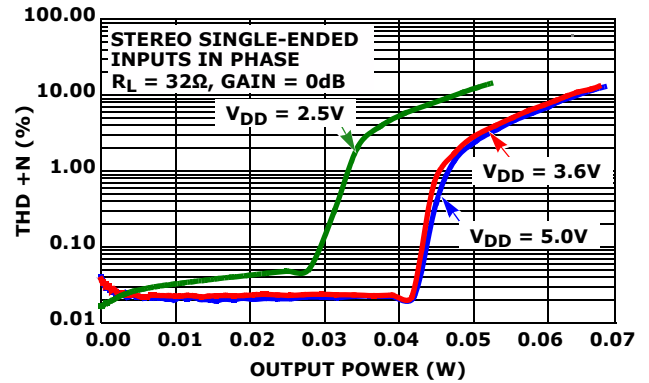


FIGURE 12. TOTAL HARMONIC DISTORTION + NOISE
(HP) vs POWER
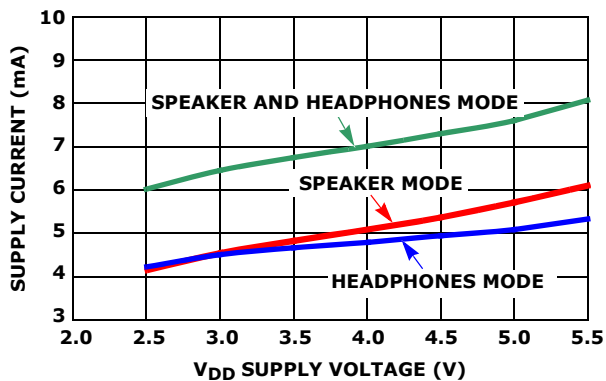


FIGURE 13. SUPPLY CURRENT vs SUPPLY VOLTAGE
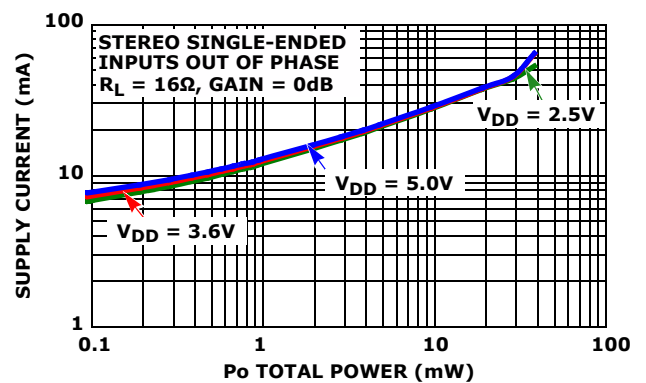


FIGURE 14. SUPPLY CURRENT (HEADPHONES) vs
TOTAL OUTPUT POWER

# Typical Performance Characteristics (Continued)
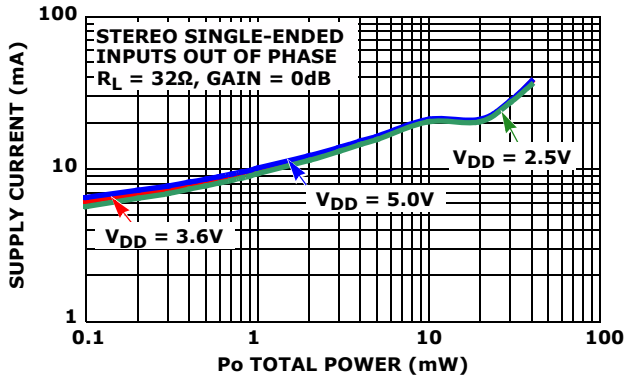


FIGURE 15. SUPPLY CURRENT (HEADPHONES) vs
TOTAL OUTPUT POWER
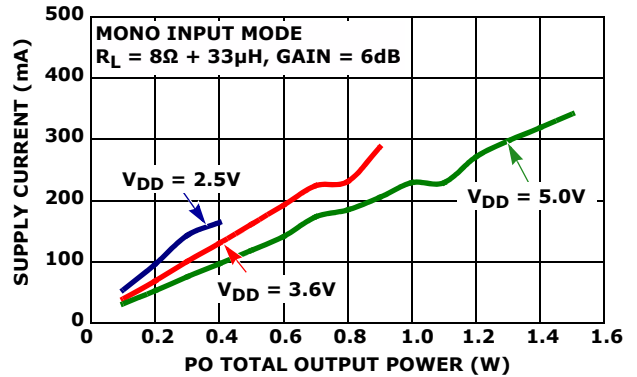


FIGURE 16. TOTAL POWER DISSIPATION (SPEAKER
MODE) vs TOTAL OUTPUT POWER
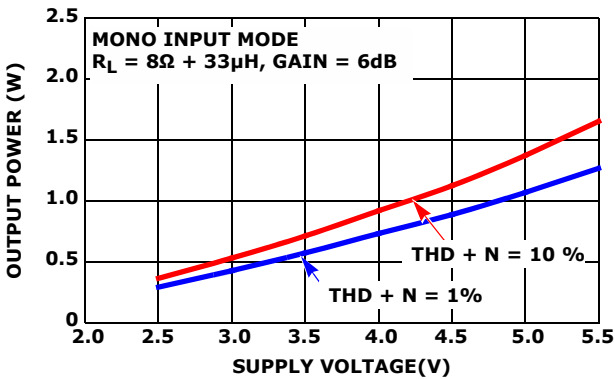


FIGURE 17. OUTPUT POWER (SPEAKER) vs SUPPLY
VOLTAGE
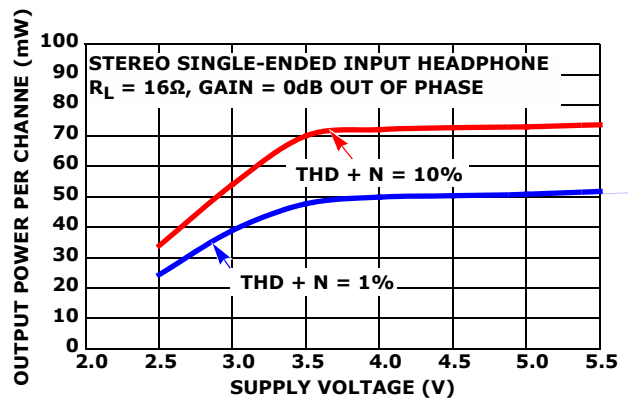


FIGURE 18. OUTPUT POWER PER CHANNEL
(HEADPHONE) vs SUPPLY VOLTAGE
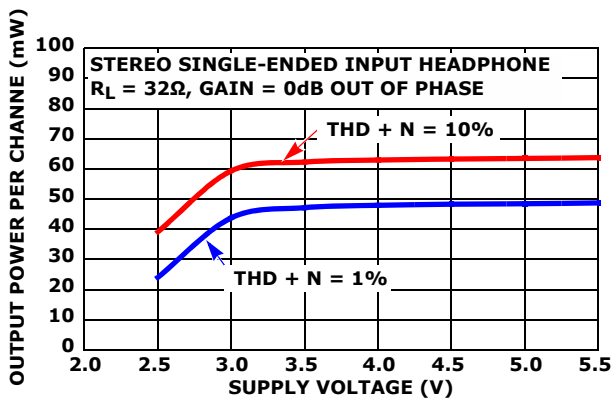


FIGURE 19. OUTPUT POWER PER CHANNEL
(HEADPHONE) vs SUPPLY VOLTAGE
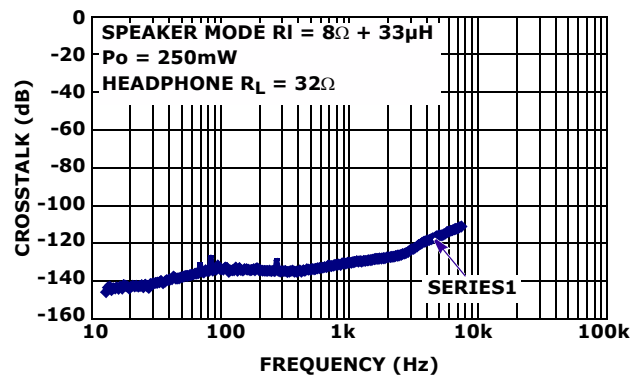


FIGURE 20. SPEAKER TO HEADPHONE CROSSTALK vs
FREQUENCY

# Typical Performance Characteristics (Continued)
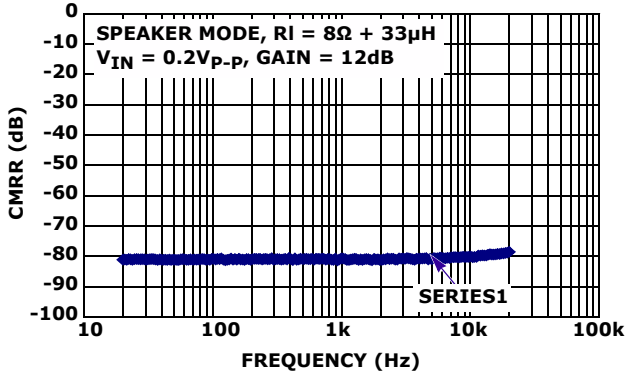


FIGURE 21. COMMON-MODE REJECTION RATIO vs FREQUENCY
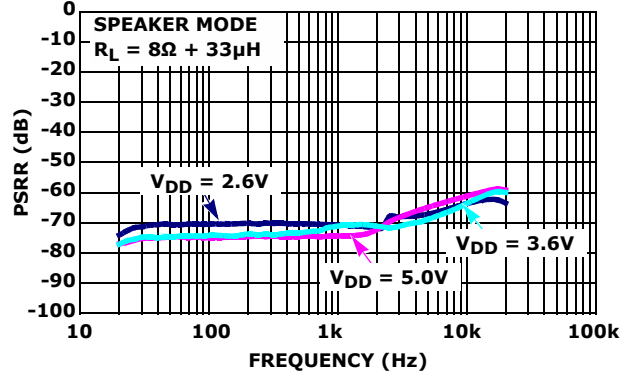


FIGURE 22. POWER SUPPLY REJECTION RATIO (SPEAKER) vs FREQUENCY
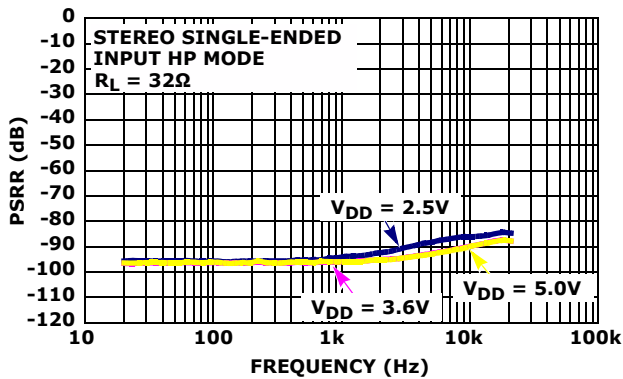


FIGURE 23. POWER SUPPLY REJECTION RATIO (HEADPHONES) vs FREQUENCY
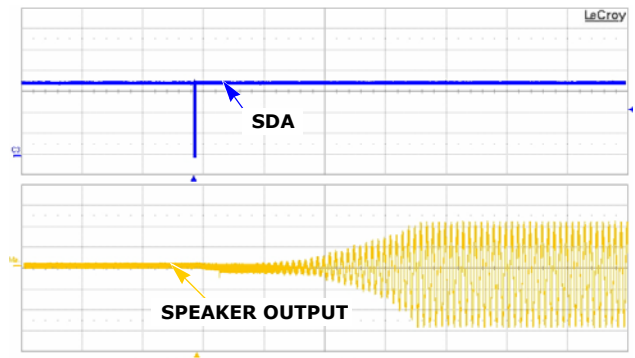


FIGURE 24. SPEAKER OUTPUT - START-UP
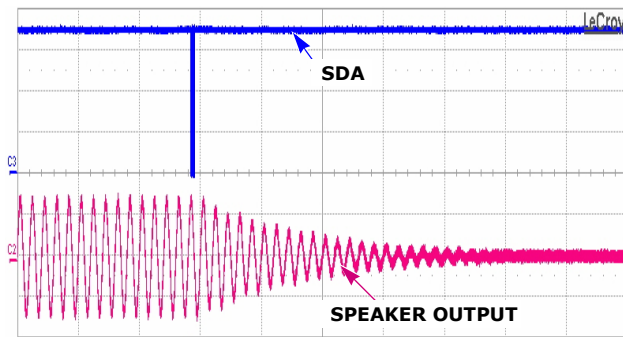


FIGURE 25. SPEAKER OUTPUT - SHUTDOWN
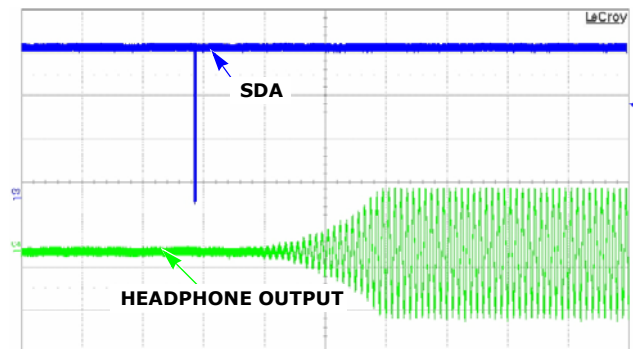


FIGURE 26. HEADPHONE OUTPUT - START-UP
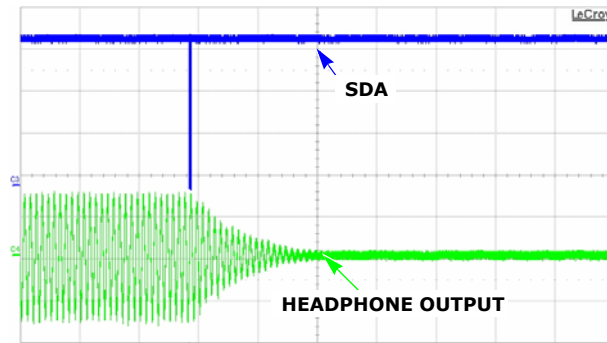
## Typical Performance Characteristics (Continued)



**FIGURE 27. HEADPHONE OUTPUT - SHUTDOWN**

# Theory of Operation

The ISL99203 supports an I$^2$C bidirectional bus oriented protocol. The protocol defines any device that sends data onto the bus as a transmitter and the receiving device as the receiver. The device controlling the transfer is a master and the device being controlled is the slave. The master always initiates data transfers and provides the clock for both transmit and receive operations. Therefore, the ISL99203 operates as a slave device in all applications.

All communication over the I$^2$C interface is conducted by sending the MSB of each byte of data first.

## Protocol Conventions

Data states on the SDA line must change only during SCL LOW periods. SDA state changes during SCL HIGH are reserved for indicating START and STOP conditions (see Figure 28). On power-up of the ISL99203, the SDA pin is in the input mode.

All I$^2$C interface operations must begin with a START condition, which is a HIGH to LOW transition of SDA while SCL is HIGH. The ISL99203 continuously monitors the SDA and SCL lines for the START condition and does not respond to any command until this condition is met (see Figure 29). A START condition is ignored during the power-up of the device.

All I$^2$C interface operations must be terminated by a STOP condition, which is a LOW to HIGH transition of SDA while SCL is HIGH (see Figure 28). A STOP condition at the end of a read operation, or at the end of a write operation places the device in its standby mode.

An ACK, Acknowledge, is a software convention used to indicate a successful data transfer. The transmitting device, either master or slave, releases the SDA bus after transmitting eight bits. During the ninth clock cycle, the receiver pulls the SDA line LOW to acknowledge the reception of the eight bits of data (see Figure 29).

The ISL99203 responds with an ACK after recognition of a START condition followed by a valid Identification Byte, and once again after successful receipt of an Address Byte. The ISL99203 also responds with an ACK after receiving a Data Byte of a write operation. The master must respond with an ACK after receiving a Data Byte of a read operation.
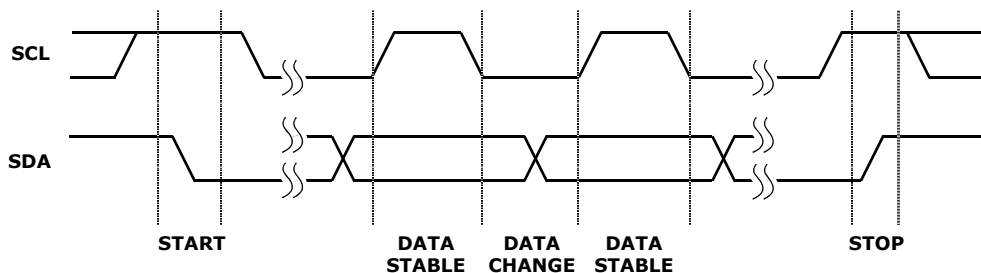


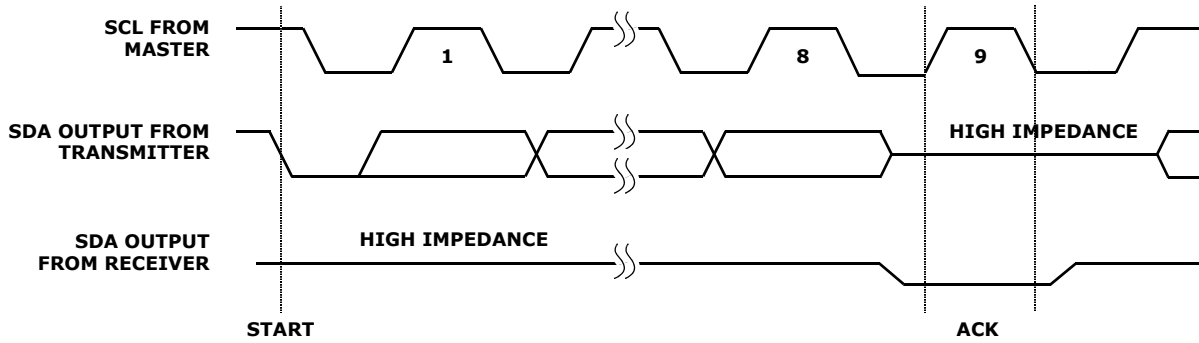**FIGURE 28. VALID DATA CHANGES, START, AND STOP CONDITIONS**

**FIGURE 29. ACKNOWLEDGE RESPONSE FROM RECEIVER**

# Revision History

The revision history provided is for informational purposes only and is believed to be accurate, but not warranted. Please go to web to make sure you have the latest Rev.

| DATE | REVISION | CHANGE |
|---|---|---|
| 6/21/10 | FN7547.1 | Added key performance graphics to page 1.<br>Moved Pin Configurations, Pin Descriptions and ordering information to follow standards. |
| 12/17/09 | FN7547.0 | Initial release. |

# Products

Intersil Corporation is a leader in the design and manufacture of high-performance analog semiconductors. The Company's products address some of the industry's fastest growing markets, such as, flat panel displays, cell phones, handheld products, and notebooks. Intersil's product families address power management and analog signal processing functions.  Go to www.intersil.com/products  for a complete list of Intersil product families.

*For a complete listing of Applications, Related Documentation and Related Parts, please see the respective device information page on intersil.com: ISL99203

To report errors or suggestions for this datasheet, please go to www.intersil.com/askourstaff

FITs are available from our website at http://rel.intersil.com/reports/search.php

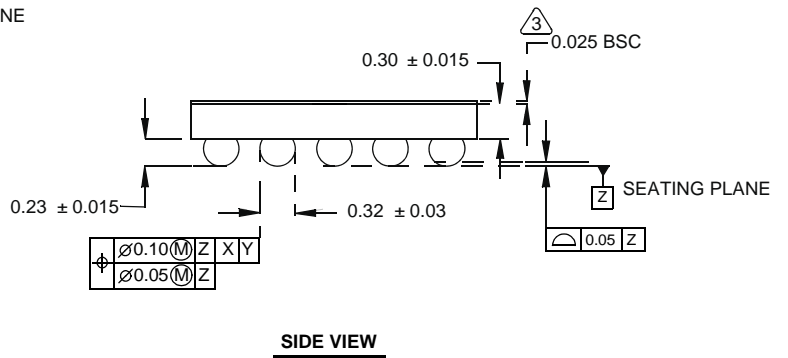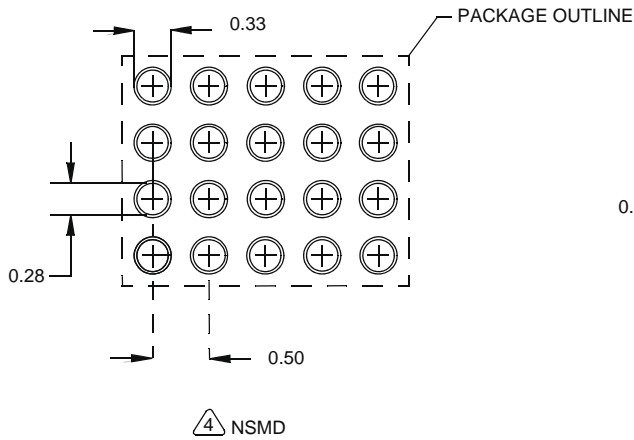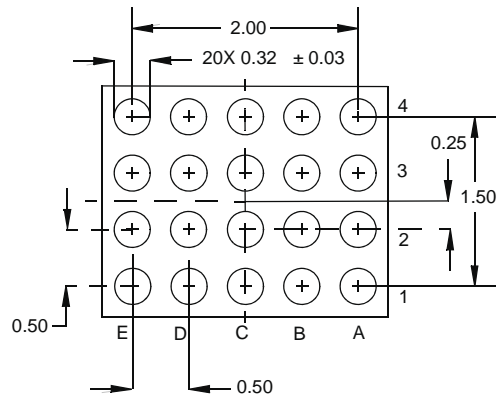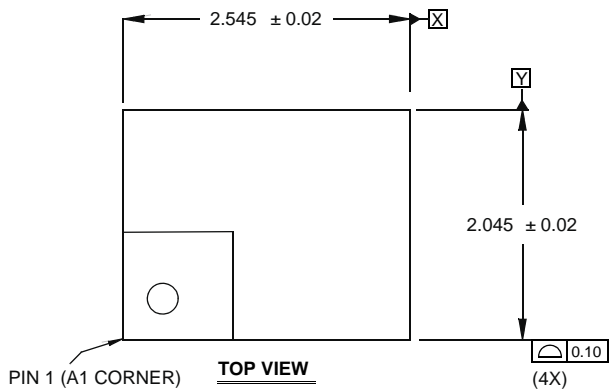For additional products, see www.intersil.com/product_tree

Intersil products are manufactured, assembled and tested utilizing ISO9000 quality systems as noted in the quality certifications found at www.intersil.com/design/quality

For information regarding Intersil Corporation and its products, see www.intersil.com

# Package Outline Drawing
## W4x5.20
**4x5 Array 20 Ball Wafer Level Chip Scale Package (WLCSP)**
**Rev 1 8/09**



2.545 ± 0.02 ⊠X

Ⓨ

2.045 ± 0.02

PIN 1 (A1 CORNER)   **TOP VIEW**   ⌓ 0.10

(4X)

2.00

20X 0.32 ± 0.03

4

0.25

3

1.50

2

0.50   1

E   D   C   B   A

0.50

**BOTTOM VIEW**

0.33   PACKAGE OUTLINE

0.28

0.50

△4 NSMD

**TYPICAL RECOMMENDED LAND PATTERN**

△3 0.025 BSC

0.30 ± 0.015

0.23 ± 0.015

0.32 ± 0.03

SEATING PLANE

Z   ⌓ 0.05 Z

⌖ | Ø0.10Ⓜ | Z | X | Y
⌖ | Ø0.05Ⓜ | Z

**SIDE VIEW**

NOTES:

1. Dimensions are in millimeters.

2. Dimensioning and tolerancing conform to AMSE Y14.5m-1994, and JESD 95-1 SPP-10.

△3. Back side coat 0.25mm thick applied to CSP package top.

△4. NSMD refers to non-solder mask defined pad design per Intersil tech brief www.intersil.com/data/tb/TB451.pdf