PIC18F2420/2520/4420/4520 Rev. B3 Silicon Errata

The PIC18F2420/2520/4420/4520 Rev. B3 parts you have received conform functionally to the Device Data Sheet (DS39631**E**), except for the anomalies described below. Any Data Sheet Clarification issues related to the PIC18F2420/2520/4420/4520 will be reported in a separate Data Sheet errata. Please check the Microchip web site for any existing issues.

The following silicon errata apply only to PIC18F2420/2520/4420/4520 devices with these Device/Revision IDs:

Part Number	Device ID	Revision ID
PIC18F2420	0001 0001 010	0 0110
PIC18F2520	0001 0001 000	0 0110
PIC18F4420	0001 0000 110	0 0110
PIC18F4520	0001 0000 100	0 0110

The Device IDs (DEVID1 and DEVID2) are located at addresses 3FFFFEh:3FFFFFh in the device's configuration space. They are shown in hexadecimal in the format "DEVID2 DEVID1".

All of the issues listed here will be addressed in future revisions of the PIC18F2420/2520/4420/4520 silicon.

1. Module: MSSP

In SPI Slave mode with slave select enabled (SSPM<3:0> = 0100), the minimum time between the falling edge of the $\overline{SS}$ pin and first SCK edge is greater than specified in parameter 70 in Table 26-16 and Table 26-17 of the above referenced data sheet.

The updated specification is shown in bold in Table 1.

Work around

None.

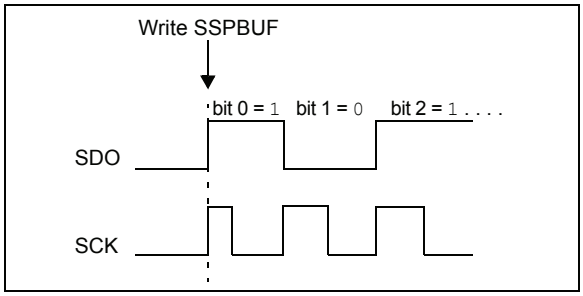
Date Codes that pertain to this issue:

All engineering and production devices.

2. Module: MSSP (SPI Mode)

When the SPI is using Timer2/2 as the clock source, a shorter than expected SCK pulse may occur on the first bit of the transmitted/received data (Figure 1).

FIGURE 1: SCK PULSE VARIATION USING TIMER2/2



Work around

To avoid producing the short pulse, turn off Timer2 and clear the TMR2 register, load the SSPBUF with the data to transmit and then turn Timer2 back on. Refer to Example 1 for sample code.

EXAMPLE 1: AVOIDING THE INITIAL SHORT SCK PULSE

```
LOOP BTFSSSSPSTAT, BF    ;Data received?
                         ;(Xmit complete?)
    BRA LOOP             ;No
    MOVFSSPBUF, W        ;W = SSPBUF
    MOVWFRXDATA          ;Save in user RAM
    MOVFTXDATA, W  ;W = TXDATA
    BCF T2CON, TMR2ON;Timer2 off
    CLRFTMR2             ;Clear Timer2
    MOVWFSSPBUF          ;Xmit New data
    BSF T2CON, TMR2ON;Timer2 on
```

Date Codes that pertain to this issue:

All engineering and production devices.

TABLE 1: EXAMPLE SPI MODE REQUIREMENTS (SLAVE MODE TIMING)

Param No.	Symbol	Characteristic	Min	Max	Units	Conditions
70	TssL2scH, TssL2scL	$\overline{SS}$ ↓ to SCK ↓ or SCK ↑ Input	**3 TCY**	—	ns	

3. Module: Enhanced Universal Synchronous Receiver Transmitter (EUSART)

One bit has been added to the BAUDCON register and one bit has been renamed. The added bit is RXDTP and is in the location, BAUDCON<5>. The renamed bit is the TXCKP bit (BAUDCON<4>), which had been named SCKP.

The TXCKP (BAUDCON<4>) and RXDTP (BAUDCON<5>) bits enable the TX and RX signals to be inverted (polarity reversed).

Register 18-3, on page 194, will be changed as shown.

Work around

None required.

Date Codes that pertain to this issue:

All engineering and production devices.

REGISTER 18-3: BAUDCON: BAUD RATE CONTROL REGISTER

R/W-0	R-1	R/W-0	R/W-0	R/W-0	U-0	R/W-0	R/W-0
ABDOVF	RCIDL	RXDTP	TXCKP	BRG16	—	WUE	ABDEN
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 7 **ABDOVF**: Auto-Baud Acquisition Rollover Status bit
1 = A BRG rollover has occurred during Auto-Baud Rate Detect mode (must be cleared in software)
0 = No BRG rollover has occurred

bit 6 **RCIDL**: Receive Operation Idle Status bit
1 = Receive operation is Idle
0 = Receive operation is Active

bit 5 **RXDTP**: Receive Data Polarity Select bit
Asynchronous mode:
1 = Receive data (RX) is inverted. Idle state is a low level.
0 = No inversion of receive data (RX). Idle state is a high level.
Synchronous mode:
1 = Data (DT) is inverted. Idle state is a low level.
0 = No inversion of data (DT). Idle state is a high level.

bit 4 **TXCKP**: Transmit/Clock Polarity Select bit
Asynchronous mode:
1 = Transmit data (TX) is inverted. Idle state is a low level.
0 = No inversion of transmit data (TX). Idle state is a high level.
Synchronous mode:
1 = Idle state for clock (CK) is a high level
0 = Idle state for clock (CK) is a low level

bit 3 **BRG16:** 16-bit Baud Rate Register Enable bit
1 = 16-bit Baud Rate Generator – SPBRGH and SPBRG
0 = 8-bit Baud Rate Generator – SPBRG only (Compatible mode); SPBRGH value ignored

bit 2 **Unimplemented:** Read as '0'

REGISTER 18-3: BAUDCON: BAUD RATE CONTROL REGISTER (CONTINUED)

bit 1 **WUE:** Wake-up Enable bit

Asynchronous mode:

1 = EUSART will continue to sample the RX pin with the interrupt generated on the falling edge; bit cleared in hardware on following rising edge

0 = RX pin is not monitored or rising edge detected

Synchronous mode:

Unused in this mode.

bit 0 **ABDEN**: Auto-Baud Detect Enable bit

Asynchronous mode:

1 = Enable baud rate measurement on the next character. Requires reception of a Sync field (55h); cleared in hardware upon completion.

0 = Baud rate measurement disabled or completed

Synchronous mode:

Unused in this mode.

4. Module: 10-Bit Analog-to-Digital Converter

When the AD clock source is selected as 2 TOSC or RC (when ADCS2:ADCS0 = 000 or x11), in extremely rare cases, the EIL (Integral Linearity Error) and EDL (Differential Linearity Error) may exceed the data sheet specification at codes 511 and 512 only.

Work around

Select the AD clock source as 4 TOSC, 8 TOSC, 16 TOSC, 32 TOSC or 64 TOSC and avoid selecting 2 TOSC or RC.

Date Codes that pertain to this issue:

All engineering and production devices.

5. Module: Enhanced Universal Synchronous Asynchronous Receiver Transmitter (EUSART)

In rare situations when interrupts are enabled, unexpected results may occur if:

- The EUSART is disabled (the SPEN bit, RCSTA <7>, = 0)
- The EUSART is re-enabled (RCSTA <7> = 1)
- A two-cycle instruction is executed

Work around

Add a 2-TCY delay after re-enabling the EUSART.

1. Disable Receive Interrupts (RCIE bit, PIE1<5>, = 0).
2. Disable the EUSART (RCSTA <7>, = 0).
3. Re-enable the EUSART (RCSTA <7> = 1).
4. Re-enable Receive Interrupts (PIE1<5> = 1).

   (This is the first TCY delay.)
5. Execute an NOP instruction.

   (This is the second TCY delay.)

Date Codes that pertain to this issue:

All engineering and production devices.

6. Module: Master Synchronous Serial Port (MSSP)

When configured for I²C™ slave reception, the MSSP module may not receive the correct data, in extremely rare cases. This occurs only if the Serial Receive/Transmit Buffer Register (SSPBUF) is not read after the SSPIF interrupt (PIR1<3>) has occurred, but before the first rising clock edge of the next byte being received.

Work around

The issue can be resolved in either of these ways:

- Prior to the I²C slave reception, enable the clock stretching feature.

  This is done by setting the SEN bit (SSPCON2<0>).
- Each time the SSPIF is set, read the SSPBUF before the first rising clock edge of the next byte being received.

Date Codes that pertain to this issue:

All engineering and production devices.

REVISION HISTORY

Rev A Document (2/2007)
First revision of this document. Silicon issue 1 (MSSP) and 2 (MSSP [SPI Master]).

Rev B Document (4/2007)
Added silicon issue 3 (Enhanced Universal Synchronous Receiver Transmitter – EUSART).

Rev C Document (6/2007)
Added silicon issue 4 (10-Bit Analog-to-Digital Converter).

Rev D Document (8/2009)
Added silicon issues 5 (EUSART) and 6 (MSSP).

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