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Kind regards,

Team Nexperia

# BUK7608-40B

## N-channel TrenchMOS standard level FET

Rev. 04 — 24 September 2008

Product data sheet

## 1. Product profile

### 1.1 General description

Standard level N-channel enhancement mode Field-Effect Transistor (FET) in a plastic package using TrenchMOS technology. This product has been designed and qualified to the appropriate AEC standard for use in automotive critical applications.

### 1.2 Features and benefits

- Low conduction losses due to low on-state resistance
- Q101 compliant
- Suitable for standard level gate drive sources
- Suitable for thermally demanding environments due to 175 °C rating

### 1.3 Applications

- 12 V loads
- Automotive systems
- General purpose power switching
- Motors, lamps and solenoids

### 1.4 Quick reference data

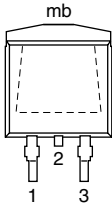
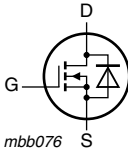
Table 1. Quick reference

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{DS}$	drain-source voltage	$T_j \geq 25\text{ °C}; T_j \leq 175\text{ °C}$	-	-	40	V
$I_D$	drain current	$V_{GS} = 10\text{ V}; T_{mb} = 25\text{ °C};$ see <a href="#">Figure 1</a> ; see <a href="#">Figure 3</a> ;	[1]	-	75	A
$P_{tot}$	total power dissipation	$T_{mb} = 25\text{ °C};$ see <a href="#">Figure 2</a>	-	-	157	W
<b>Avalanche ruggedness</b>						
$E_{DS(AL)S}$	non-repetitive drain-source avalanche energy	$I_D = 75\text{ A}; V_{sup} \leq 40\text{ V};$ $R_{GS} = 50\text{ }\Omega; V_{GS} = 10\text{ V};$ $T_{j(init)} = 25\text{ °C};$ unclamped	-	-	241	mJ
<b>Dynamic characteristics</b>						
$Q_{GD}$	gate-drain charge	$V_{GS} = 10\text{ V}; I_D = 25\text{ A};$ $V_{DS} = 32\text{ V}; T_j = 25\text{ °C};$ see <a href="#">Figure 14</a>	-	12	-	nC
<b>Static characteristics</b>						
$R_{DS(on)}$	drain-source on-state resistance	$V_{GS} = 10\text{ V}; I_D = 25\text{ A};$ $T_j = 25\text{ °C};$ see <a href="#">Figure 12</a> ; see <a href="#">Figure 11</a>	-	6.6	8	m $\Omega$

[1] Continuous current is limited by package.

## 2. Pinning information

**Table 2. Pinning information**

Pin	Symbol	Description	Simplified outline	Graphic symbol
1	G	gate	 <p><b>SOT404 (D2PAK)</b></p>	 <p>mbb076</p>
2	D	drain <a href="#">[1]</a>		
3	S	source		
mb	D	mounting base; connected to drain		

[1] It is not possible to make a connection to pin 2.

## 3. Ordering information

**Table 3. Ordering information**

Type number	Package		Version
	Name	Description	
BUK7608-40B	D2PAK	Plastic single-ended surface-mounted package (D2PAK); 3 leads (one lead cropped)	SOT404

## 4. Limiting values

**Table 4. Limiting values**

In accordance with the Absolute Maximum Rating System (IEC 60134).

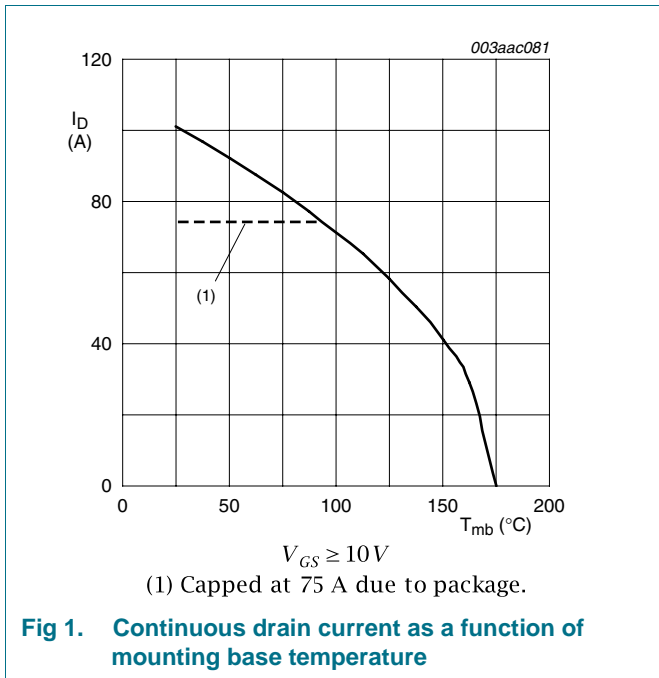
Symbol	Parameter	Conditions	Min	Max	Unit
$V_{DS}$	drain-source voltage	$T_j \geq 25\text{ °C}$ ; $T_j \leq 175\text{ °C}$	-	40	V
$V_{DGR}$	drain-gate voltage	$R_{GS} = 20\text{ k}\Omega$	-	40	V
$V_{GS}$	gate-source voltage		-20	20	V
$I_D$	drain current	$T_{mb} = 25\text{ °C}$ ; $V_{GS} = 10\text{ V}$ ; see <a href="#">Figure 1</a> ; see <a href="#">Figure 3</a> ; <a href="#">[1]</a>	-	101	A
		$T_{mb} = 100\text{ °C}$ ; $V_{GS} = 10\text{ V}$ ; see <a href="#">Figure 1</a> ; <a href="#">[1]</a>	-	71	A
		$T_{mb} = 25\text{ °C}$ ; $V_{GS} = 10\text{ V}$ ; see <a href="#">Figure 1</a> ; see <a href="#">Figure 3</a> ; <a href="#">[2]</a>	-	75	A
$I_{DM}$	peak drain current	$T_{mb} = 25\text{ °C}$ ; $t_p \leq 10\text{ }\mu\text{s}$ ; pulsed; see <a href="#">Figure 3</a>	-	407	A
$P_{tot}$	total power dissipation	$T_{mb} = 25\text{ °C}$ ; see <a href="#">Figure 2</a>	-	157	W
$T_{stg}$	storage temperature		-55	175	°C
$T_j$	junction temperature		-55	175	°C
<b>Source-drain diode</b>					
$I_S$	source current	$T_{mb} = 25\text{ °C}$ ; <a href="#">[1]</a>	-	101	A
		$T_{mb} = 25\text{ °C}$ ; <a href="#">[2]</a>	-	75	A
$I_{SM}$	peak source current	$t_p \leq 10\text{ }\mu\text{s}$ ; pulsed; $T_{mb} = 25\text{ °C}$	-	407	A

**Table 4. Limiting values ...continued**

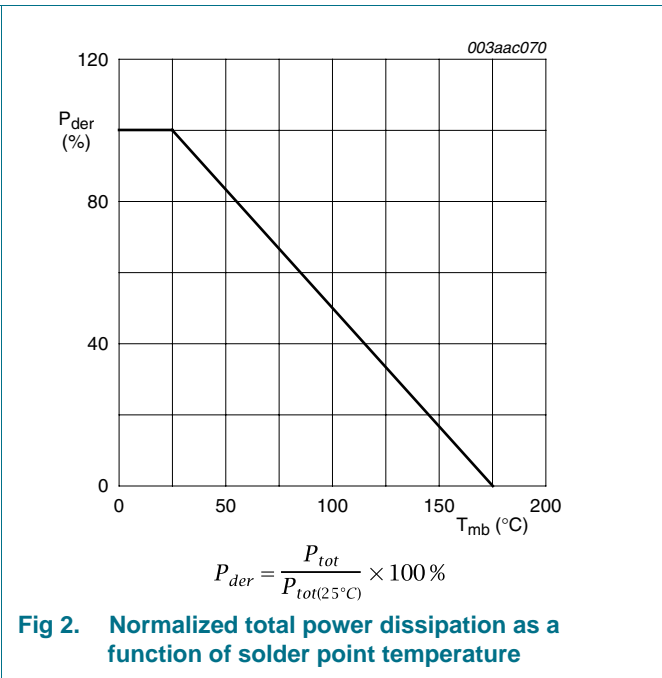
In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
<b>Avalanche ruggedness</b>					
$E_{DS(AL)S}$	non-repetitive drain-source avalanche energy	$I_D = 75\text{ A}$ ; $V_{sup} \leq 40\text{ V}$ ; $R_{GS} = 50\ \Omega$ ; $V_{GS} = 10\text{ V}$ ; $T_{j(\text{init})} = 25\text{ }^\circ\text{C}$ ; unclamped	-	241	mJ

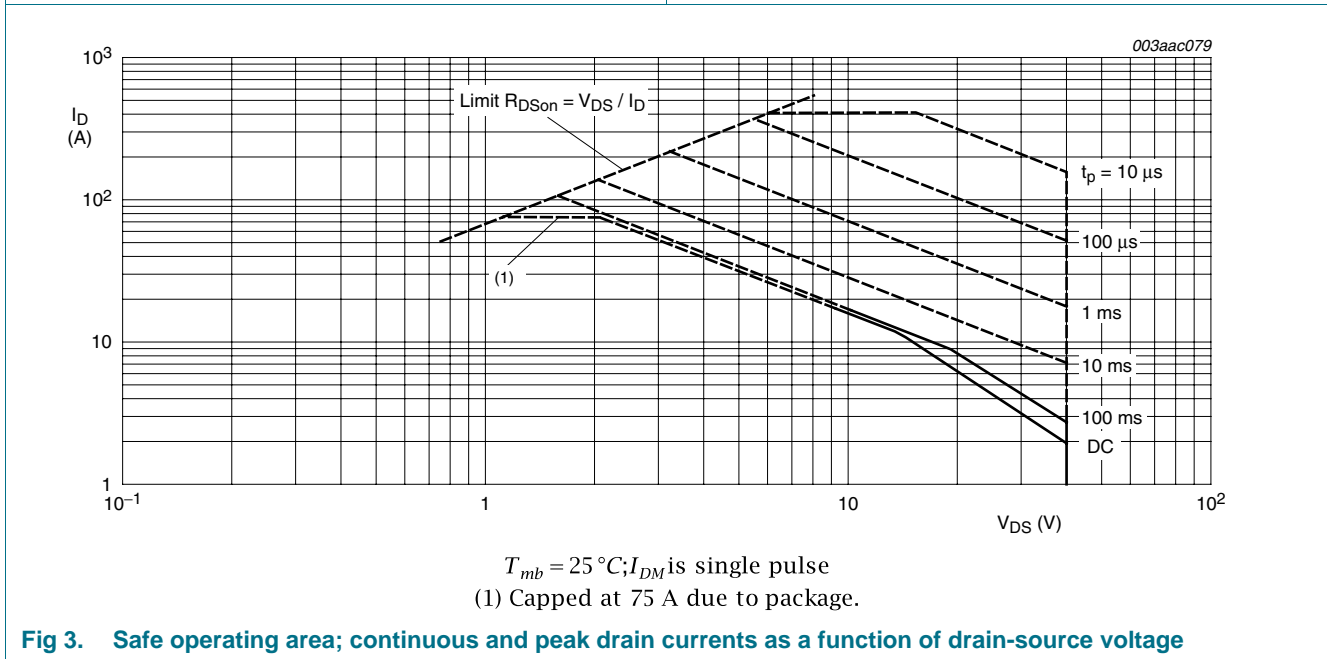
- [1] Current is limited by power dissipation chip rating.
- [2] Continuous current is limited by package.



**Fig 1. Continuous drain current as a function of mounting base temperature**



**Fig 2. Normalized total power dissipation as a function of solder point temperature**

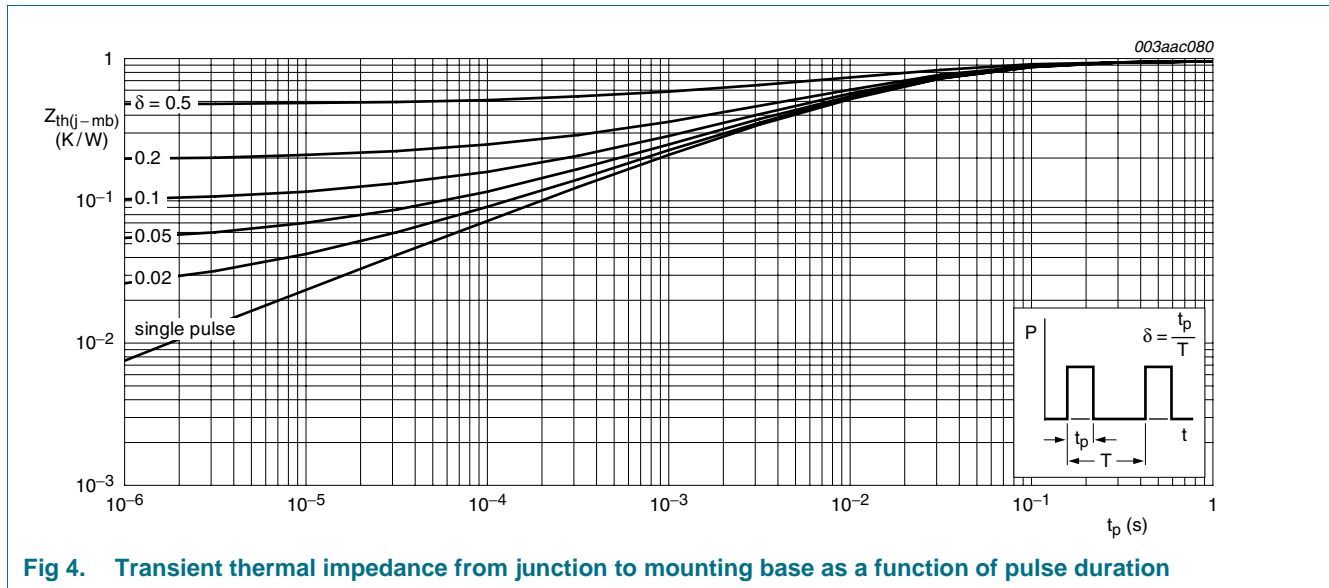


**Fig 3. Safe operating area; continuous and peak drain currents as a function of drain-source voltage**

## 5. Thermal characteristics

**Table 5. Thermal characteristics**

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$R_{th(j-a)}$	thermal resistance from junction to ambient	mounted on a printed-circuit board; minimum footprint	-	50	-	K/W
$R_{th(j-mb)}$	thermal resistance from junction to mounting base	see <a href="#">Figure 4</a>	-	-	0.95	K/W

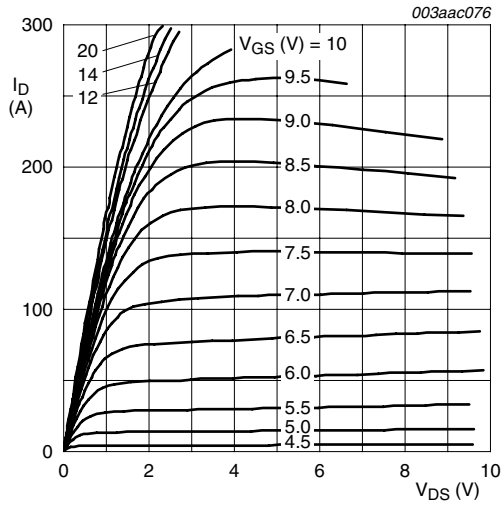


**Fig 4. Transient thermal impedance from junction to mounting base as a function of pulse duration**

## 6. Characteristics

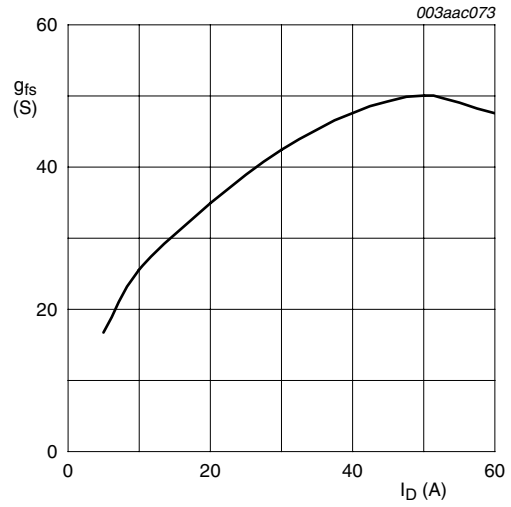
**Table 6. Characteristics**

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
<b>Static characteristics</b>						
$V_{(BR)DSS}$	drain-source breakdown voltage	$I_D = 0.25 \text{ mA}; V_{GS} = 0 \text{ V}; T_j = 25 \text{ }^\circ\text{C}$	40	-	-	V
		$I_D = 0.25 \text{ mA}; V_{GS} = 0 \text{ V}; T_j = -55 \text{ }^\circ\text{C}$	36	-	-	V
$V_{GS(th)}$	gate-source threshold voltage	$I_D = 1 \text{ mA}; V_{DS} = V_{GS}; T_j = 25 \text{ }^\circ\text{C}$ ; see <a href="#">Figure 9</a> ; see <a href="#">Figure 10</a>	2	3	4	V
		$I_D = 1 \text{ mA}; V_{DS} = V_{GS}; T_j = -55 \text{ }^\circ\text{C}$ ; see <a href="#">Figure 9</a> ; see <a href="#">Figure 10</a>	-	-	4.4	V
		$I_D = 1 \text{ mA}; V_{DS} = V_{GS}; T_j = 175 \text{ }^\circ\text{C}$ ; see <a href="#">Figure 9</a> ; see <a href="#">Figure 10</a>	1	-	-	V
$I_{DSS}$	drain leakage current	$V_{DS} = 40 \text{ V}; V_{GS} = 0 \text{ V}; T_j = 25 \text{ }^\circ\text{C}$	-	0.02	1	$\mu\text{A}$
		$V_{DS} = 40 \text{ V}; V_{GS} = 0 \text{ V}; T_j = 175 \text{ }^\circ\text{C}$	-	-	500	$\mu\text{A}$
$I_{GSS}$	gate leakage current	$V_{DS} = 0 \text{ V}; V_{GS} = 20 \text{ V}; T_j = 25 \text{ }^\circ\text{C}$	-	2	100	nA
		$V_{DS} = 0 \text{ V}; V_{GS} = -20 \text{ V}; T_j = 25 \text{ }^\circ\text{C}$	-	2	100	nA
$R_{DS(on)}$	drain-source on-state resistance	$V_{GS} = 10 \text{ V}; I_D = 25 \text{ A}; T_j = 175 \text{ }^\circ\text{C}$ ; see <a href="#">Figure 11</a> ; see <a href="#">Figure 12</a>	-	-	15.2	m $\Omega$
		$V_{GS} = 10 \text{ V}; I_D = 25 \text{ A}; T_j = 25 \text{ }^\circ\text{C}$ ; see <a href="#">Figure 12</a> ; see <a href="#">Figure 11</a>	-	6.6	8	m $\Omega$
<b>Dynamic characteristics</b>						
$Q_{G(tot)}$	total gate charge	$I_D = 25 \text{ A}; V_{DS} = 32 \text{ V}; V_{GS} = 10 \text{ V}; T_j = 25 \text{ }^\circ\text{C}$ ; see <a href="#">Figure 14</a>	-	36	-	nC
$Q_{GS}$	gate-source charge		-	9	-	nC
$Q_{GD}$	gate-drain charge		-	12	-	nC
$C_{iss}$	input capacitance	$V_{GS} = 0 \text{ V}; V_{DS} = 25 \text{ V}; f = 1 \text{ MHz}; T_j = 25 \text{ }^\circ\text{C}$ ; see <a href="#">Figure 15</a>	-	2017	2689	pF
$C_{oss}$	output capacitance		-	486	583	pF
$C_{rss}$	reverse transfer capacitance		-	213	291	pF
$t_{d(on)}$	turn-on delay time	$V_{DS} = 30 \text{ V}; R_L = 1.2 \text{ } \Omega; V_{GS} = 10 \text{ V}; R_{G(ext)} = 10 \text{ } \Omega; T_j = 25 \text{ }^\circ\text{C}$	-	20	-	ns
$t_r$	rise time		-	51	-	ns
$t_{d(off)}$	turn-off delay time		-	20	-	ns
$t_f$	fall time		-	33	-	ns
$L_D$	internal drain inductance	from drain lead 6 mm from package to center of die; $T_j = 25 \text{ }^\circ\text{C}$	-	4.5	-	nH
		from upper edge of drain mounting base to centre of die; $T_j = 25 \text{ }^\circ\text{C}$	-	2.5	-	nH
$L_S$	internal source inductance	from source lead 6 mm from package to source bond pad; $T_j = 25 \text{ }^\circ\text{C}$	-	7.5	-	nH
<b>Source-drain diode</b>						
$V_{SD}$	source-drain voltage	$I_S = 25 \text{ A}; V_{GS} = 0 \text{ V}; T_j = 25 \text{ }^\circ\text{C}$ ; see <a href="#">Figure 13</a>	-	0.85	1.2	V
$t_{rr}$	reverse recovery time	$I_S = 20 \text{ A}; di_S/dt = -100 \text{ A}/\mu\text{s}; V_{GS} = -10 \text{ V}; V_{DS} = 20 \text{ V}; T_j = 25 \text{ }^\circ\text{C}$	-	53	-	ns
$Q_r$	recovered charge		-	44	-	nC



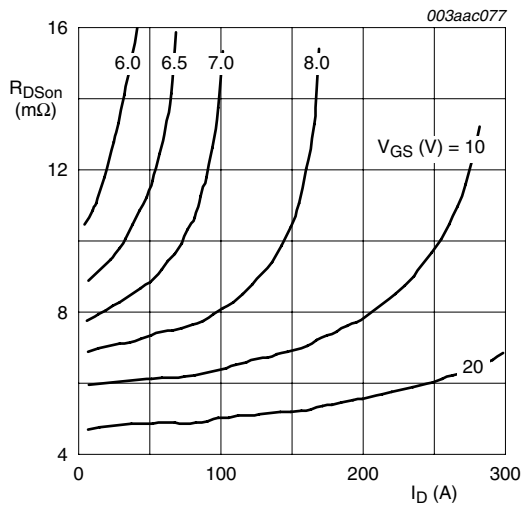
$T_j = 25^\circ\text{C}; t_p = 300\mu\text{s}$

**Fig 5. Output characteristics: drain current as a function of drain-source voltage; typical values**



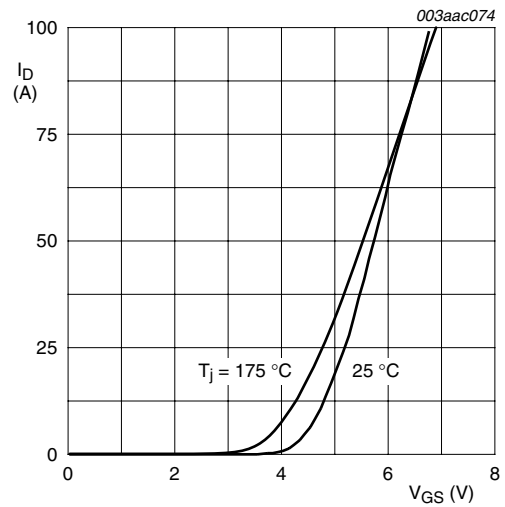
$T_j = 25^\circ\text{C}; V_{DS} = 25\text{V}$

**Fig 6. Forward transconductance as a function of drain current; typical values**



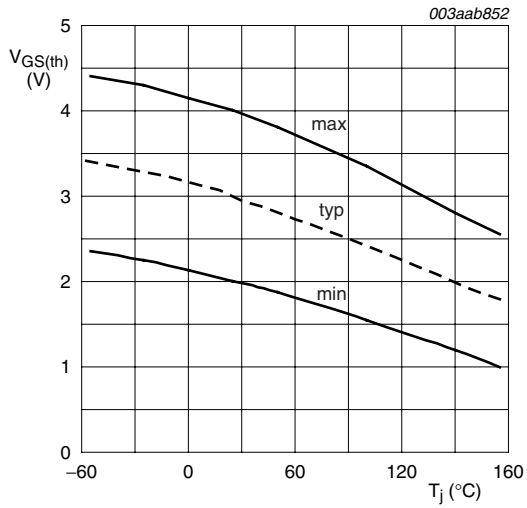
$T_j = 25^\circ\text{C}$

**Fig 7. Drain-source on-state resistance as a function of drain current; typical values**



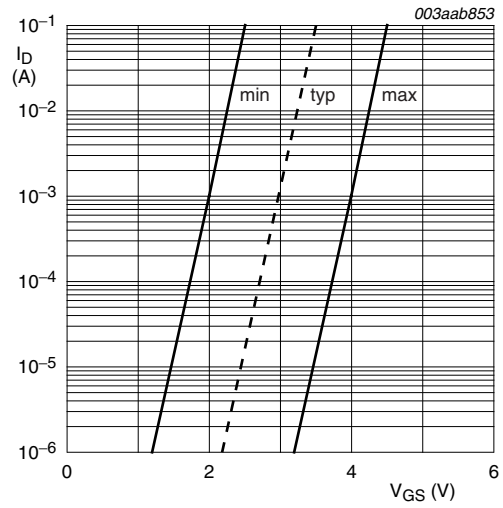
$V_{DS} = 25\text{V}$

**Fig 8. Transfer characteristics: drain current as a function of gate-source voltage; typical values**



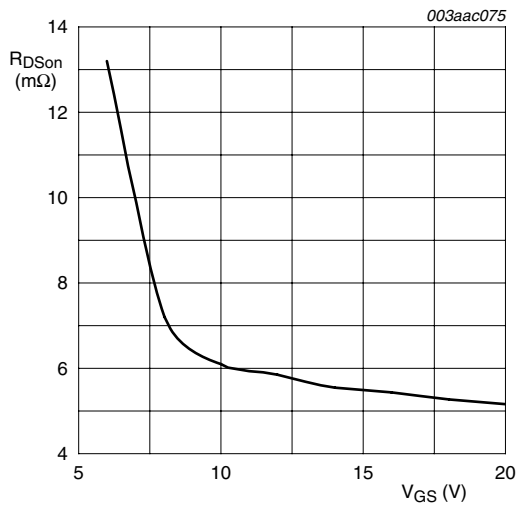
$$I_D = 1\text{ mA}; V_{DS} = V_{GS}$$

**Fig 9. Gate-source threshold voltage as a function of junction temperature**



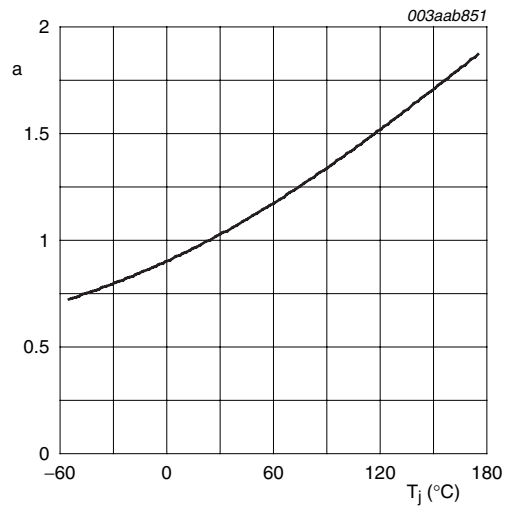
$$T_j = 25\text{ }^\circ\text{C}; V_{DS} = V_{GS}$$

**Fig 10. Sub-threshold drain current as a function of gate-source voltage**



$$T_j = 25\text{ }^\circ\text{C}; I_D = 25\text{ A}$$

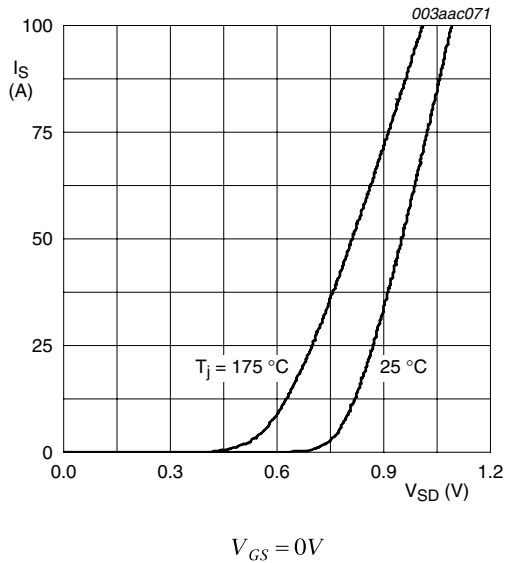
**Fig 11. Drain-source on-state resistance as a function of gate-source voltage; typical values**



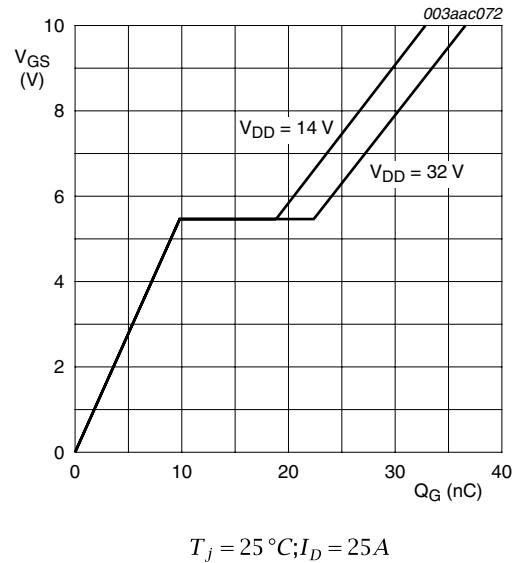
$$a = \frac{R_{DSon}}{R_{DSon(25^\circ\text{C})}}$$

**Fig 12. Normalized drain-source on-state resistance factor as a function of junction temperature**

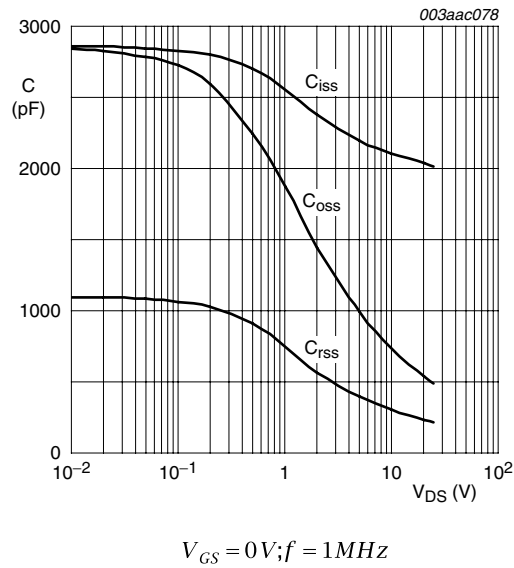




**Fig 13. Reverse diode current as a function of reverse diode voltage; typical values**



**Fig 14. Gate-source voltage as a function of turn-on gate charge; typical values**

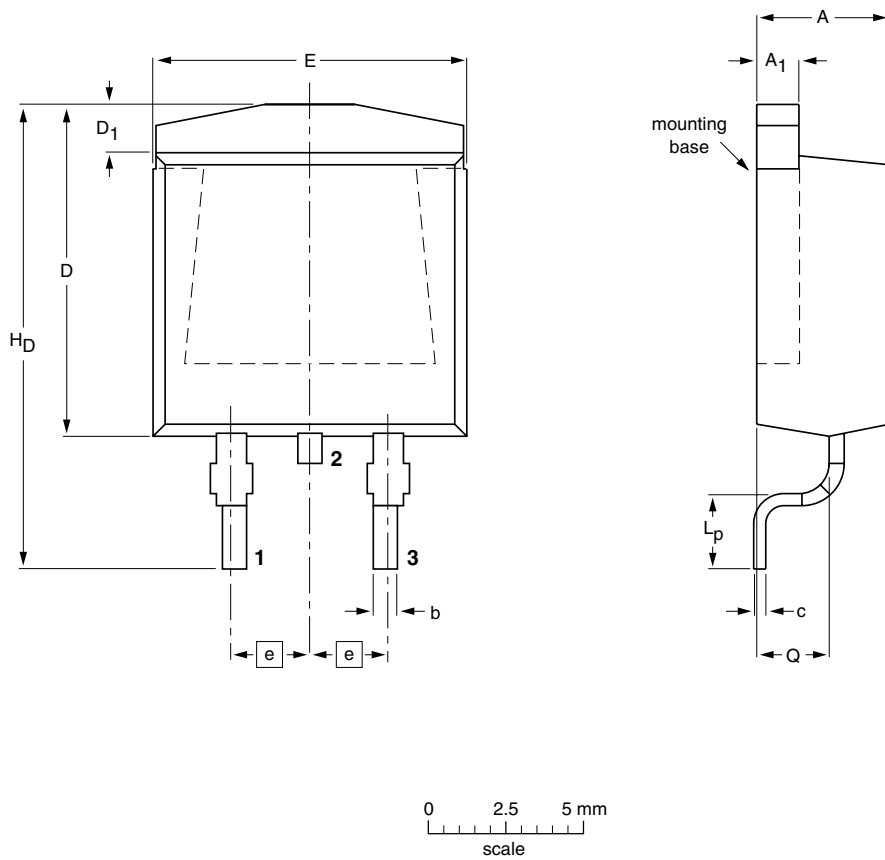


**Fig 15. Input, output and reverse transfer capacitances as a function of drain-source voltage; typical values**

**7. Package outline**

Plastic single-ended surface-mounted package (D2PAK); 3 leads (one lead cropped)

**SOT404**



**DIMENSIONS** (mm are the original dimensions)

UNIT	A	A <sub>1</sub>	b	c	D max.	D <sub>1</sub>	E	e	L <sub>p</sub>	H <sub>D</sub>	Q
mm	4.50	1.40	0.85	0.64	11	1.60	10.30	2.54	2.90	15.80	2.60
	4.10	1.27	0.60	0.46		1.20	9.70		2.10	14.80	2.20

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT404						05-02-11 06-03-16

**Fig 16. Package outline SOT404 (D2PAK)**

## 8. Revision history

Table 7. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
BUK7608-40B_4	20080924	Product data sheet	-	BUK75_7608-40B_3
Modifications:	• Type number BUK7608-40B separated from data sheet BUK75_7608-40B_3			
BUK75_7608-40B_3	20071128	Product data sheet	-	BUK75_7608-40B_2
BUK75_7608-40B_2	20071116	Product data sheet	-	BUK75_7608_40B-01
BUK75_7608_40B-01	20030319	Product data sheet	-	-

## 9. Legal information

### 9.1 Data sheet status

Document status <sup>[1][2]</sup>	Product status <sup>[3]</sup>	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

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**11. Contents**

**1 Product profile . . . . .1**

1.1 General description . . . . .1

1.2 Features and benefits . . . . .1

1.3 Applications . . . . .1

1.4 Quick reference data . . . . .1

**2 Pinning information . . . . .2**

**3 Ordering information . . . . .2**

**4 Limiting values . . . . .2**

**5 Thermal characteristics . . . . .4**

**6 Characteristics . . . . .5**

**7 Package outline . . . . .9**

**8 Revision history . . . . .10**

**9 Legal information . . . . .11**

9.1 Data sheet status . . . . .11

9.2 Definitions . . . . .11

9.3 Disclaimers . . . . .11

9.4 Trademarks . . . . .11

**10 Contact information . . . . .11**

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