SPECIFICATION

SPEC. No. C-ULI-a

D A T E : 2013 Sep.

To

CUSTOMER'S PRODUCT NAME	TDK PRODUCT NAME
	MULTILAYER CERAMIC CHIP CAPACITORS CLL Series / Commercial Grade Ultra Low Inductance

Please return this specification to TDK representatives.
If orders are placed without returned specification, please allow us to judge that specification is accepted by your side.

RECEIPT CONFIRMATION

DATE: YEAR MONTH DAY

TDK Corporation
Sales
Electronic Components
Sales & Marketing Group

TDK-EPC Corporation
Engineering
Ceramic Capacitors Business Group

APPROVED	Person in charge

APPROVED	CHECKED	Person in charge

1. SCOPE

This specification is applicable to chip type multilayer ceramic capacitors with a priority over the other relevant specifications.

Production places defined in this specification shall be TDK-EPC Corporation Japan, TDK (Suzhou) Co., Ltd and TDK Components U.S.A. Inc.

EXPLANATORY NOTE:

This specification warrants the quality of the ceramic chip capacitors. The chips should be evaluated or confirmed a state of mounted on your product.

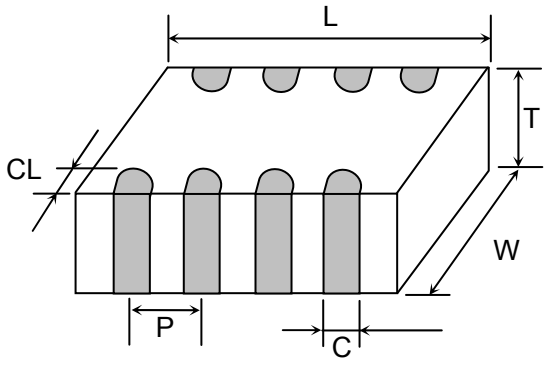
If the use of the chips goes beyond the bounds of the specification, we can not afford to guarantee.

2. CODE CONSTRUCTION

(Example)

Catalog Number : (Web)	CLLC1A (1)	X7S (2)	0G (3)	105 (4)	M (5)	050 (6)	A (7)	C (8)
Item Description :	CLLC1A (1)	X7S (2)	0G (3)	105 (4)	M (5)	T (9)	xxxx (10)	

(1) Type



Please refer to product list for the dimension of each product.

(2) Temperature Characteristics (Details are shown in table 1 No.6 at page 3)

(3) Rated Voltage

Symbol	Rated Voltage
1A	DC 10 V
0J	DC 6.3 V
0G	DC 4 V

(4) Rated Capacitance

Stated in three digits and in units of pico farads (pF).

The first and Second digits identify the first and second significant figures of the capacitance, the third digit identifies the multiplier.

R is designated for a decimal point.

Example 105 → 1,000,000pF

(5) Capacitance tolerance

Symbol	Tolerance
M	± 20 %

(6) Thickness code (Only Catalog Number)

(7) Package code (Only Catalog Number)

(8) Special code (Only Catalog Number)

(9) Packaging (Only Item Description)

Symbol	Packaging
B	Bulk
T	Taping

(10) Internal code (Only Item Description)

3. RATED CAPACITANCE AND CAPACITANCE TOLERANCE

3.1 Standard combination of rated capacitance and tolerances

Temperature Characteristics	Capacitance tolerance	Rated capacitance
X6S X7R X7S	M (± 20 %)	E – 6 series

3.2 Capacitance Step in E series

E series	Capacitance Step					
E- 6	1.0	1.5	2.2	3.3	4.7	6.8

4. OPERATING TEMPERATURE RANGE

T.C.	Min. operating Temperature	Max. operating Temperature	Reference Temperature
X6S	-55°C	105°C	25°C
X7R X7S	-55°C	125°C	25°C

5. STORING CONDITION AND TERM

5 to 40°C at 20 to 70%RH

6 months Max.

6. INDUSTRIAL WASTE DISPOSAL

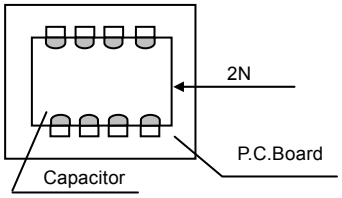
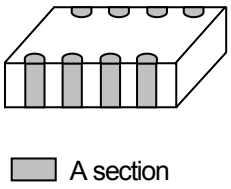
Dispose this product as industrial waste in accordance with the Industrial Waste Law.

7. PERFORMANCE

table 1

<table>
<tr><th>No.</th><th>Item</th><th>Performance</th><th>Test or inspection method</th></tr>
<tr><td>1</td><td>External Appearance</td><td>No defects which may affect performance.</td><td>Inspect with magnifying glass.
(×3 magnifications)</td></tr>
<tr><td>2</td><td>Insulation Resistance</td><td>100MΩ·μF min.</td><td>Apply rated voltage for 60s.
Measure 8 terminal electrodes at the same time.</td></tr>
<tr><td>3</td><td>Voltage Proof</td><td>Withstand test voltage without insulation breakdown or other damage.</td><td>2.5 times of rated voltage
Above DC voltage shall be applied for 1~5s.
Charge / discharge current shall not exceed 50mA.
Measure 8 terminal electrodes at the same time.</td></tr>
<tr><td>4</td><td>Capacitance</td><td>Within the specified tolerance at 1000hrs age (Per IEC-384-9).</td><td>
<table>
<tr><th>Measuring frequency</th><th>WV</th><th>Measuring voltage</th></tr>
<tr><td rowspan="2">1kHz±10%</td><td>10V</td><td>1.0±0.2Vrms.</td></tr>
<tr><td>6.3V and under</td><td>0.5±0.2Vrms.</td></tr>
</table>
Measure 8 terminal electrodes at the same time.
</td></tr>
<tr><td>5</td><td>Dissipation Factor</td><td>Characteristics
<table>
<tr><th>T.C.</th><th>D.F.</th></tr>
<tr><td>X6S
X7R
X7S</td><td>0.10 max.</td></tr>
</table>
</td><td>See No.4 in this table for measuring condition.</td></tr>
<tr><td>6</td><td>Temperature Characteristics of Capacitance</td><td>
<table>
<tr><th>Capacitance Change (%)</th></tr>
<tr><td>No DC voltage applied</td></tr>
<tr><td>X7R : ±15
X6S
X7S : ±22</td></tr>
</table>
</td><td>Capacitance shall be measured by the steps shown in the following table after thermal equilibrium is obtained for each step.
Capacitance change shall be calculated by the value of the reference temperature in Step 3.
<table>
<tr><th>Step</th><th>Temperature(°C)</th></tr>
<tr><td>1</td><td>Reference temp.
per para.4. ± 2</td></tr>
<tr><td>2</td><td>Min. operating temp.
per para.4. ± 2</td></tr>
<tr><td>3</td><td>Reference temp.
per para.4. ± 2</td></tr>
<tr><td>4</td><td>Max. operating temp.
per para.4. ± 2</td></tr>
</table>
</td></tr>
</table>

(continued)

<table>
<tr><th>No.</th><th colspan="2">Item</th><th>Performance</th><th>Test or inspection method</th></tr>
<tr><td>7</td><td colspan="2">Robustness of Terminations</td><td>No sign of termination coming off, breakage of ceramic, or other abnormal signs.</td><td>Reflow solder the capacitors on a P.C.Board shown in Appendix 1 and 2 and apply a pushing force of for 10±1s.
 
</td></tr>
<tr><td>8</td><td colspan="2">Solderability</td><td>All terminations shall exhibit a continuous solder coating free from defects for a minimum of 75% of the surface area of any individual termination. Anomalies other than dewetting, non-wetting, and pin holes are not cause for rejection.
 
</td><td>Completely soak both terminations in solder at 235±5°C for 2±0.5s.

Solder : H63A (JIS Z 3282)

Flux : Isopropyl alcohol (JIS K 8839)
Rosin(JIS K 5902) 25% solid solution.</td></tr>
<tr><td rowspan="4">9</td><td rowspan="4">Resistance to solder heat</td><td>External appearance</td><td>No cracks are allowed and terminations shall be covered at least 60% with new solder.</td><td rowspan="4">Completely soak both terminations in solder at 260±5°C for 5±1s.

Preheating condition
Temp. : 150±10°C
Time : 1 to 2min.

Flux : Isopropyl alcohol (JIS K 8839)
Rosin (JIS K 5902) 25% solid solution.

Solder : H63A (JIS Z 3282)

Leave the capacitors in ambient condition for 24±2h before measurement.</td></tr>
<tr><td>Capacitance</td><td><table><tr><th>Characteristics</th><th>Change from the value before test</th></tr><tr><td>X6S
X7R
X7S</td><td>± 7.5 %</td></tr></table></td></tr>
<tr><td>D.F.</td><td>Meet the initial spec.</td></tr>
<tr><td>Insulation Resistance</td><td>Meet the initial spec.</td></tr>
</table>

(continued)

<table>
<tr><th>No.</th><th colspan="2">Item</th><th>Performance</th><th>Test or inspection method</th></tr>
<tr><td rowspan="3">10</td><td rowspan="3">Vibration</td><td>External appearance</td><td>No mechanical damage.</td><td rowspan="3">Reflow solder the specimens on a P.C.Board shown in Appendix 1 and 2 before testing.

Vibrate the specimens with amplitude of 1.5mm p-p sweeping the frequencies from 10Hz to 55Hz and back to 10Hz in a minute.
Repeat this cycle for 2h each in 3 perpendicular directions (6h in total).</td></tr>
<tr><td>Capacitance</td><td><table><tr><th>Characteristics</th><th>Change from the value before test</th></tr><tr><td>X6S
X7R
X7S</td><td>± 7.5 %</td></tr></table></td></tr>
<tr><td>D.F.</td><td>Meet the initial spec.</td></tr>
<tr><td rowspan="5">11</td><td rowspan="5">Temperature cycle</td><td>External appearance</td><td>No mechanical damage.</td><td rowspan="5">Reflow Solder the capacitors on a P.C.Board shown in Appendix 1 and 2 before testing.
Expose the specimens in the condition step 1 through 4 and repeat 5 times consecutively.
Leave the specimens in ambient condition for the following time before measurement.<table><tr><th>Step</th><th>Temperature(°C)</th><th>Time (min.)</th></tr><tr><td>1</td><td>Min. operating temp. per para.4. ± 3</td><td>30 ± 3</td></tr><tr><td>2</td><td>Reference temp. per para.4.</td><td>2 - 5</td></tr><tr><td>3</td><td>Max. operating temp. per para.4. ± 2</td><td>30 ± 2</td></tr><tr><td>4</td><td>Reference temp. per para.4.</td><td>2 - 5</td></tr></table></td></tr>
<tr><td>Capacitance</td><td><table><tr><th>Characteristics</th><th>Change from the value before test</th></tr><tr><td>X6S
X7R
X7S</td><td>± 7.5 %</td></tr></table></td></tr>
<tr><td>D.F.</td><td>Meet the initial spec.</td></tr>
<tr><td>Insulation Resistance</td><td>Meet the initial spec.</td></tr>
<tr><td>Voltage proof</td><td>No insulation breakdown or other damage.</td></tr>
<tr><td rowspan="4">12</td><td rowspan="4">Moisture Resistance (Steady State)</td><td>External appearance</td><td>No mechanical damage.</td><td rowspan="4">Reflow Solder the capacitors on a P.C. Board shown in Appendix 1 and 2 before testing.

Leave at temperature 40 ± 2°C, 90 to 95%RH for 500 +24,0h.

Leave the specimens in ambient condition for 24 ± 2h before the measurement.</td></tr>
<tr><td>Capacitance</td><td><table><tr><th>Characteristics</th><th>Change from the value before test</th></tr><tr><td>X6S
X7R
X7S</td><td>± 7.5 %</td></tr></table></td></tr>
<tr><td>D.F.</td><td>200% of initial spec. max.</td></tr>
<tr><td>Insulation Resistance</td><td>10MΩ·μF min.</td></tr>
</table>

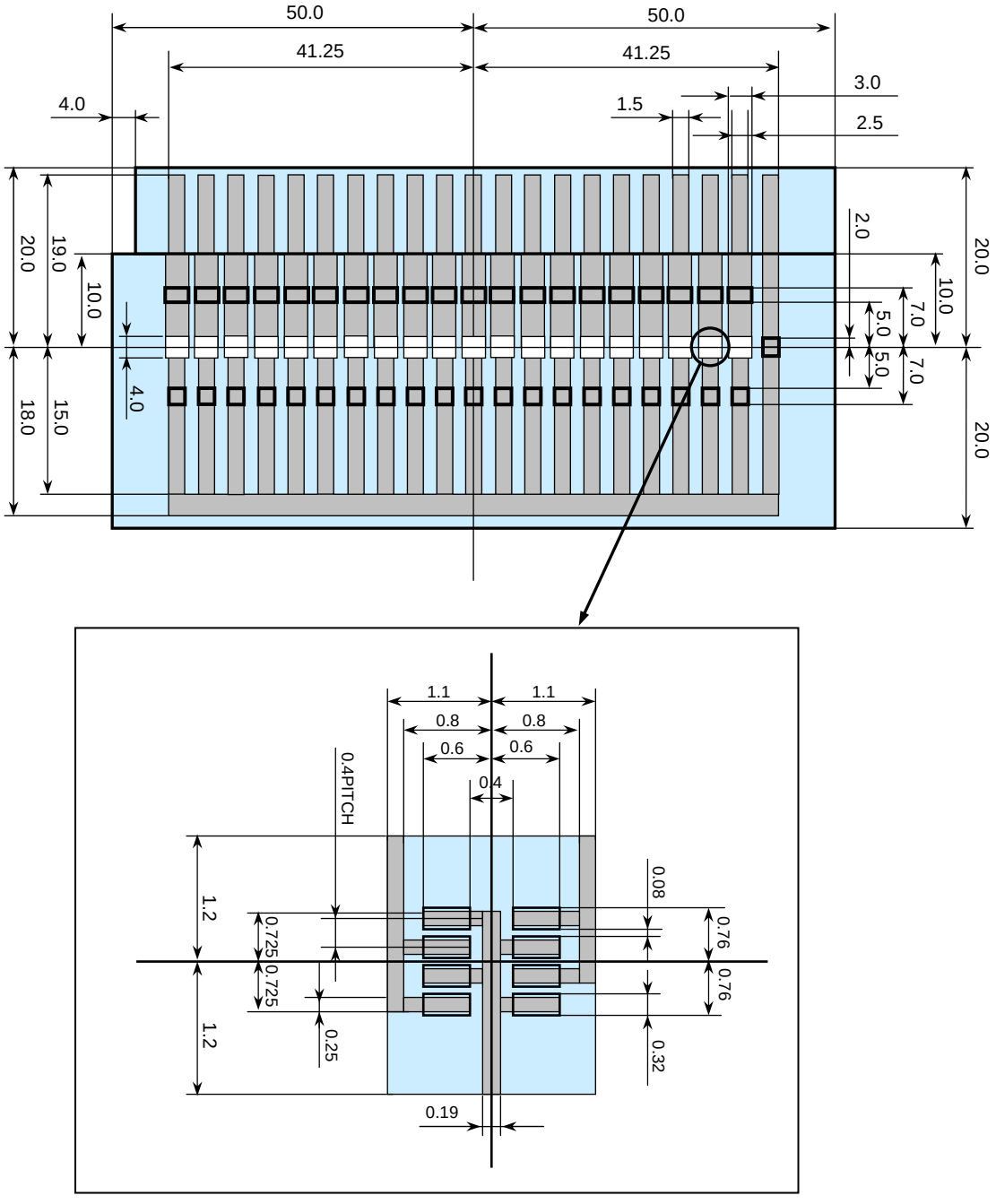
(continued)

<table>
<tr><th>No.</th><th colspan="2">Item</th><th>Performance</th><th>Test or inspection method</th></tr>
<tr><td rowspan="4">13</td><td rowspan="4">Moisture Resistance</td><td>External appearance</td><td>No mechanical damage.</td><td rowspan="4">Reflow Solder the capacitors on a P.C. Board shown in Appendix 1 and 2 before testing.
Apply the rated voltage at temperature 40±2°C, and 90 to 95%RH for 500+24,0h
Charge/discharge current shall not exceed 50mA.
Leave the capacitors in ambient condition for 48 ± 4h before measurement.
Voltage conditioning:
Voltage treat the specimen under testing temperature and voltage for 1 hour.
Use this measurement for initial value.</td></tr>
<tr><td>Capacitance</td><td><table><tr><th>Characteristics</th><th>Change from the value before test</th></tr><tr><td>X6S
X7R
X7S</td><td>± 12.5 %</td></tr></table></td></tr>
<tr><td>D.F.</td><td>200% of initial spec. max.</td></tr>
<tr><td>Insulation Resistance</td><td>5MΩ·μF min.</td></tr>
<tr><td rowspan="4">14</td><td rowspan="4">Life</td><td>External appearance</td><td>No mechanical damage.</td><td rowspan="4">Reflow Solder the capacitors on a P.C.Board shown in Appendix 1 and 2 before testing.
Apply the rated voltage at maximum operating temperature ± 2°C for 1,000 +48,0h
Charge/discharge current shall not exceed 50mA.
Voltage conditioning:
Voltage treat the capacitors under testing temperature and voltage for 1 hour.
Leave the specimens in ambient condition for 48 ± 4h before measurement as initial value.</td></tr>
<tr><td>Capacitance</td><td><table><tr><th>Characteristics</th><th>Change from the value before test</th></tr><tr><td>X6S
X7R
X7S</td><td>± 15 %</td></tr></table></td></tr>
<tr><td>D.F.</td><td>200% of initial spec. max.</td></tr>
<tr><td>Insulation Resistance</td><td>10MΩ·μF min.</td></tr>
</table>

Appendix 1

CLLC1A

PC Board



(Unit: mm)

1. Material: Glass Epoxy (As per JIS C6484 GE4)

2. Thickness: 0.8mm

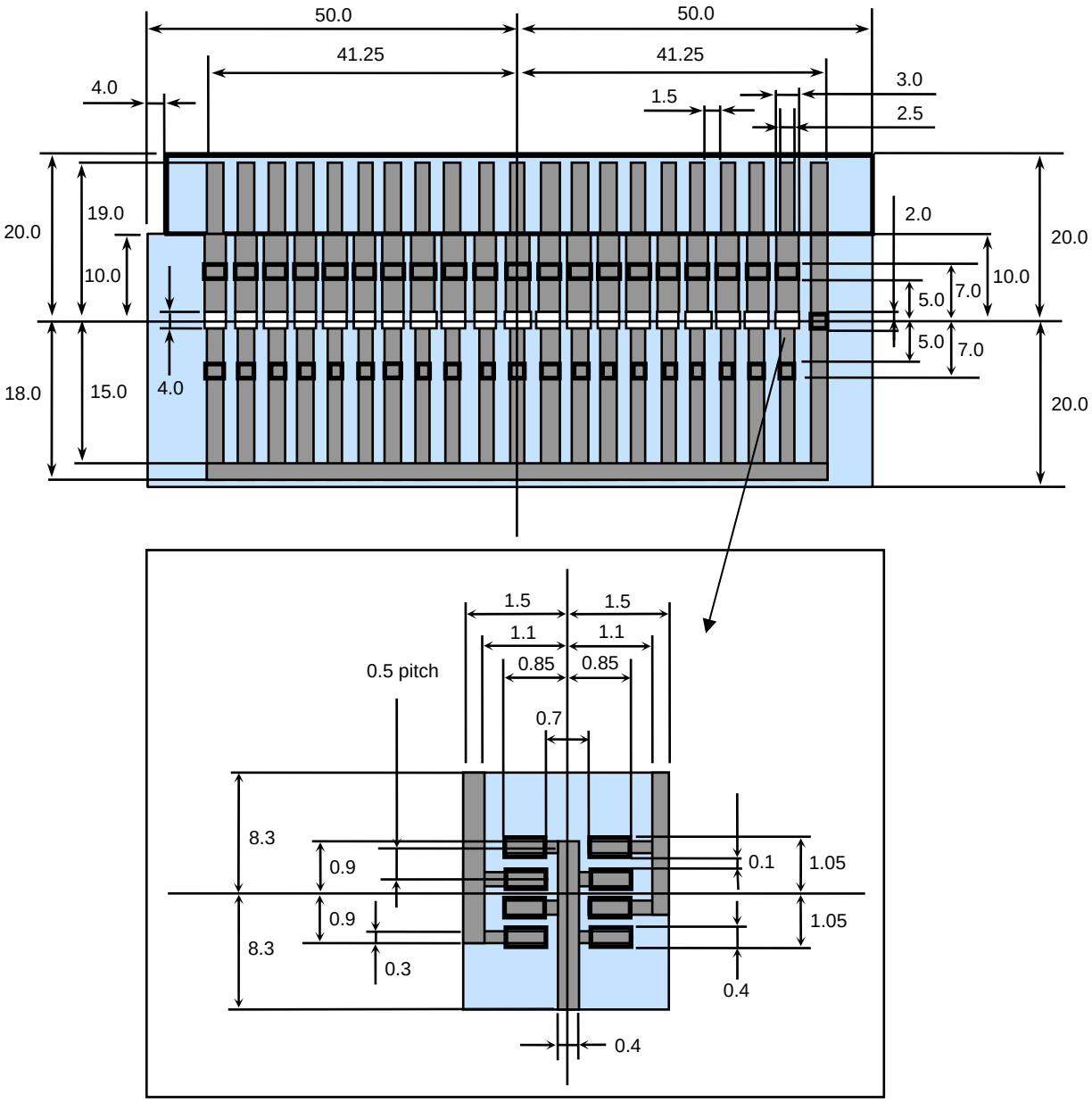
Copper (Thickness: 0.035mm)

Solder resist

Appendix 2

CLLE1A

PC Board



(Unit: mm)

1. Material: Glass Epoxy (As per JIS C6484 GE4)
2. Thickness: 1.6mm

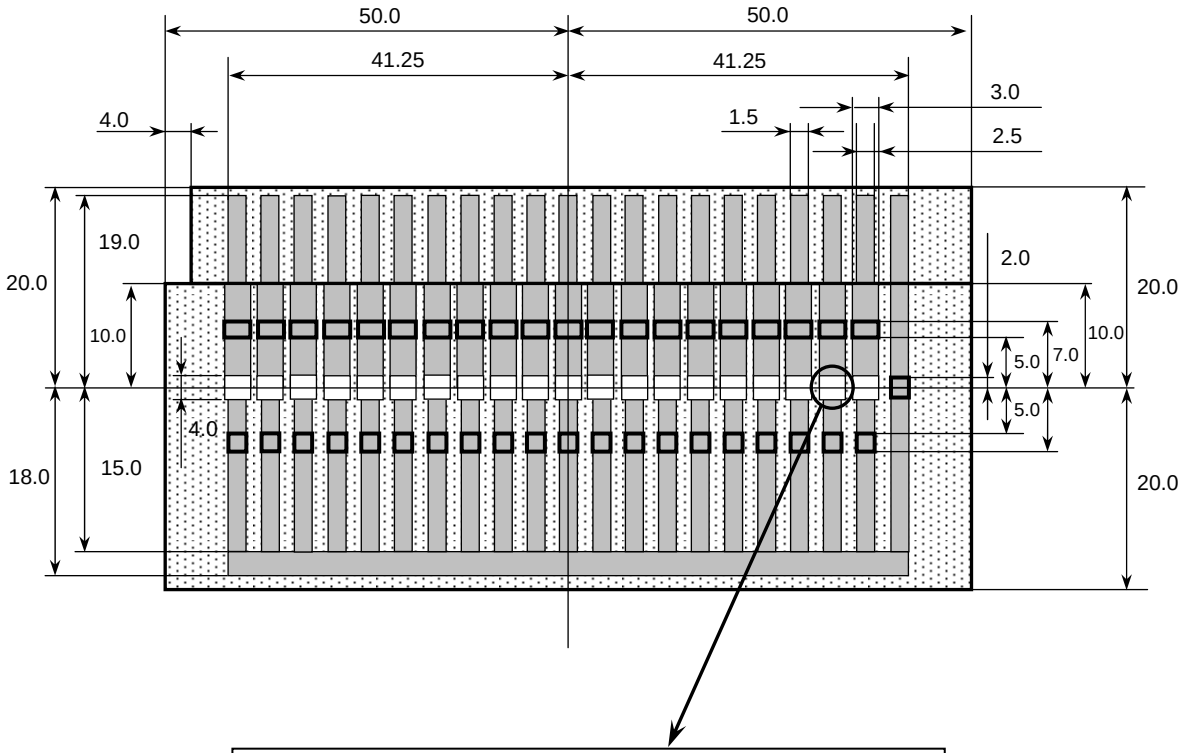
Copper (Thickness: 0.035mm)

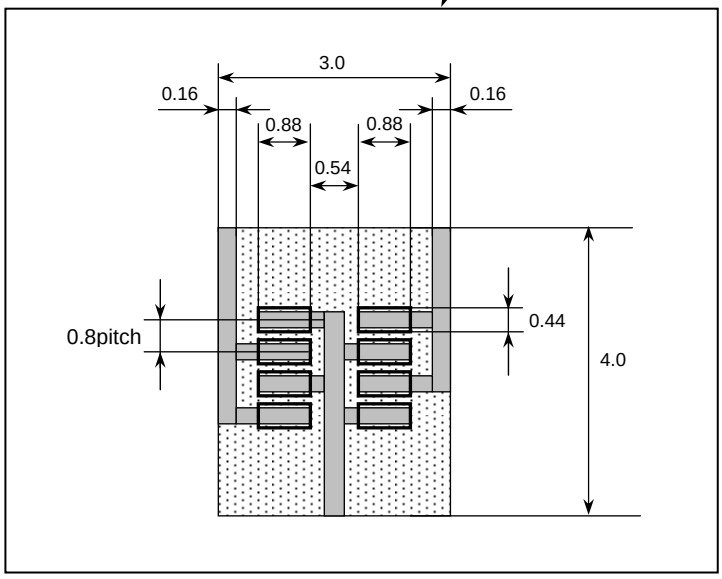
Solder resist

Appendix 3

CLLG1A

PC Board





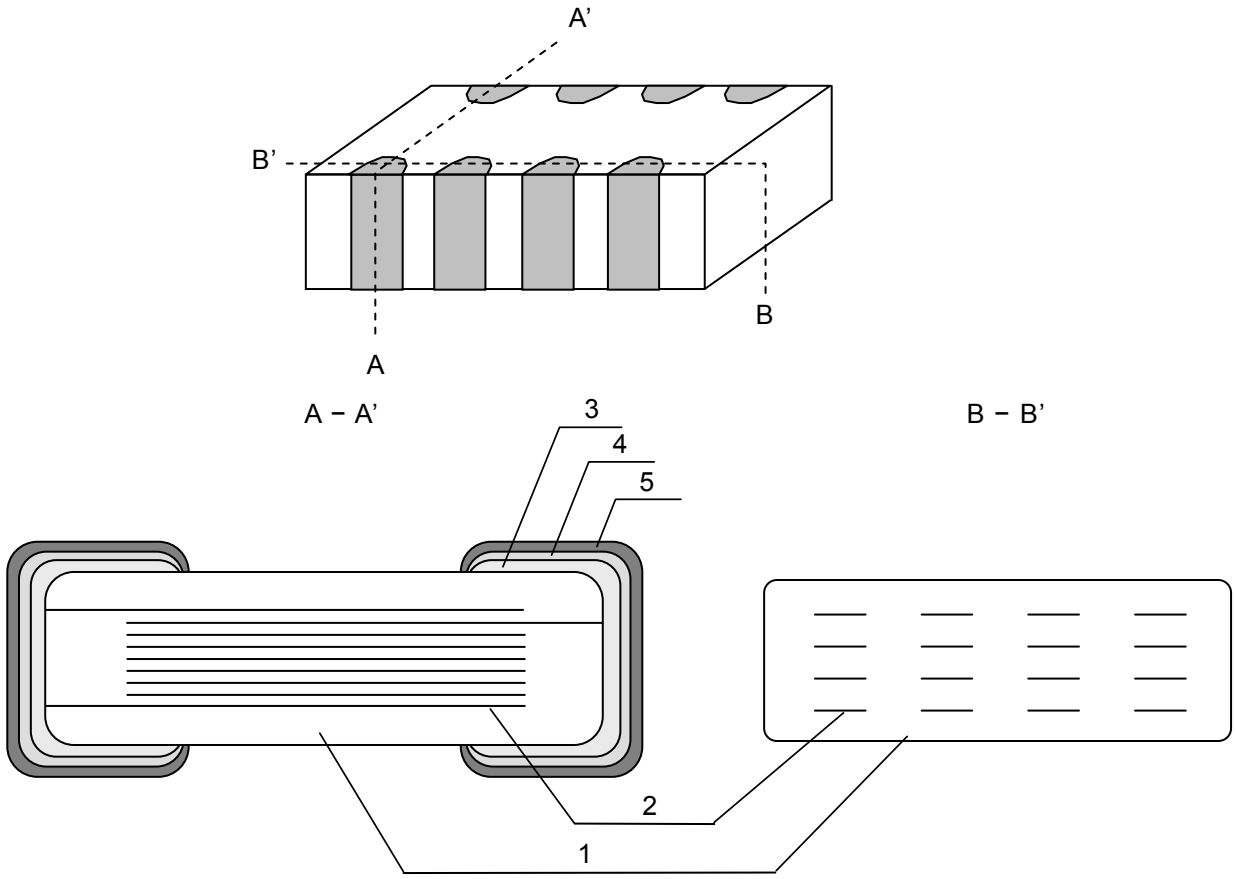
(UNIT: mm)

1. MATERIAL: GLASS EPOXY (AS PER JIS C6484 GE4)
2. THICKNESS: 1.6MM

COPPER (THICKNESS: 0.035MM)

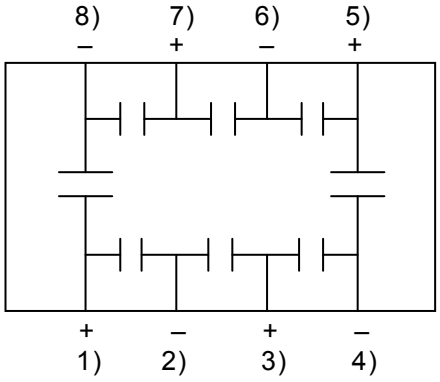
SOLDER RESIST

8. INSIDE STRUCTURE AND MATERIAL



No.	NAME	MATERIAL
1	Dielectric	$BaTiO_3$
2	Electrode	Ni
3	Termination	Cu
4		Ni
5		Sn

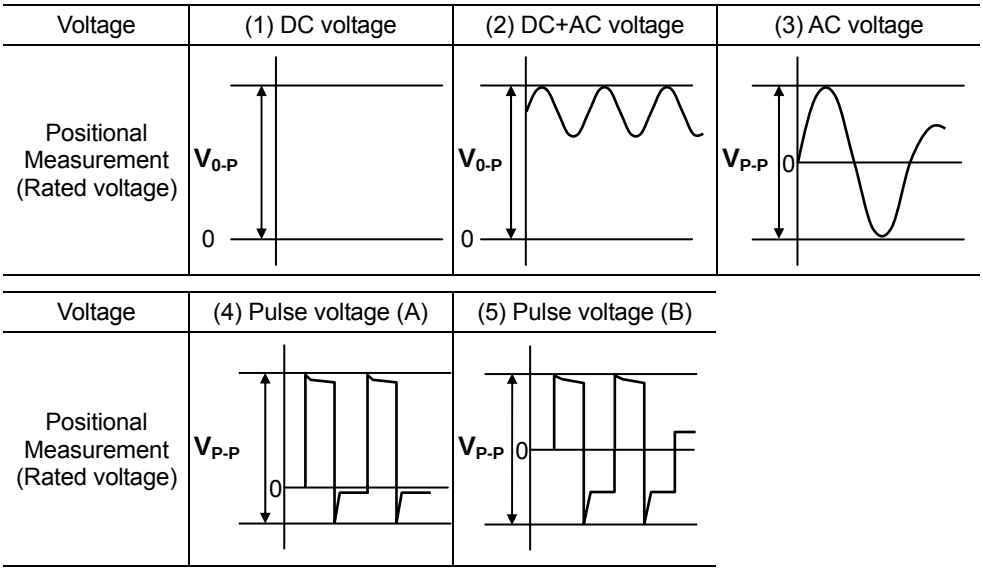
9. EQUIVALENT CIRCUIT



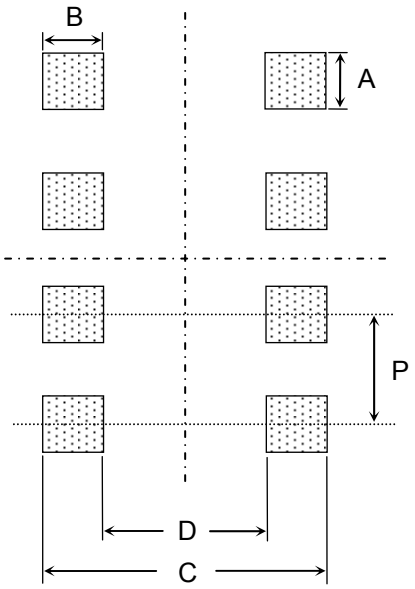
+ 1) 3) 5) 7)
– 2) 4) 6) 8)

8 terminals are connected and measured at the same time.

10. Caution

<table>
<tr><th>No.</th><th>Process</th><th>Condition</th></tr>
<tr><td>1</td><td>Operating Condition (Storage, Transportation)</td><td>1-1. Storage
1) The capacitors must be stored in an ambient temperature of 5 ~ 40°C with a relative humidity of 20~70%RH. The products should be used within 6 months upon receipt.
2) The capacitors must be operated and stored in an environment free of dew condensation and these gases such as Hydrogen Sulphide, Hydrogen Sulphate, Chlorine, Ammonia and sulfur.
3) Avoid storing in sun light and falling of dew.
4) Do not use capacitors under high humidity and high and low atmospheric pressure which may affect capacitors reliability.
5) Capacitors should be tested for the solderability when they are stored for long time.
1-2. Handling in transportation
In case of the transportation of the capacitors, the performance of the capacitors may be deteriorated depending on the transportation condition.
(Refer to JEITA RCR-2335B 9.2 Handling in transportation)</td></tr>
<tr><td>2</td><td>Circuit design
⚠ Caution</td><td>2-1 Operating temperature
Operating temperature should be followed strictly within this specification, especially be careful with maximum temperature.
1) Do not use capacitor above the maximum allowable operating temperature.
2) Surface temperature including self heating should be below maximum operating temperature.
(Due to dielectric loss, capacitor will heat itself when AC is applied. Especially at high frequencies around its SRF, the heat might be so extreme that it may damage itself or the product mounted on. Please design the circuit so that the maximum temperature of the capacitor including the self heating to be below the maximum allowable operating temperature. Temperature rise shall be below 20°C)
3) The electrical characteristics of the capacitors will vary depending on the temperature. The capacitors should be selected and designed in taking the temperature into consideration.
2-2 Operating voltage
1) Operating voltage across the terminals should be below the rated voltage.
When AC and DC are super imposed, $V_{0\text{-}P}$ must be below the rated voltage. ——— (1) and (2)
AC or pulse with overshooting, $V_{P\text{-}P}$ must be below the rated voltage. ——— (3), (4) and (5)
When the voltage is started to apply to the circuit or it is stopped applying, the irregular voltage may be generated for a transit period because of resonance or switching. Be sure to use a capacitor within rated voltage containing these irregular voltage.
 
</td></tr>
</table>

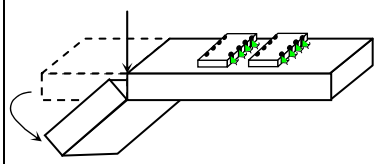
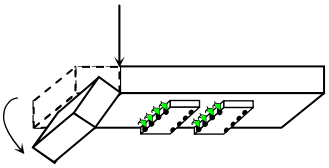
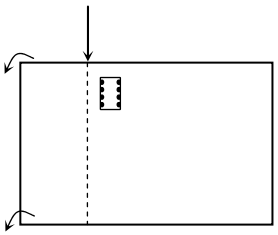
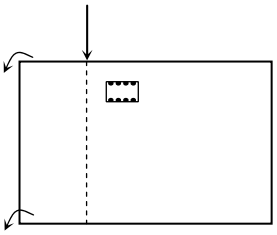
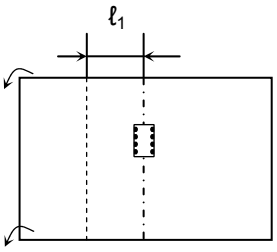
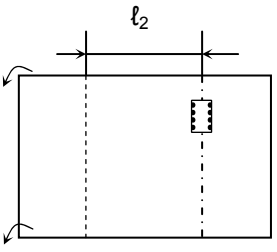
No.	Process	Condition
2	Circuit design ⚠ Caution	2) Even below the rated voltage, if repetitive high frequency AC or pulse is applied, the reliability of the capacitors may be reduced. 3) The effective capacitance will vary depending on applied DC and AC voltages. The capacitors should be selected and designed in taking the voltages into consideration. 2-3. Frequency When the capacitors (Class 2) are used in AC and/or pulse voltages, the capacitors may vibrate themselves and generate audible sound.
3	Designing P.C. board	The amount of solder at the terminations has a direct effect on the reliability of the capacitors. 1) The greater the amount of solder, the higher the stress on the chip capacitor, and the more likely that it will break. When designing a P.C. board, determine the shape and size of the solder lands to have proper amount of solder on the terminations. 2) Avoid using common solder land for multiple terminations and provide individual solder land for each terminations. 3) Size and recommended land dimensions.

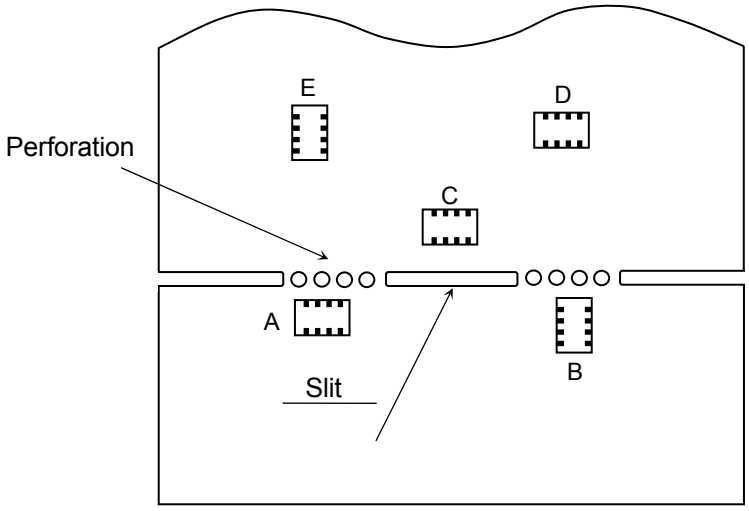


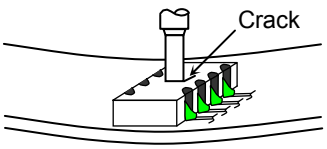
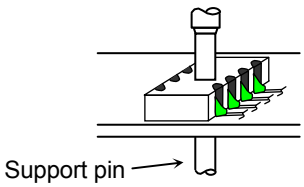
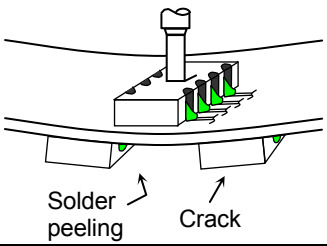
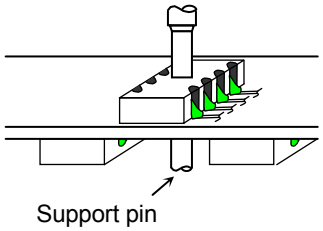
Recommended Land Dimensions (mm)

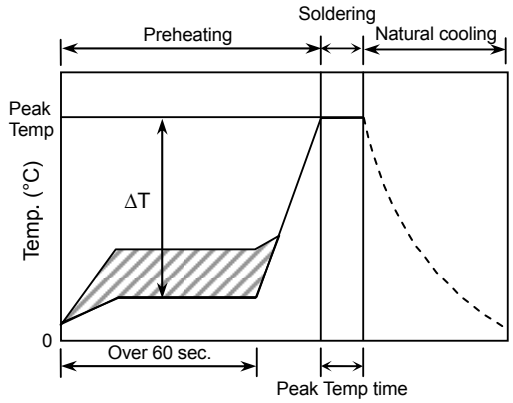
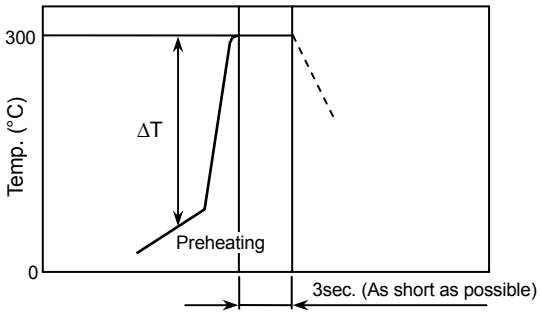
Type / Symbol	CLLC1A (CC0603)	CLLE1A (CC0805)	CLLG1A (CC1206)
A	0.25	0.30	0.44
B	0.40	0.30 - 0.60	0.88
C	1.20	1.30 - 1.80	2.30
D	0.40	0.50 - 0.80	0.54
P	0.40	0.50	0.80

No.	Process	Condition
3	Designing P.C. board	4) Recommended chip capacitor layout is as following.

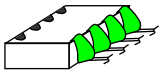
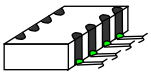
	Disadvantage against bending stress	Advantage against bending stress
Mounting face	Perforation or slit  Break P.C. board with mounted side up.	Perforation or slit  Break P.C. board with mounted side down.
Chip arrangement (Direction)	Mount perpendicularly to perforation or slit Perforation or slit 	Mount in parallel with perforation or slit Perforation or slit 
Distance from slit	Closer to slit is higher stress  $(\ell_1 < \ell_2)$	Away from slit is less stress  $(\ell_1 < \ell_2)$

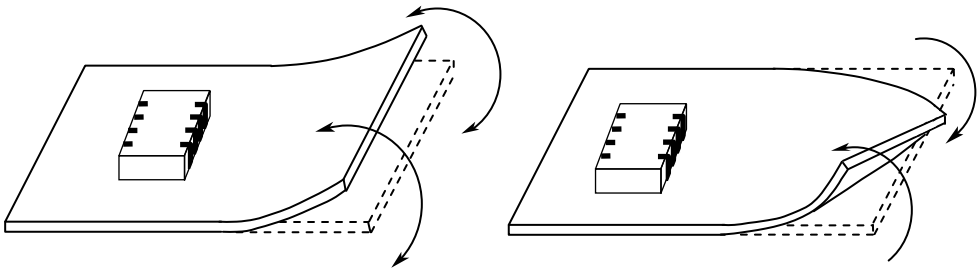
<table>
<tr><th>No.</th><th>Process</th><th>Condition</th></tr>
<tr><td>3</td><td>Designing P.C. board</td><td>5) Mechanical stress varies according to location of chip capacitors on the P.C. board.
 

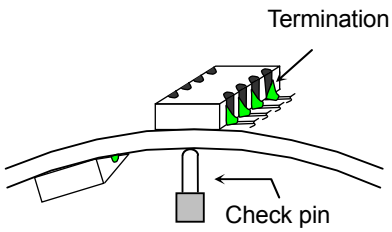
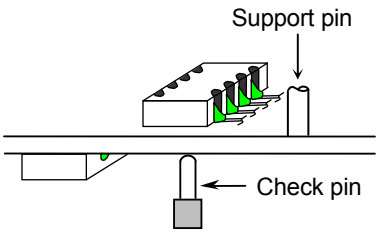
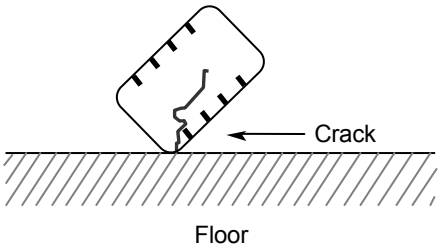
The stress in capacitors is in the following order.
A > B = C > D > E</td></tr>
<tr><td>4</td><td>Mounting</td><td>4-1. Stress from mounting head
If the mounting head is adjusted too low, it may induce excessive stress in the chip capacitor to result in cracking. Please take following precautions.
1) Adjust the bottom dead center of the mounting head to reach on the P.C. board surface and not press it.
2) Adjust the mounting head pressure to be 1 to 3N of static weight.
3) To minimize the impact energy from mounting head, it is important to provide support from the bottom side of the P.C. board. See following examples.
<table>
<tr><th></th><th>Not recommended</th><th>Recommended</th></tr>
<tr><td>Single sided mounting</td><td> 
</td><td> 
</td></tr>
<tr><td>Double-sides mounting</td><td> 
</td><td> 
</td></tr>
</table>
When the centering jaw is worn out, it may give mechanical impact on the capacitor to cause crack. Please control the close up dimension of the centering jaw and provide sufficient preventive maintenance and replacement of it.</td></tr>
</table>

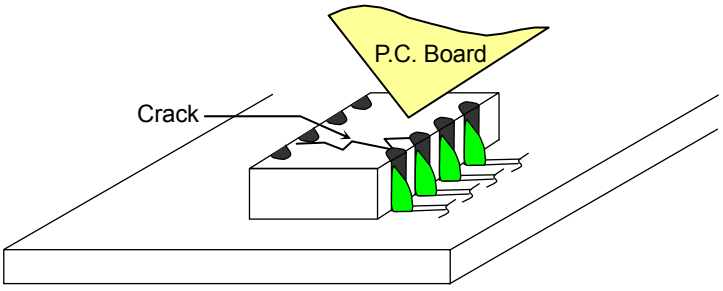
No.	Process	Condition
5	Soldering	5-1. Flux selection Although highly-activated flux gives better solderability, substances which Increase activity may also degrade the insulation of the chip capacitors. To avoid such degradation, it is recommended following. 1) It is recommended to use a mildly activated rosin flux (less than 0.1wt% chlorine). Strong flux is not recommended. 2) Excessive flux must be avoided. Please provide proper amount of flux. 3) When water-soluble flux is used, enough washing is necessary. 5-2. Recommended soldering profile by various methods Reflow soldering  Manual soldering (Solder iron)  5-3. Recommended soldering peak temp and peak temp duration Recommended solder compositions Sn-37Pb (Pb-Sn solder) Sn-3.0Ag-0.5Cu (Lead Free Solder)

Temp./Duration / Solder	Peak temp	Duration
Pb-Sn Solder	230°C max.	20 sec. max.
Lead Free Solder	260°C max.	10 sec. max.

No.	Process	Condition
5	Soldering	5-4. Avoiding thermal shock 1) Preheating condition Soldering / Temp. (°C): Reflow soldering: ΔT ≤ 150; Manual soldering: ΔT ≤ 150 2) Cooling condition Natural cooling using air is recommended. If the chips are dipped into a solvent for cleaning, the temperature difference (ΔT) must be less than 100°C. 5-5. Amount of solder Excessive solder will induce higher tensile force in chip capacitors when temperature changes and it may result in chip cracking. In sufficient solder may detach the capacitors from the P.C. board. 5-6. Amount of solder Excessive solder will induce higher tensile force in chip capacitor when temperature changes and it may result in chip cracking. In sufficient solder may detach the capacitor from the P.C. board. Excessive solder  Higher tensile force in chip capacitor to cause crack Adequate  Insufficient solder  Low robustness may cause contact failure or chip capacitor comes off the P.C. board. 5-7. Solder repair by solder iron 1) Selection of the soldering iron tip Tip temperature of solder iron varies by its type, P.C. board material and solder land size. Higher the tip temperature, quick the operation. Please make sure the tip temp. before soldering and keep the peak temp and time in accordance with following recommended condition. (Please preheat the chip capacitors with the condition in 5-4 to avoid the thermal shock.) Recommended solder iron condition (Pb-Sn Solder and Lead Free Solder) Temp. (°C) / Duration (sec.) / Wattage (W) / Shape (mm): 300 max. / 3 max. / 20 max. / Ø 3.0 max. 2) Direct contact of the soldering iron with ceramic dielectric of chip capacitors may cause crack. Do not touch the ceramic dielectric and the terminations by solder iron.

No.	Process	Condition
5	Soldering	5-8. Sn-Zn solder Sn-Zn solder affects product reliability. Please contact TDK in advance when utilize Sn-Zn solder. 5-9. Countermeasure for tombstone The misalignment between the mounted positions of the capacitors and the land patterns should be minimized. The tombstone phenomenon may occur especially the capacitors are mounted (in longitudinal direction) in the same direction of the reflow soldering. (Refer to JEITA RCR-2335B Annex A (Informative) Recommendations to prevent the tombstone phenomenon)
6	Cleaning	1) If an unsuitable cleaning fluid is used, flux residue or some foreign articles may stick to chip capacitor surface to deteriorate especially the insulation resistance. 2) If cleaning condition is not suitable, it may damage the chip capacitor. 2)-1. Insufficient washing (1) Lead wire and terminal electrodes may corrode by Halogen in the flux. (2) Halogen in the flux may adhere on the surface of capacitor, and lower the insulation resistance. (3) Water soluble flux has higher tendency to have above mentioned problems (1) and (2). 2)-2. Excessive washing (1) Excessive washing may damage the coating material of coated capacitor and deteriorate it. (2) When ultrasonic cleaning is used, excessively high ultrasonic energy output can affect the connection between the ceramic chip capacitor's body and the terminal electrode. To avoid this, following is the recommended condition. Power: 20W/ℓmax. Frequency: 40kHz max. Washing time: 5 minutes max. 2)-3. If the cleaning fluid is contaminated, density of Halogen increases, and it may bring the same result as insufficient cleaning.
7	Coating and molding of the P.C. board	1) When the P.C. board is coated, please verify the quality influence on the product. 2) Please verify carefully that there is no harmful decomposing or reaction gas emission during curing which may damage the chip capacitor. 3) Please verify the curing temperature.
8	Handling after chip mounted ⚠ Caution	1) Please pay attention not to bend or distort the P.C. board after soldering in handling otherwise the chip capacitor may crack. Bend Twist 

<table>
<tr><th>No.</th><th>Process</th><th>Condition</th></tr>
<tr><td></td><td></td><td>2) When functional check of the P.C. board is performed, check pin pressure tends to be adjusted higher for fear of loose contact. But if the pressure is excessive and bend the P.C. Board, it may crack the chip capacitor or peel the terminations off. Please adjust the check pins not to bend the P.C. Board.
<table>
<tr><th>Item</th><th>Not recommended</th><th>Recommended</th></tr>
<tr><td>Board bending</td><td> 
</td><td> 
</td></tr>
</table></td></tr>
<tr><td>9</td><td>Handling of loose chip capacitor</td><td>1) If dropped the chip capacitor may crack. Once dropped do not use it.
Especially, the large case sized chip capacitor is tendency to have cracks easily, so please handle with care.


2) Piling the P.C. board after mounting for storage or handling, the corner of the P.C. Board may hit the chip capacitor of another board to cause crack.

</td></tr>
</table>

No.	Process	Condition
10	Capacitance aging	The capacitors (Class 2) have aging in the capacitance. They may not be used in precision time constant circuit. In case of the time constant circuit, the evaluation should be done well.
11	Estimated life and estimated failure rate of capacitors	As per the estimated life and the estimated failure rate depend on the temperature and the voltage. This can be calculated by the equation described in JEITA RCR-2335B Annex 6 (Informative) Calculation of the estimated lifetime and the estimated failure rate (Voltage acceleration coefficient : 3 multiplication rule, Temperature acceleration coefficient : 10°C rule) The failure rate can be decreased by reducing the temperature and the voltage but they will not be guaranteed.
12	Others ⚠ Caution	The products listed on this specification sheet are intended for use in general electronic equipment (AV equipment, telecommunications equipment, home appliances, amusement equipment, computer equipment, personal equipment, office equipment, measurement equipment, industrial robots) under a normal operation and use condition. The products are not designed or warranted to meet the requirements of the applications listed below, whose performance and/or quality require a more stringent level of safety or reliability, or whose failure, malfunction or trouble could cause serious damage to society, person or property. Please understand that we are not responsible for any damage or liability caused by use of the products in any of the applications below or for any other use exceeding the range or conditions set forth in this specification sheet. If you intend to use the products in the applications listed below or if you have special requirements exceeding the range or conditions set forth in this specification, please contact us. (1) Aerospace/Aviation equipment (2) Transportation equipment (cars, electric trains, ships, etc.) (3) Medical equipment (4) Power-generation control equipment (5) Atomic energy-related equipment (6) Seabed equipment (7) Transportation control equipment (8) Public information-processing equipment (9) Military equipment (10) Electric heating apparatus, burning equipment (11) Disaster prevention/crime prevention equipment (12) Safety equipment (13) Other applications that are not considered general-purpose applications When designing your equipment even for general-purpose applications, you are kindly requested to take into consideration securing protection circuit/device or providing backup circuits in your equipment.

11. Packaging label

Packaging shall be done to protect the components from the damage during transportation and storing, and a label which has the following information shall be attached.

1) Inspection No.
2) TDK P/N
3) Customer's P/N
4) Quantity

*Composition of Inspection No.

Example M 2 A – OO – OOO
(a) (b) (c) (d) (e)

a) Line code
b) Last digit of the year
c) Month and A for January and B for February and so on. (Skip I)
d) Inspection Date of the month.
e) Serial No. of the day

12. Bulk packaging quantity

Total number of components in a plastic bag for bulk packaging: 1,000pcs.

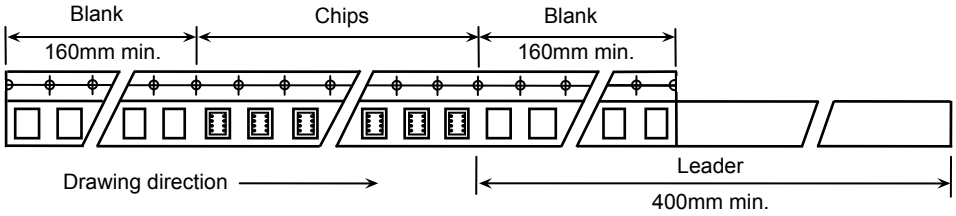
13. TAPE PACKAGING SPECIFICATION

1. CONSTRUCTION AND DIMENSION OF TAPING

1-1. Dimensions of carrier tape

Dimensions of plastic tape shall be according to Appendix 3.

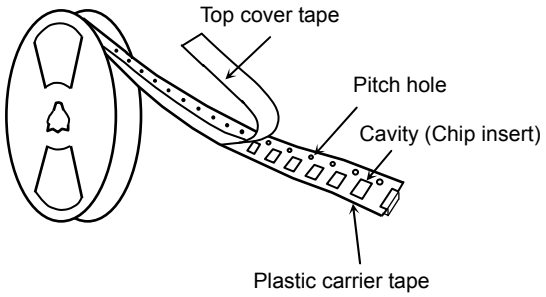
1-2. Trailer and leader of carrier tape



1-3. Dimensions of taping reel

Dimensions of 178mm diameter reel shall be according to Appendix 4.
Dimensions of 330mm diameter reel shall be according to Appendix 5.

1-4. Structure of taping



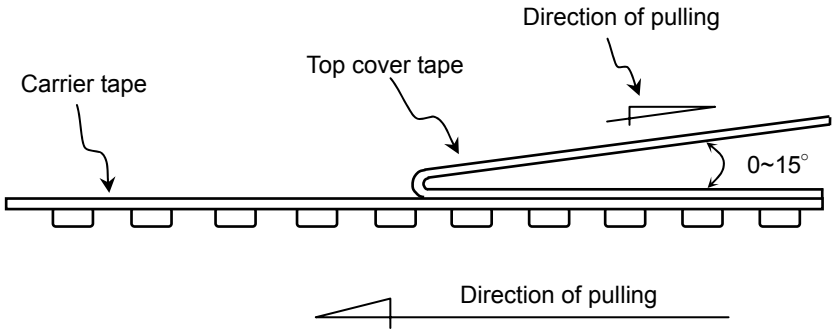
2. CHIP QUANTITY

Type	Taping Material	Chip quantity (pcs.)	
		Ø178mm reel	Ø330mm reel
CLLC1A (CC0603)	Plastic	4,000	10,000
CLLE1A (CC0805)	Plastic	4,000	10,000
CLLG1A (CC0805)	Plastic	4,000	10,000

3. PERFORMANCE SPECIFICATIONS

3-1. Peel back strength (top cover tape)

0.05-0.7N. (See the following figure.)



3-2. Carrier tape shall be flexible enough to be wound around a minimum radius of 30mm with components in tape.

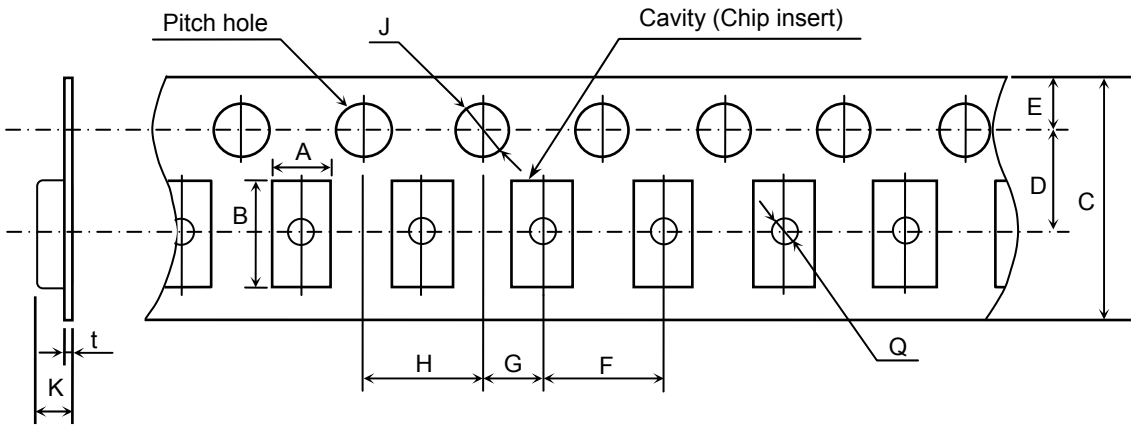
3-3. The number of components missing shall be less than 0.1%

3-4. Components shall not stick to top cover tape.

3-5. The top cover tape shall not protrude beyond the edges of the carrier tape not shall cover the sprocket holes.

Appendix 3

Plastic tape



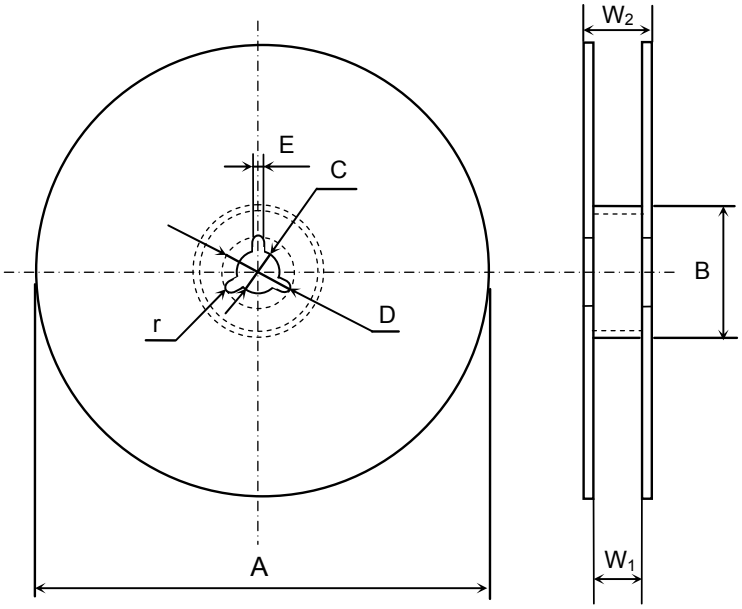
(Unit: mm)

Symbol / Type	A	B	C	D	E	F
CLLC1A	1.1 ± 0.2	1.9 ± 0.2	8.0 ± 0.3	3.5 ± 0.05	1.75 ± 0.1	4.0 ± 0.1
CLLE1A	1.5 ± 0.2	2.3 ± 0.2				
CLLG1A	1.9 ± 0.2	3.5 ± 0.2				

Symbol / Type	G	H	J	K	t	Q
CLLC1A	2.0 ± 0.05	4.0 ± 0.1	Ø1.5 $^{+0.1}_{0}$	2.5 max.	0.3 max.	Ø0.5 min.
CLLE1A						
CLLG1A						

Appendix 4

Reel material: Polystyrene



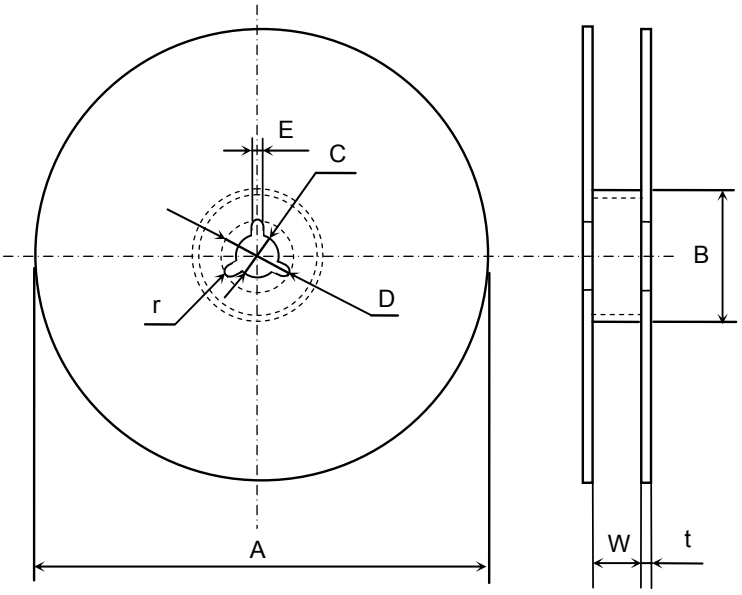
(Unit: mm)

Symbol	A	B	C	D	E	W1
Dimension	Ø178 ± 2.0	Ø60 ± 2.0	Ø13 ± 0.5	Ø21 ± 0.8	2.0 ± 0.5	9.0 ± 0.3

Symbol	W2	r
Dimension	13.0 ± 1.4	1.0

Appendix 5

Reel material: Polystyrene



(Unit: mm)

Symbol	A	B	C	D	E	W
Dimension	Ø382 max. (Nominal Ø330)	Ø50 min.	Ø13 ± 0.5	Ø21 ± 0.8	2.0 ± 0.5	10.0 ± 1.5

Symbol	t	r
Dimension	2.0 ± 0.5	1.0