

# FSTD3306

## 2-Bit Low-Power Bus Switch with Level Shifting

### Features

- Typical 3Ω switch resistance at 5.0V  $V_{CC}$ ,  $V_{IN} = 0V$
- Level shift facilitates 5V to 3.3V interfacing
- Minimal propagation delay through the switch
- Power down high impedance input/output
- Zero bounce in flow-through mode
- TTL compatible active LOW control inputs
- Control inputs are over-voltage tolerant

### Description

The FSTD3306 is a 2-bit ultra high-speed CMOS FET bus switch with enhanced level-shifting circuitry and TTL-compatible active LOW control inputs. The low on resistance of the switch allows inputs to be connected to outputs with minimal propagation delay and without generating additional ground bounce noise. The device is organized as a 2-bit switch with independent bus-enable ( $\overline{BE}$ ) controls. When  $\overline{BE}$  is LOW, the switch is ON and Port A is connected to Port B. When  $\overline{BE}$  is HIGH, the switch is OPEN and a high-impedance state exists between the two ports. Reduced voltage drive to the gate of the FET switch permits nominal level shifting of 5V to 3V through the switch. Control inputs tolerate voltages up to 5.5V independent of  $V_{CC}$ .

### Ordering Information

Part Number	Top Mark	Package	Pb-Free	Operating Temperature Range	Packing Method
FSTD3306MTCX	FD3306	8-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 4.4mm Wide	Yes	-40 to +85°C	Tape & Reel
FSTD3306MTC	FD3306	8-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 4.4mm Wide	Yes	-40 to +85°C	Tube
FSTD3306L8X	TD	8-Lead MicroPak™	Yes	-40 to +85°C	5000 units on Reel

### Logic Diagram

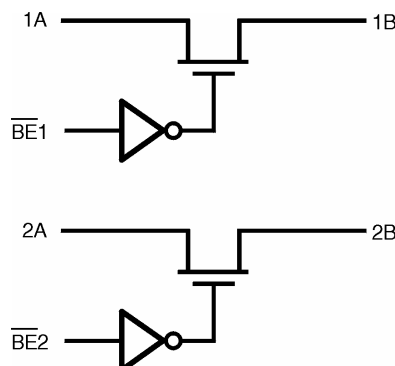


Figure 1. Logical Connections for the FSTD3306

## Connections Diagram

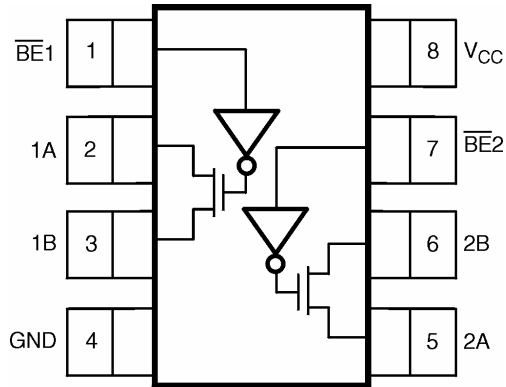


Figure 2. TSSOP Pin Outs (Top View)

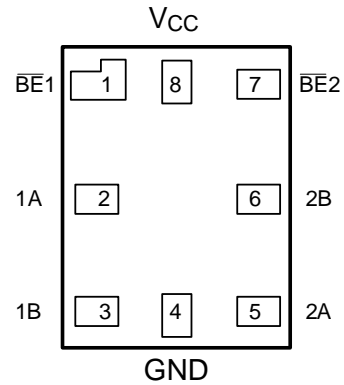


Figure 3. MicroPak Pin Outs (Top View)

## Pin Definitions

Pin	Description
A	Bus A switch I/O
B	Bus B switch I/O
$\overline{BE}$	Bus enable input

## Function Table

Bus Enable Input ( $\overline{BE}$ )	Function
LOW Logic Level	B connected to A
HIGH Logic Level	Disconnected

## Absolute Maximum Ratings

The “Absolute Maximum Ratings” are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the Electrical Characteristics tables are not guaranteed at the absolute maximum ratings. The “Recommended Operating Conditions” table defines the conditions for actual device operation.

Symbol	Parameter	Condition	Min.	Typ.	Max	Unit
V <sub>CC</sub>	Supply Voltage		- 0.5		+ 7.0	V
V <sub>S</sub>	DC Switch Voltage		- 0.5		+ 7.0	V
V <sub>IN</sub>	DC Output Voltage <sup>(1)</sup>		- 0.5		+ 7.0	V
I <sub>IK</sub>	DC Input Diode Current	V <sub>IN</sub> < 0V		- 50		mA
I <sub>OUT</sub>	DC Output Sink Current			128		mA
I <sub>CC</sub> /I <sub>GND</sub>	DC V <sub>CC</sub> or Ground Current			± 100		mA
T <sub>STG</sub>	Storage Temperature Range		- 65		+150	°C
T <sub>J</sub>	Junction Temperature	under Bias		+ 150		°C
T <sub>L</sub>	Junction Lead Temperature	(Soldering, 10 Seconds)		+ 260		°C
P <sub>D</sub>	Power Dissipation	at +85°C		250		mW

**Notes:**

1. The input and output negative voltage ratings may be exceeded if the input and output diode current ratings are observed.

## Recommended Operating Conditions<sup>(2)</sup>

Symbol	Parameter	Condition	Min.	Typ.	Max	Unit
V <sub>CC</sub>	Supply Voltage		4.5		5.5	V
V <sub>IN</sub>	Control Input Voltage		0.0		5.5	V
V <sub>IN</sub>	Switch Input Voltage		0.0		5.5	V
V <sub>OUT</sub>	Switch Output Voltage		0.0		5.5	V
T <sub>A</sub>	Operating Temperature		- 40		+ 85	°C
t <sub>r</sub> , t <sub>f</sub>	Input Rise and Fall Time	Control Input	0		5	ns/V
		Switch I/O	0		DC	ns/V
Θ <sub>JA</sub>	Thermal Resistance			250		°C/W

**Notes:**

2. Unused logic inputs must be held HIGH or LOW. They may not float.

## DC Electrical Characteristics

Ambient temperature ( $T_A$ ) is  $-40^\circ\text{C}$  to  $+85^\circ$  unless otherwise specified.

Symbol	Parameters	Conditions	$V_{CC}$ (V)	Min.	Typ.	Max.	Unit
$V_{IK}$	Clamp Diode Voltage	$I_{IN} = -18\text{ mA}$	4.5			-1.2	V
$V_{IH}$	HIGH-Level Input Voltage		4.5-5.5	2.0			V
$V_{IL}$	LOW-Level Input Voltage		4.5-5.5			0.8	V
$V_{OH}$	HIGH-Level Output Voltage	$V_{IN} = V_{CC}$	4.5-5.5		(3)		V
$I_{IN}$	Input Leakage Current	$0 \leq V_{IN} \leq 5.5\text{V}$	5.5			$\pm 1.0$	$\mu\text{A}$
$I_{OFF}$	Power OFF Leakage Current	$0 \leq A, B \leq V_{CC}$	5.5			$\pm 1.0$	$\mu\text{A}$
$R_{ON}$	Switch On Resistance <sup>(4)</sup>	$V_{IN} = 0\text{V}, I_{IN} = 64\text{mA}$	4.5		3	7	$\Omega$
		$V_{IN} = 0\text{V}, I_{IN} = 30\text{mA}$	4.5		3	7	$\Omega$
		$V_{IN} = 2.4\text{V}, I_{IN} = 15\text{mA}$	4.5		15	50	$\Omega$
$I_{CC}$	Quiescent Supply Current	$V_{IN} = V_{CC}$ or GND, $I_{OUT} = 0$ $\overline{BE} 1 = \overline{BE} 2 = \text{GND}$	5.5		1.1	1.5	$\text{mA}$
		$V_{IN} = V_{CC}$ or GND, $I_{OUT} = 0$ $\overline{BE} 1 = \overline{BE} 2 = V_{CC}$	5.5			10	$\mu\text{A}$
$\Delta I_{CC}$	Increase in $I_{CC}$ per Input <sup>(5)</sup>	$V_{IN} = 3.4\text{V}, I_O = 0$ , one control input only, other $\overline{BE} = V_{CC}$	5.5		1	2.5	$\text{mA}$

### Notes:

- For typical DC characteristics, see Figures 7-9.
- Measured by the voltage drop between A and B pins at the indicated current through the switch. On resistance is determined by the lower of the voltages on the two (A or B) pins.
- Increase per TTL-driven input ( $V_{IN} = 3.4\text{V}$ , control input only). A and B pins do not contribute to  $I_{CC}$ .

## AC Electrical Characteristics

Ambient temperature ( $T_A$ ) is  $-40^\circ\text{C}$  to  $+85^\circ$  and  $C_L = 50\text{pF}$ ,  $R_U = R_D = 500\Omega$  unless otherwise specified.

Symbol	Parameter	Conditions	$V_{CC}$ (V)	Min.	Typ.	Max.	Unit
$t_{PHL}, t_{PLH}$	Propagation Delay Bus-to-Bus <sup>(6)</sup>	$V_I = \text{OPEN}$	4.5 - 5.5			0.25	ns
$t_{PZL}, t_{PZH}$	Output Enable Time	$V_I = 7\text{V}$ for $t_{PZL}$ , $V_I = 0\text{V}$ for $t_{PZH}$	4.5 - 5.5	1.0	3.5	5.8	ns
$t_{PLZ}, t_{PHZ}$	Output Disable Time	$V_I = 7\text{V}$ for $t_{PLZ}$ , $V_I = 0\text{V}$ for $t_{PHZ}$	4.5 - 5.5	0.8	3.5	4.8	ns

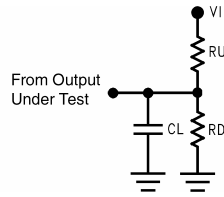
### Notes:

- This parameter is guaranteed. The bus switch contributes no propagation delay other than the RC delay of the typical on resistance of the switch and the 50pF load capacitance when driven by an ideal voltage source (zero output impedance). The specified limit is calculated on this basis.

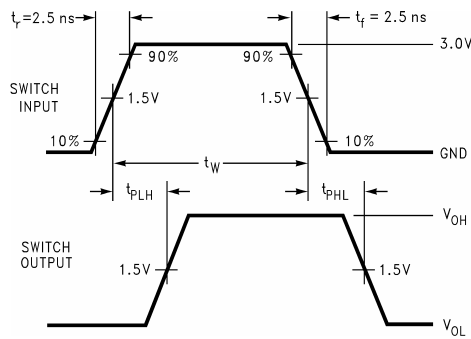
## Capacitance

Symbol	Parameter	Conditions	Typ.	Unit
$C_{IN}$	Control Pin Input Capacitance	$V_{CC} = 0\text{V}$	2.5	pF
$C_{I/O} (\text{OFF})$	Port OFF Capacitance	$V_{CC} = 5.0\text{V} = \overline{BE}$	6	pF
$C_{I/O} (\text{ON})$	Port ON Capacitance	$V_{CC} = 5.0\text{V}, \overline{BE} = 0\text{V}$	12	pF

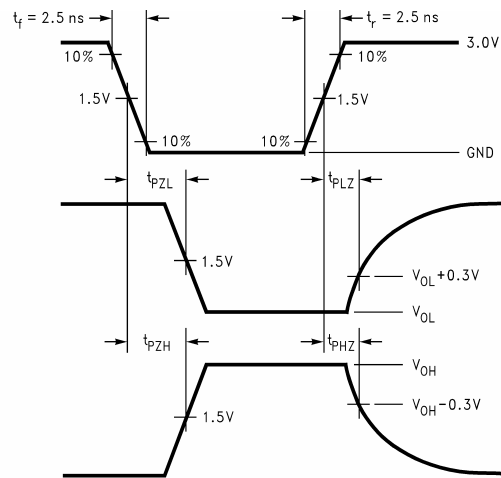
## AC Loading and Waveforms



**Figure 4. AC Test Circuit.** Input driven by 50Ω source-terminated in 50Ω.  $C_L$  includes load and stray capacitance. Input PRR = 1.0 MHz;  $T_W = 500\text{ns}$ .



**Figure 5. AC Waveform**



**Figure 6. AC Waveform**

## DC Characteristics

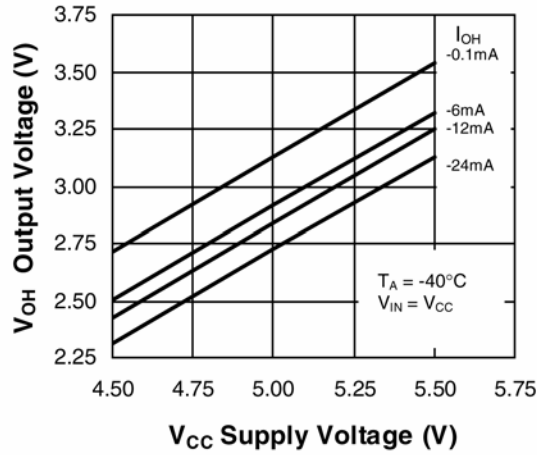


Figure 7. Typical High-Level Output Voltage vs. Supply Voltage ( $T_A = -40^\circ\text{C}$ ,  $V_{IN} = V_{CC}$ )

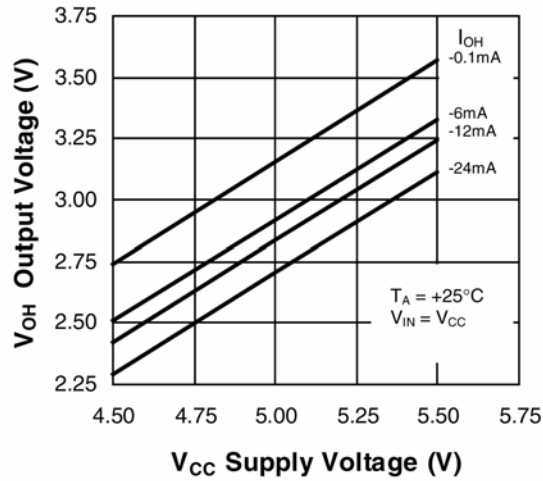


Figure 8. Typical High-Level Output Voltage vs. Supply Voltage ( $T_A = 25^\circ\text{C}$ ,  $V_{IN} = V_{CC}$ )

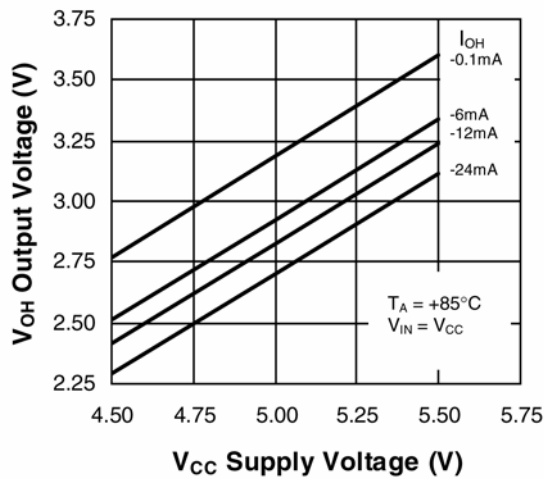


Figure 9. Typical High-Level Output Voltage vs. Supply Voltage ( $T_A = 85^\circ\text{C}$ ,  $V_{IN} = V_{CC}$ )

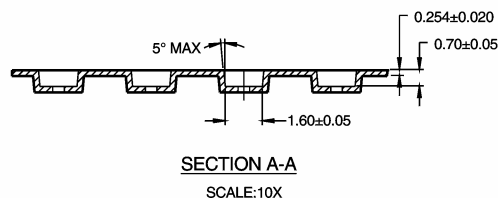
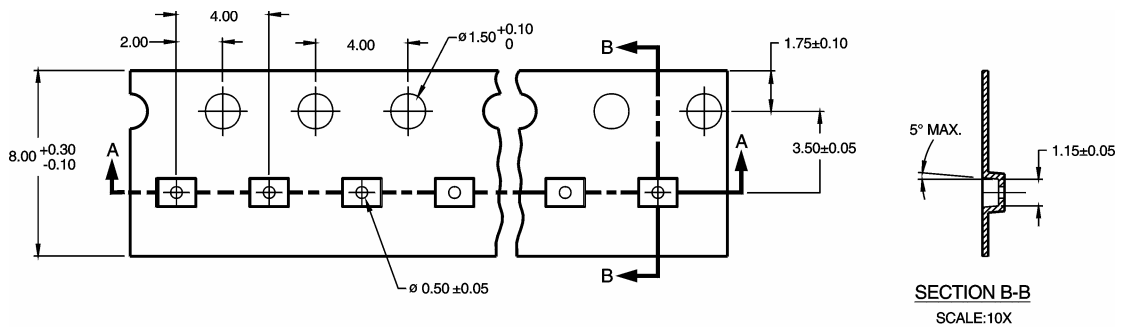
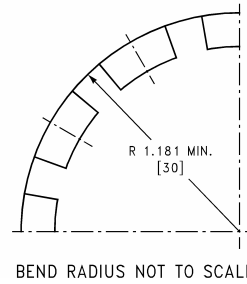
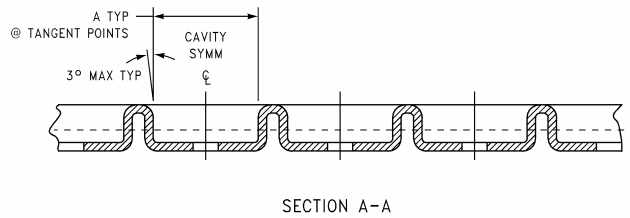
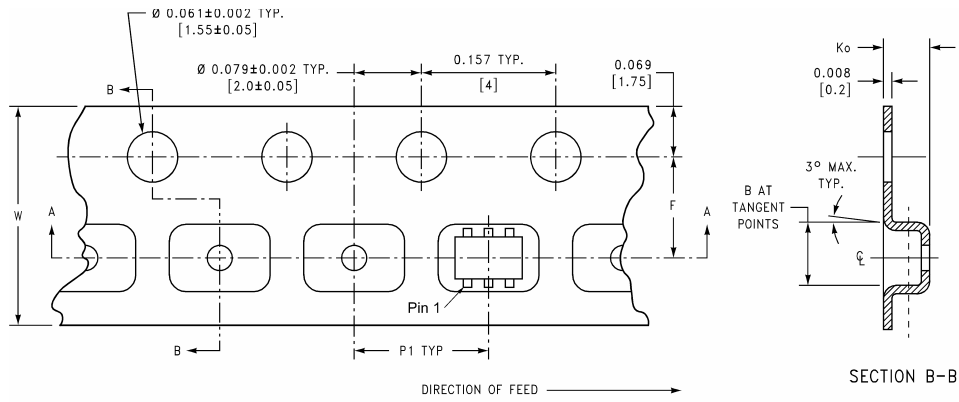
## Tape and Reel Specifications

### Tape Format MicroPak

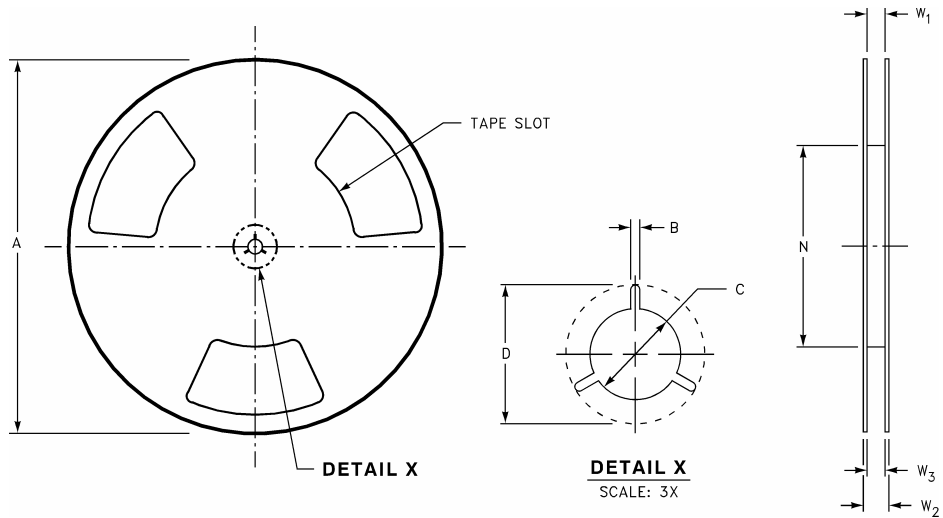
Package Designator	Tape Section	Number Cavities	Cavity Status	Cover Tape Status
L8X	Leader (Start End)	125 (typ.)	Empty	Sealed
	Carrier	5000	Filled	Sealed
	Trailer (Hub End)	75 (typ.)	Empty	Sealed

### Tape Dimensions

Dimensions are in millimeters unless otherwise noted.



### Reel Dimensions

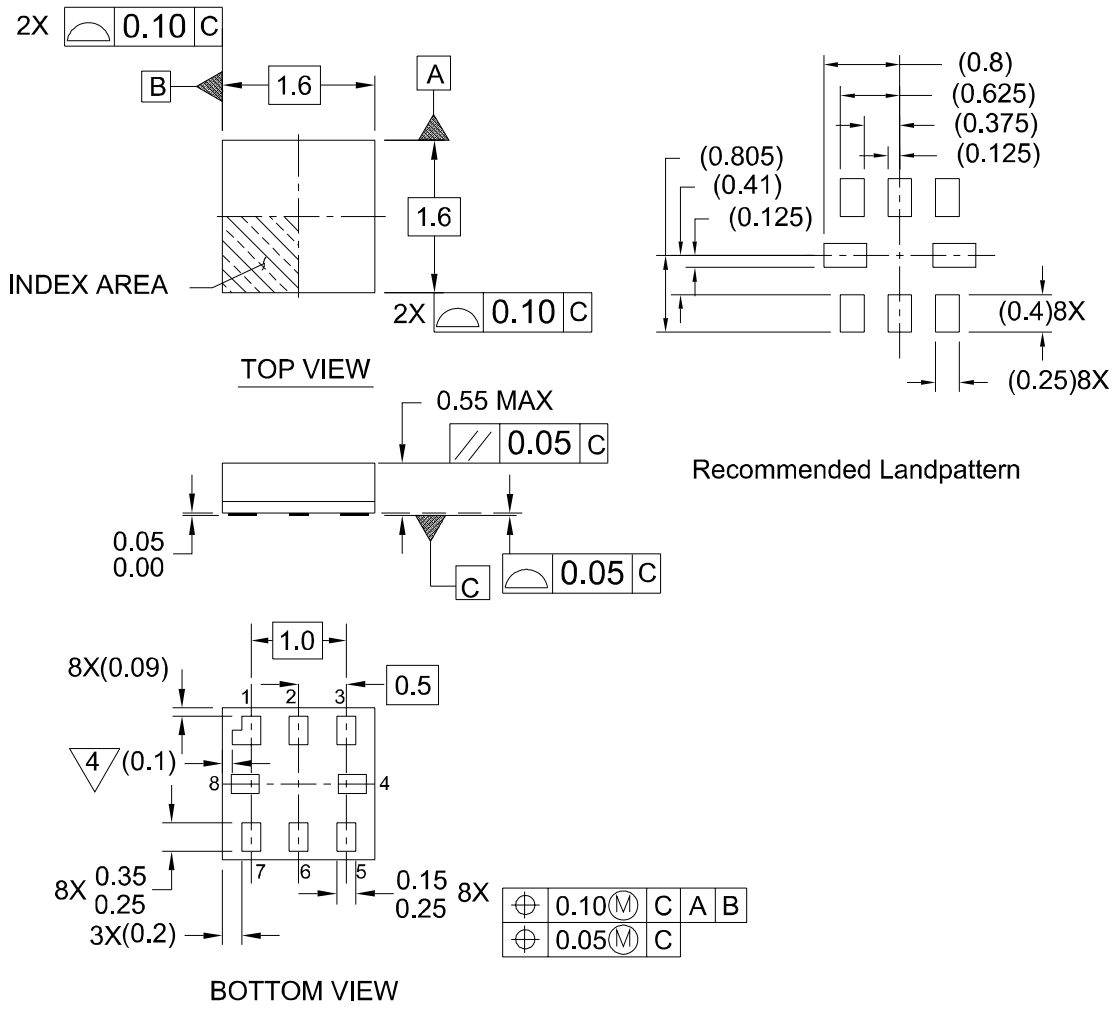


Tape Size	A	B	C	D	N	W1	W2	W23
8mm	7.0 (177.8)	0.059 (1.50)	0.512 (13.00)	0.795 (20.20)	2.165 (55.00)	.0331 +0.059 / -0.000 (8.40 +1.50 / -0.00)	0.567 (14.40)	W1 +0.078 / -0.039 (W1 +2.00 / -1.00)



## Physical Dimensions

Dimensions are in millimeters unless otherwise noted.



**Notes:**

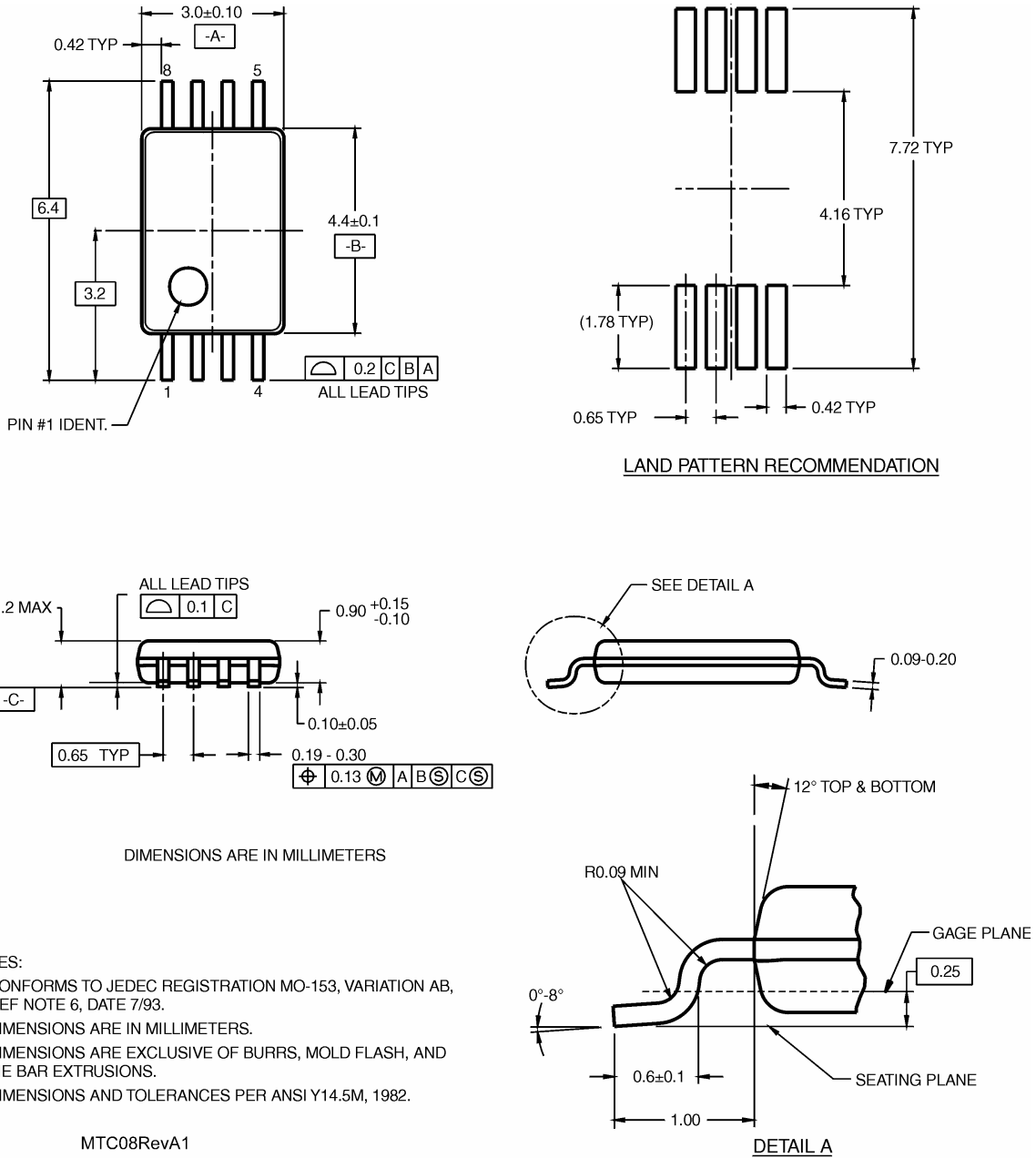
1. PACKAGE CONFORMS TO JEDEC MO-255 VARIATION UAAD
2. DIMENSIONS ARE IN MILLIMETERS
3. DRAWING CONFORMS TO ASME Y.14M-1994
4. PIN 1 FLAG, END OF PACKAGE OFFSET.

MAC08AREVC

**Figure 10. 8-Lead MicroPak, 1.6mm-wide Package**

## Physical Dimensions

Dimensions are in millimeters unless otherwise noted.



**Figure 11. 8-Lead Thin Shrink Small Outline (TSSOP), JEDEC MO-153, 4.4mm-wide Package**

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FACT™	MicroFET™	QS™	TCM™	Wire™
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Rev. I20