

PROTECTION PRODUCTS - RailClamp®

Description

RailClamp® TVS diodes are ultra low capacitance devices designed to protect sensitive electronics from damage or latch-up due to ESD, EFT, and EOS. They are designed for use on high speed ports in applications such as cell phones, notebook computers, and other portable electronics. These devices offer desirable characteristics for board level protection including fast response time, low operating and clamping voltage, and no device degradation.

RClamp®3331ZA features extremely good ESD protection characteristics including a low typical dynamic resistance of 0.20 Ohms, low peak ESD clamping voltage, and high ESD withstand voltage (+/-18kV contact per IEC 61000-4-2). Low typical capacitance (0.35pF at VR=0V) allows the RClamp3331ZA to be used in applications operating in excess of 5GHz without appreciable signal attenuation. Each device will protect one high speed data line operating at 3.3 Volts.

RClamp3331ZA is in a 2-pin SLP0603P2X3F package measuring 0.6 x 0.3 mm with a nominal height of 0.25mm. Leads are finished with lead-free NiAu. The small package gives the designer the flexibility to protect single lines in applications where arrays are not practical. The combination of low peak ESD clamping, low dynamic resistance, and low capacitance makes this device suitable for applications such as USB 3.0, MIPI and V-By-One interfaces in portable devices.

Features

- ◆ High ESD withstand Voltage: +/-**18kV** (Contact/Air) per **IEC 61000-4-2**
- ◆ Able to withstand over 1000 ESD strikes per IEC 61000-4-2 Level 4
- ◆ Ultra-small **0201 package**
- ◆ Protects one high speed data line
- ◆ Working voltage: +/- 3.3V
- ◆ Low capacitance: **0.35pF typical**
- ◆ Extremely low dynamic resistance: **0.20 Ohms (Typ)**
- ◆ Low ESD clamping voltage
- ◆ Solid-state silicon-avalanche technology

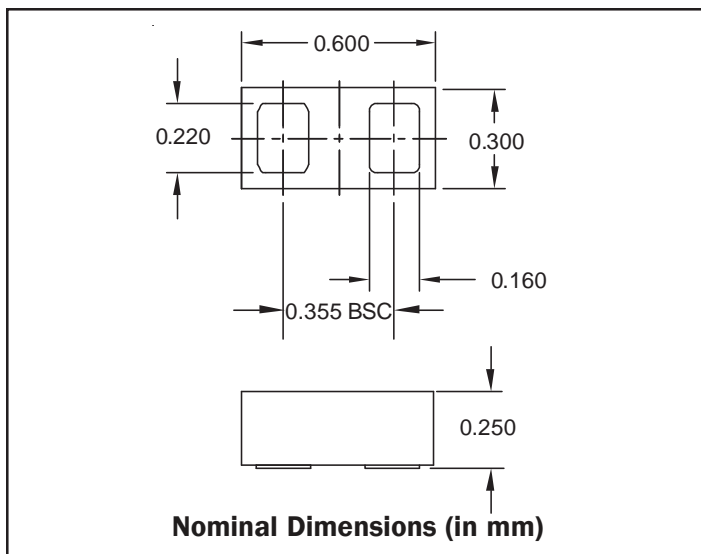
Mechanical Characteristics

- ◆ SLP0603P2X3F Package
- ◆ Pb-Free, Halogen Free, RoHS/WEEE Compliant
- ◆ Nominal Dimensions: 0.6 x 0.3 x 0.25 mm
- ◆ Lead Finish: NiAu
- ◆ Marking: Marking Code
- ◆ Packaging: Tape and Reel

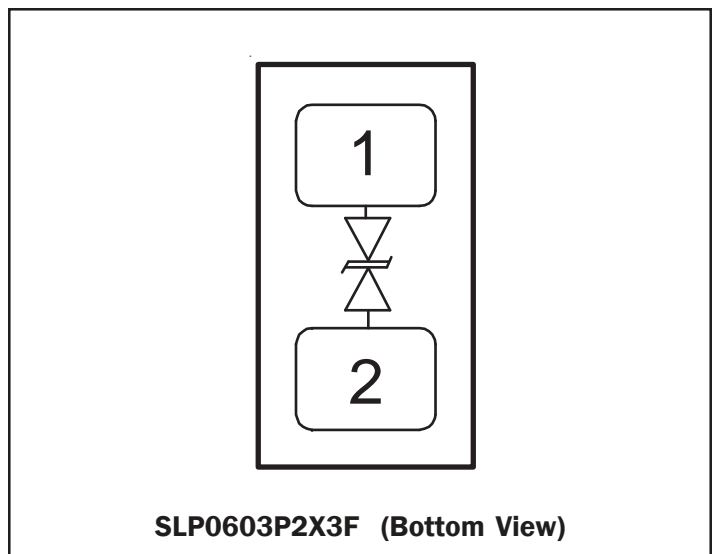
Applications

- ◆ USB 2.0 / USB 3.0
- ◆ MIPI / MDDI
- ◆ V-By-One
- ◆ eDP
- ◆ MHL
- ◆ LVDS

Nominal Dimensions



Schematic



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Absolute Maximum Rating

Rating	Symbol	Value	Units
Peak Pulse Power (tp = 8/20μs)	P_{pk}	30	Watts
Maximum Peak Pulse Current (tp = 8/20μs)	I_{pp}	4	Amps
ESD per IEC 61000-4-2 (Air) ¹ ESD per IEC 61000-4-2 (Contact) ¹	V_{ESD}	+/- 18 +/- 18	kV
Operating Temperature	T_J	-40 to +85	°C
Storage Temperature	T_{STG}	-55 to +150	°C

Electrical Characteristics (T=25°C)

Parameter	Symbol	Conditions	Minimum	Typical	Maximum	Units
Reverse Stand-Off Voltage	V_{RWM}	Pin 1 to 2 or 2 to 1			3.3	V
Breakdown Voltage	V_{BR}	$I_{BR} = 10\mu A$ Pin 1 to 2 or 2 to 1	5.5	8	10.5	V
Reverse Leakage Current	I_R	$V_{RWM} = 3.3V, T=25^\circ C$ Pin 1 to 2 or 2 to 1		<1	50	nA
Clamping Voltage	V_C	$I_{pp} = 1A, tp = 8/20\mu s$ Pin 1 to 2 or 2 to 1		3.8	5.5	V
Clamping Voltage	V_C	$I_{pp} = 4A, tp = 8/20\mu s$ Pin 1 to 2 or 2 to 1		5.5	7.5	V
ESD Clamping Voltage ²	V_C	IPP = 4A, t _{lp} = 0.2/100ns		4.5		V
ESD Clamping Voltage ²	V_C	IPP = 16A, t _{lp} = 0.2/100ns		7		V
Dynamic Resistance ^{2,3}	R_D	tp = 0.2/100ns		0.20		Ohms
Junction Capacitance	C_J	$V_R = 0V, f = 1MHz$		0.35	0.45	pF

Notes

1) ESD gun return path connected to ESD ground reference plane.

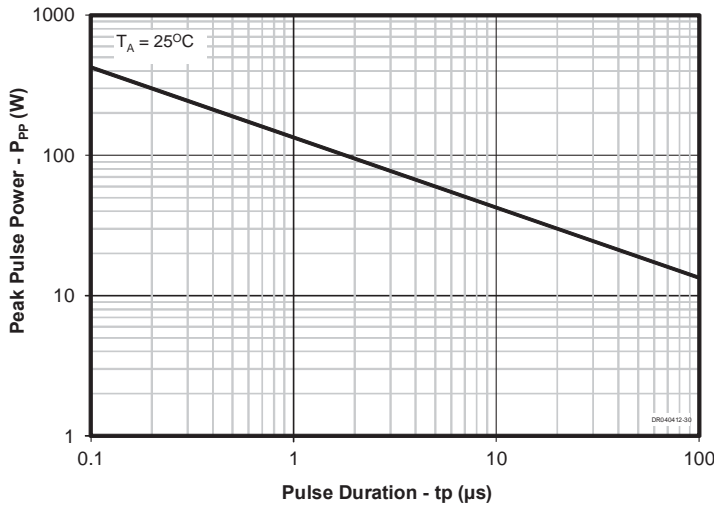
2) Transmission Line Pulse Test (TLP) Settings: $t_p = 100ns, t_r = 0.2ns, I_{TLP}$ and V_{TLP} averaging window: $t_1 = 70ns$ to $t_2 = 90ns$.

3) Dynamic resistance calculated from $I_{TLP} = 4A$ to $I_{TLP} = 16A$

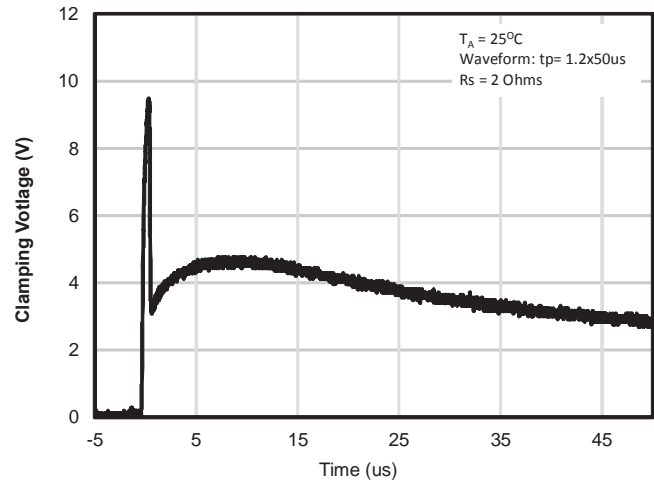
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Typical Characteristics

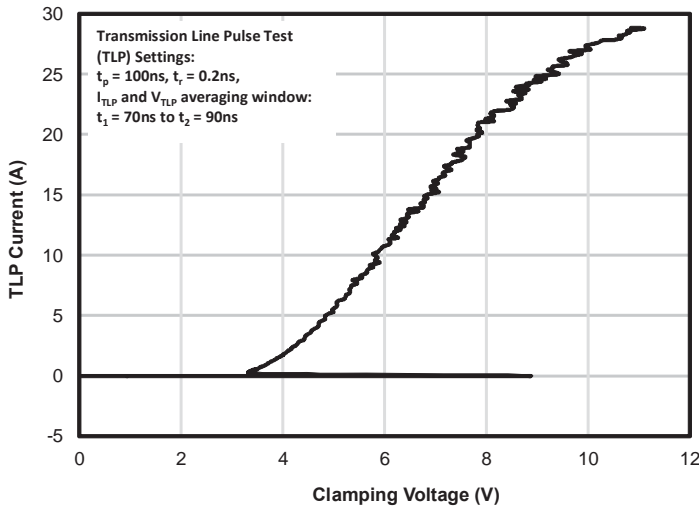
Non-Repetitive Peak Pulse Power vs. Pulse Time



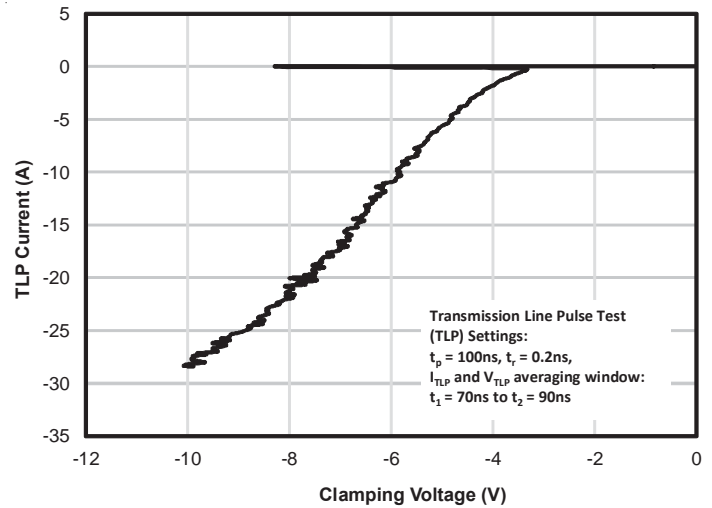
Clamping Waveform (t_p=1.2/50us)



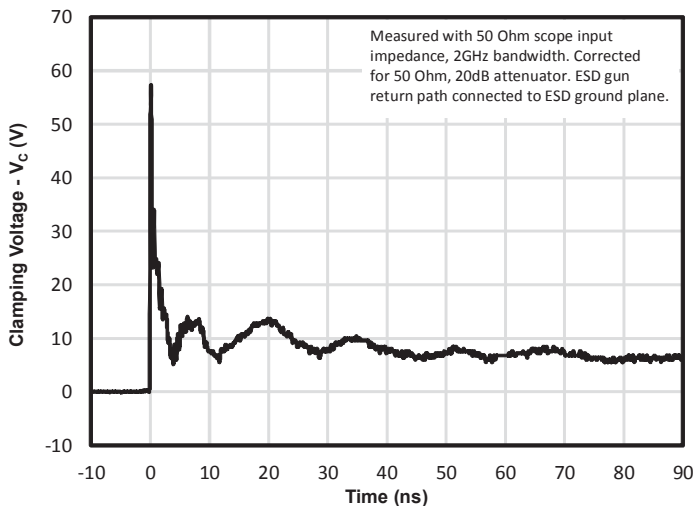
TLP Characteristic (Positive)



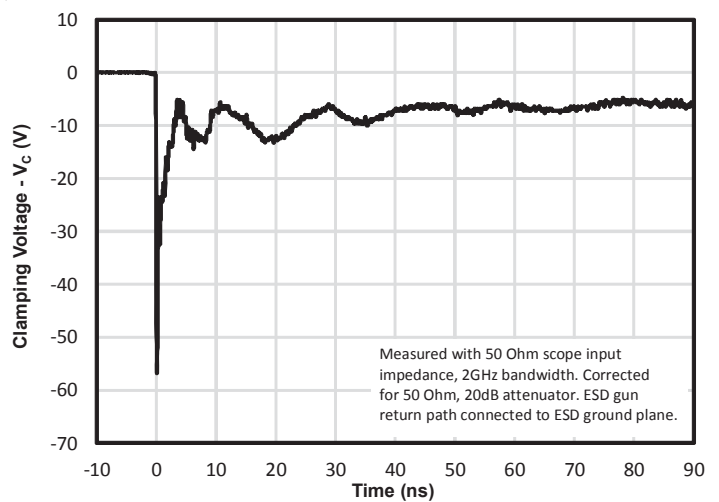
TLP Characteristic (Negative)



ESD Clamping (+8kV Contact per IEC 61000-4-2)



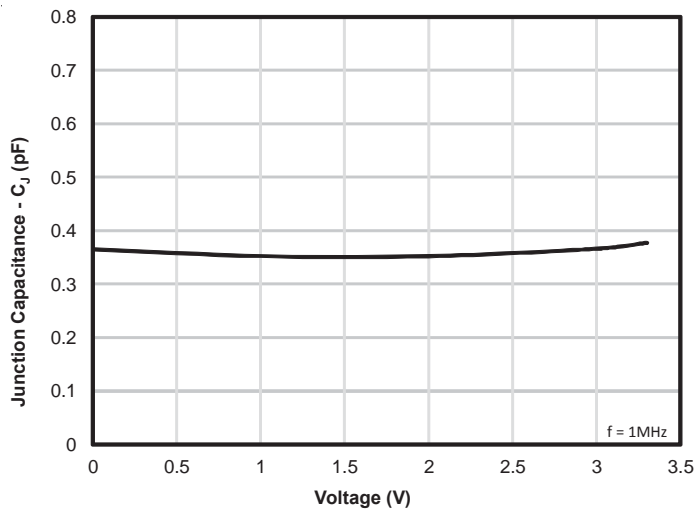
ESD Clamping (-8kV Contact per IEC 61000-4-2)



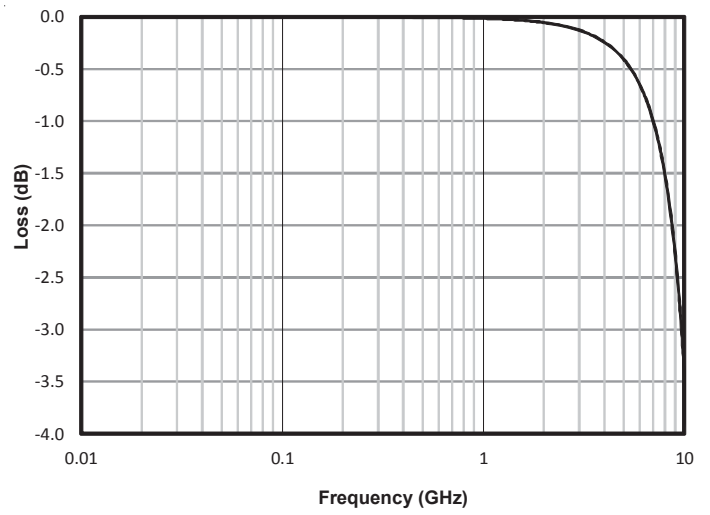
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Typical Characteristics

Junction Capacitance vs. Reverse Voltage



Typical Insertion Loss S21



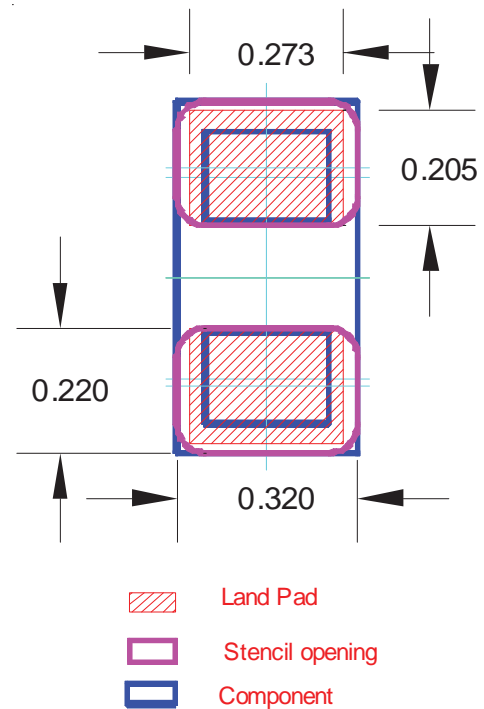
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Applications Information

Assembly Guidelines

The small size of this device means that some care must be taken during the mounting process to insure reliable solder joints. The figure at the right details Semtech's recommended aperture based on the assembly guidelines detailed in the table below. Note that these are only recommendations and should serve only as a starting point for design since there are many factors that affect the assembly process. Exact manufacturing parameters will require some experimentation to get the desired solder application.

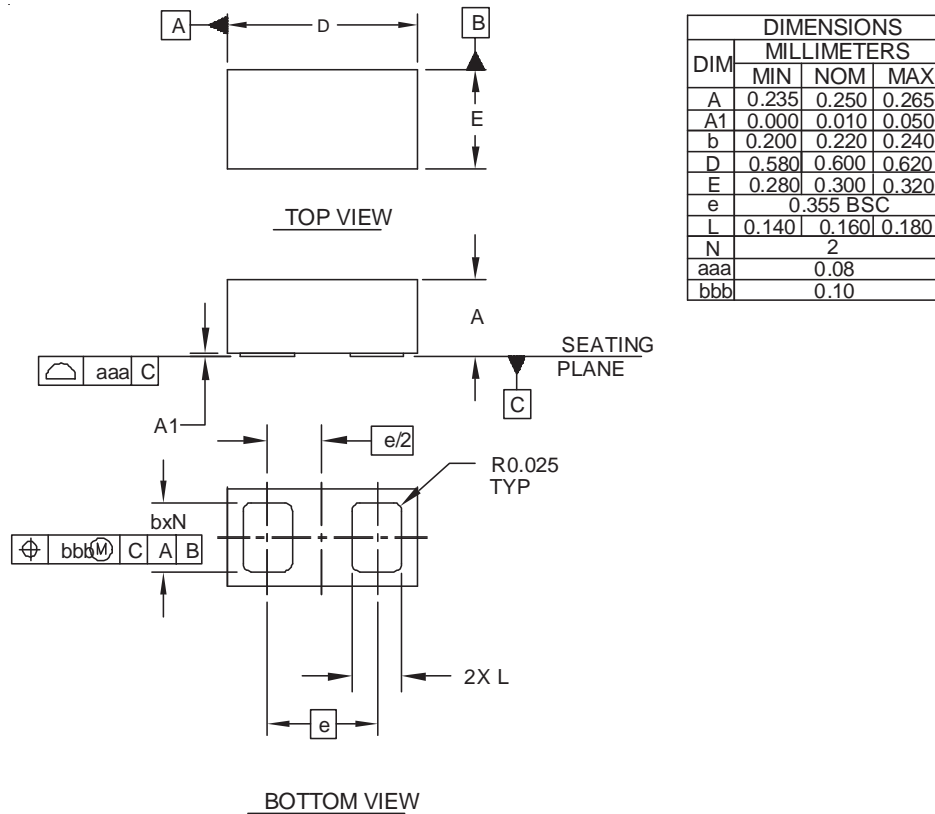
Assembly Parameter	Recommendation
Solder Stencil Design	Laser cut, Electro-polished
Aperture shape	Rectangular with rounded corners
Solder Stencil Thickness	0.100 mm (0.004")
Solder Paste Type	Type 4 size sphere or smaller
Solder Reflow Profile	Per JEDEC J-STD-020
PCB Solder Pad Design	Non-Solder mask defined
PCB Pad Finish	OSP OR NiAu



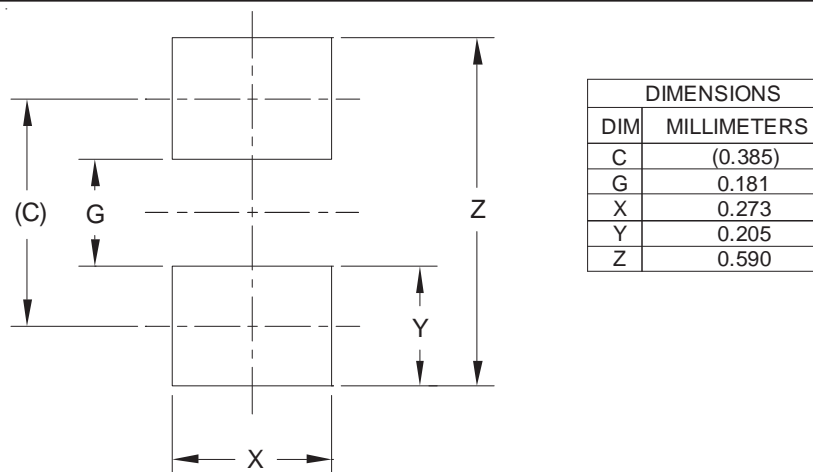
Recommended Mounting Pattern

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Outline Drawing - SLP0603P2X3F



Land Pattern - SLP0603P2X3F



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