RF7244

3V W-CDMA BAND 4 LINEAR PA MODULE

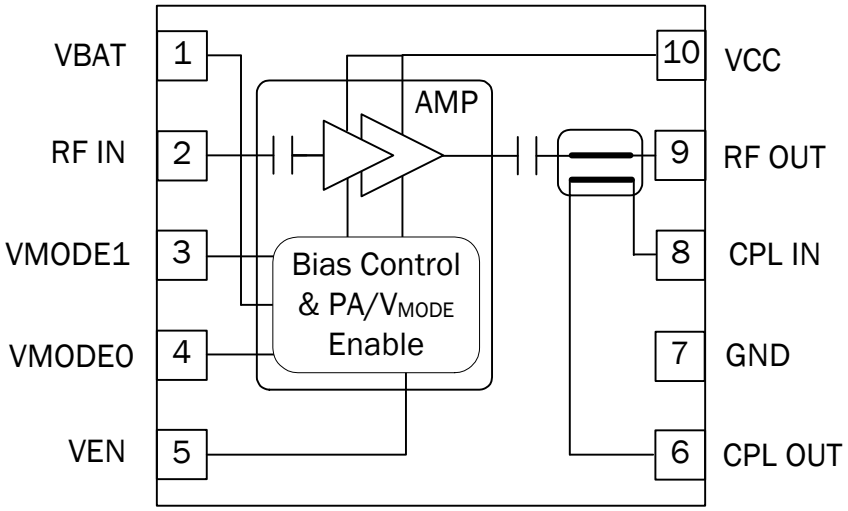
Package Style: Module, 10-Pin, 3mmx3mmx1.0mm

Features

- HSDPA /HSUPA /HSPA+/LTE
- Low Voltage Positive Bias Supply (3.0V to 4.2V)
- +28.25dBm Linear Output Power (+27.25dBm HSDPA and HSPA+)
- High Efficiency Operation 48% at P_{OUT}=+28.25dBm
- Low Quiescent Current in Low Power Mode: 5mA when using DC/Dc converter
- Internal Voltage Regulator Eliminates the Need for External Reference Voltage (V_{REF})
- 3-Mode Power States with Digital Control Interface
- Optimized for DC/DC Converter Operation
- Integrated Power Coupler
- Integrated Blocking and Collector Decoupling Capacitors

Applications

- WCDMA/HSDPA/HSPA+/LTE Wireless Handsets and Data Cards
- Dual-Mode UMTS Wireless Handsets



Functional Block Diagram

Product Description

The RF7244 is a high-power, high-efficiency, linear power amplifier designed for use as the final RF amplifier in 3V, 50Ω W-CDMA mobile cellular equipment and spread-spectrum systems. This PA is developed for UMTS Band 4 which operates in the 1710MHz to 1755MHz frequency band. The RF7244 has two digital control pins to select one of three power modes to optimize performance and current drain at lower power levels. The part also has an integrated directional coupler which eliminates the need for an external discrete coupler at the output. The RF7244 meets the spectral linearity requirements of High Speed Downlink Packet Access (HSDPA), High Speed Uplink Packet Access (HSUPA), and Long Term Evolution (LTE) data transmission and is assembled in a 10-pin, 3mmx3mm module.

Ordering Information

RF7244	3V W-CDMA Band 4 Linear PA Module
RF7244PCBA-410	Fully Assembled Evaluation Board

Optimum Technology Matching® Applied

☐ GaAs HBT	☐ SiGe BiCMOS	☐ GaAs pHEMT	☐ GaN HEMT
☐ GaAs MESFET	☐ Si BiCMOS	☐ Si CMOS	☐ RF MEMS
☑ InGaP HBT	☐ SiGe HBT	☐ Si BJT	☐ LDMOS

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Absolute Maximum Ratings

Parameter	Rating	Unit
Supply Voltage in Standby Mode	6.0	V
Supply Voltage in Idle Mode	6.0	V
Supply Voltage in Operating Mode, 50Ω Load	6.0	V
Supply Voltage, V_{BAT}	6.0	V
Control Voltage, V_{MODE0}, V_{MODE1}	3.5	V
Control Voltage, V_{EN}	3.5	V
RF - Input Power	+10	dBm
RF - Output Power	+30	dBm
Output Load VSWR (Ruggedness)	10:1	
Operating Ambient Temperature	-30 to +110	°C
Storage Temperature	-55 to +150	°C

Caution! ESD sensitive device.

Exceeding any one or a combination of the Absolute Maximum Rating conditions may cause permanent damage to the device. Extended application of Absolute Maximum Rating conditions to the device may reduce device reliability. Specified typical performance or functional operation of the device under Absolute Maximum Rating conditions is not implied.

RoHS status based on EUDirective2002/95/EC (at time of this document revision).

Parameter	Specification			Unit	Condition
	Min.	Typ.	Max.		
Recommended Operating Conditions					
Operating Frequency Range	1710		1755	MHz	
V_{BAT}	+3.0	+3.4	+4.2	V	
V_{CC}	+0.5[1]	+3.4	+4.2	V	
V_{EN}	0		0.5	V	PA disabled.
	1.5	1.8	3.0	V	PA enabled.
V_{MODE0}, V_{MODE1}	0		0.5	V	Logic “low”.
	1.5	1.8	3.0	V	Logic “high”.
P_{OUT}					
Maximum Linear Output (HPM)	28.25[2,3]			dBm	High Power Mode (HPM) V_{CC}=3.4V
Maximum Linear Output (HPM)	28.25[4]			dBm	High Power Mode (HPM) V_{CC}=3.7V
Maximum Linear Output (MPM)	19.0[3]			dBm	Medium Power Mode (MPM) V_{CC}=1.52V
Maximum Linear Output (LPM)	10.0[3]			dBm	Low Power Mode (LPM) V_{CC}=0.83V
Ambient Temperature	-30	+25	+85	°C	

Notes:
1. V_{CC} down to 0.5V may be used for backed-off power when using DC/DC converter to conserve battery current.
2. For operation at V_{CC}=3.0V, derate P_{OUT} by 1.0dB.
3. P_{OUT} is specified for 3GPP (Rel99) modulation. For HSPA+ operation, derate P_{OUT} by 1.0dB:
   HSPA+ Configuration: 3GPP Rel7 Subtest 1.
4. P_{OUT} is specified for 3GPP (HSDPA Sub-test 2 and HSUPA Sub-test 1) modulation.

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Parameter	Specification			Unit	Condition
	Min.	Typ.	Max.		
Electrical Specifications					T=+25°C, V_{BAT}=+3.4V, V_{EN}=+1.8V, 50Ω system, W-CDMA Rel 99 Modulation unless otherwise specified.
Gain		28		dB	HPM, P_{OUT}=28.25dBm, V_{CC}=3.4V
		26		dB	MPM, P_{OUT}≤19.0dBm, V_{CC}=1.52V
		20		dB	LPM, P_{OUT}≤10.0dBm, V_{CC}=0.83V
Gain Linearity		±0.7		dB	HPM, 19.0dBm≤P_{OUT}≤28.0dBm
ACLR - 5MHz Offset		-40		dBc	HPM, P_{OUT}=28.25dBm, V_{CC}=3.4V
		-40		dBc	MPM, P_{OUT}=19.0dBm, V_{CC}=1.52V
		-40		dBc	LPM, P_{OUT}=10.0dBm, V_{CC}=0.83V
ACLR - 10MHz Offset		-52		dBc	HPM, P_{OUT}=28.25dBm, V_{CC}=3.4V
		-60		dBc	MPM, P_{OUT}=19.0dBm, V_{CC}=1.52V
		-60		dBc	LPM, P_{OUT}= 10.0dBm, V_{CC}=0.83V
PAE		48		%	HPM, P_{OUT}=28.25dBm, V_{CC}=3.4V
		38		%	MPM, P_{OUT}=19.0dBm, V_{CC}=1.52V
		23		%	LPM, P_{OUT}=10.0dBm, V_{CC}=0.83V
Current Drain		410		mA	HPM, P_{OUT}=28.25dBm, V_{CC}=3.4V
		138		mA	MPM, P_{OUT}=19.0dBm, V_{CC}=1.52V
		52		mA	LPM, P_{OUT}=10.0dBm, V_{CC}=0.83V
Quiescent Current		45		mA	HPM, DC only
		36		mA	MPM, DC only
		19		mA	LPM, DC only
Enable Current		0.1		mA	Source or sink current. V_{EN}=1.8V.
Mode Current (I_{MODE0}, I_{MODE1})		0.1		mA	Source or sink current. V_{MODE0}, V_{MODE1}=1.8V.
Leakage Current		5.0	15.0	µA	DC only. V_{CC}=V_{BAT}=4.2V, V_{EN}=V_{MODE0}=V_{MODE1}=0.5V.
Noise Power in Receive Band		-145		dBm/Hz	All power modes, measured at duplex offset frequency (FTX+400MHz). Rx: 2110MHz to 2170MHz, P_{OUT}≤28.25dBm
Input Impedance		1.5:1		VSWR	No ext. matching, P_{OUT}≤28.25dBm, all modes.
Harmonic, 2FO		-17		dBm	P_{OUT}≤28.25dBm, all power modes.
Harmonic, 3FO		-26		dBm	P_{OUT}≤28.25dBm, all power modes.
Spurious Output Level			-70	dBc	All spurious, P_{OUT}≤28.25dBm, all conditions, load VSWR≤6:1, all phase angles.
Insertion Phase Shift		±10		°	Phase shift at 19dBm when switching from HPM to MPM and MPM to LPM at 10dBm.
DC Enable Time			10	µS	DC only. Time from V_{EN}=high to stable idle current (90% of steady state value).
RF Rise/Fall Time			6	µS	P_{OUT}≤28.25dBm, all modes. 90% of target, DC settled prior to RF.
Coupling Factor		-20		dB	P_{OUT}≤28.25dBm, all modes.
Coupling Accuracy - Temp/Voltage		±0.5		dB	P_{OUT}≤28.25dBm, all modes. -30°C≤T≤85°C, V_{CC} as required, referenced to 25°C, 3.4V conditions.
Coupling Accuracy - VSWR		±0.25		dB	P_{OUT}≤28.25dBm, all modes, load VSWR=2:1, ±0.25dB accuracy corresponds to 20dB directivity.

Pin	Function	Description
1	VBAT	Supply voltage for bias circuitry.
2	RF IN	RF input internally matched to 50Ω and DC blocked.
3	VMODE1	Digital control input for power mode selection (see Operating Modes truth table).
4	VMODE0	Digital control input for power mode selection (see Operating Modes truth table).
5	VEN	Digital control input for PA enable and disable (see Operating Modes truth table).
6	CPL_OUT	Coupler output.
7	GND	This pin must be grounded.
8	CPL_IN	Coupler input used for cascading couplers in series. Terminate this pin with a 50Ω resistor if not connected to another coupler.
9	RF OUT	RF output internally matched to 50Ω and DC blocked.
10	VCC	Supply voltage for the first and second stage amplifier which can be connected to battery supply or output of DC-DC converter.
Pkg Base	GND	Ground connection. The package backside should be soldered to a topside ground pad connecting to the PCB ground plane with multiple ground vias. The pad should have a low thermal resistance and low electrical impedance to the ground plane.

V_{EN}	V_{MODE0}	V_{MODE1}	V_{BAT}	V_{CC}	Conditions/Comments
Low	Low	Low	3.0V to 4.2V	0.5V to 4.2V	Power down mode
Low	X	X	3.0V to 4.2V	0.5V to 4.2V	Standby Mode
High	Low	Low	3.0V to 4.2V	0.5V to 4.2V	High power mode
High	High	Low	3.0V to 4.2V	0.5V to 4.2V	Medium power mode
High	High	High	3.0V to 4.2V	0.5V to 4.2V	Low power mode

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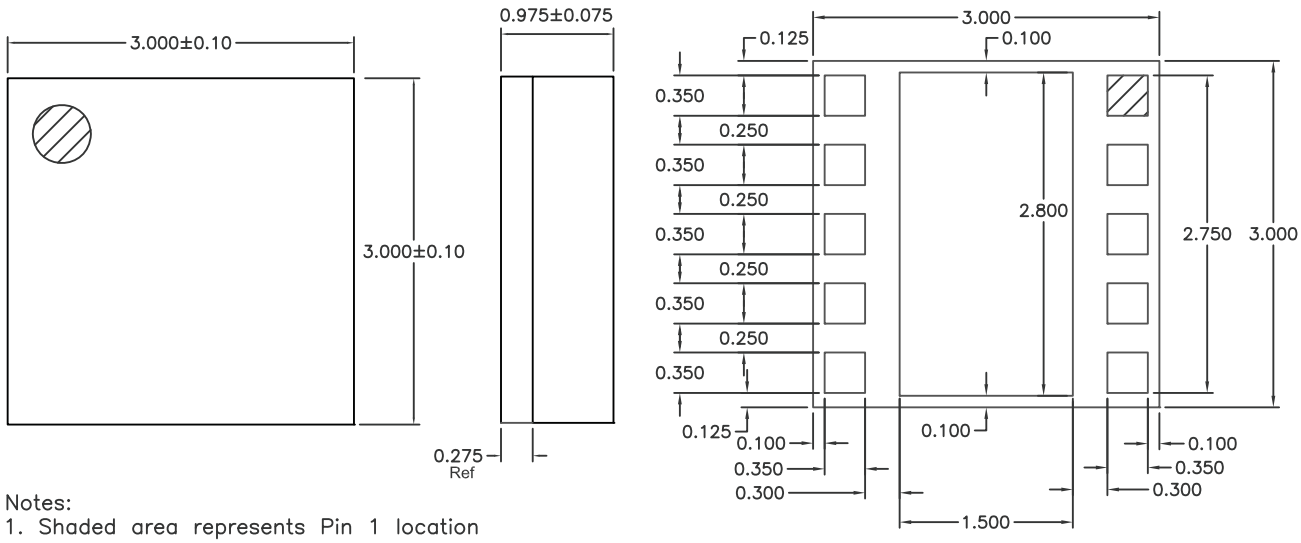
Look Up Table for V_{CC} Optimization

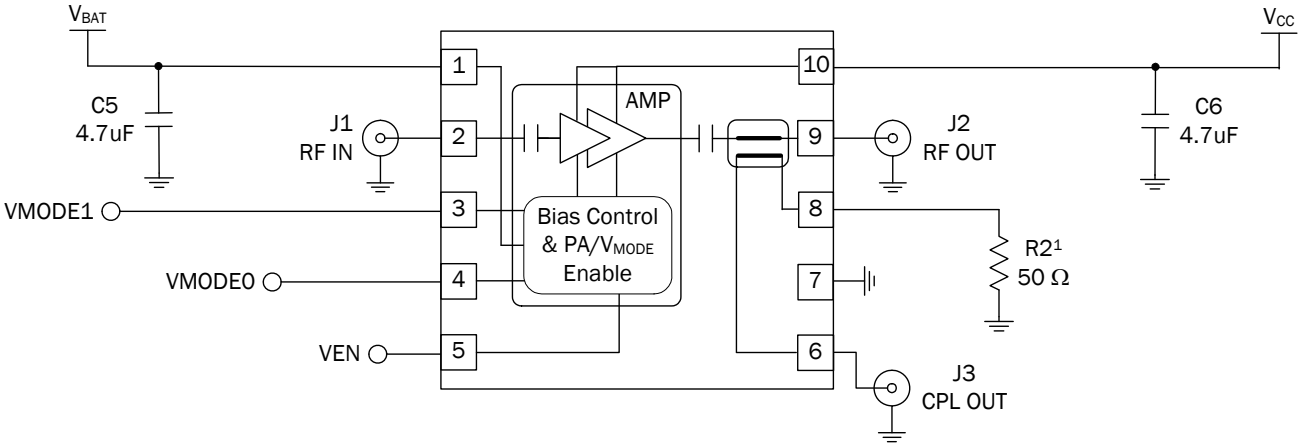
P_{OUT}	HPM V_{CC}	MPM V_{CC}	LPM V_{CC}
28.25	3.4		
28	3.35		
27	3.05		
26	2.81		
25	2.51		
24	2.3		
23	2.11		
22	1.92		
21	1.75		
20	1.59		
19	1.44	1.5	
18	1.31	1.36	
17	1.21	1.25	
16	1.12	1.15	
15	1.05	1.07	
14	0.98	1	
13	0.94	0.94	
12	0.89	0.89	
11	0.84	0.84	0.88
10	0.8	0.8	0.83
9	0.77	0.77	0.78
8	0.74	0.74	0.74
7	0.71	0.72	0.72
6	0.68	0.69	0.69
5	0.65	0.66	0.66
4	0.62	0.63	0.63
3	0.6	0.6	0.6
2	0.58	0.58	0.58
1	0.56	0.56	0.56
0	0.54	0.54	0.54

Package Drawing



Notes:
1. Shaded area represents Pin 1 location

Preliminary Application Schematic



NOTES:
1. The 50 Ω resistor will be removed if pin 8 is connected to another coupler.

PCB Design Requirements

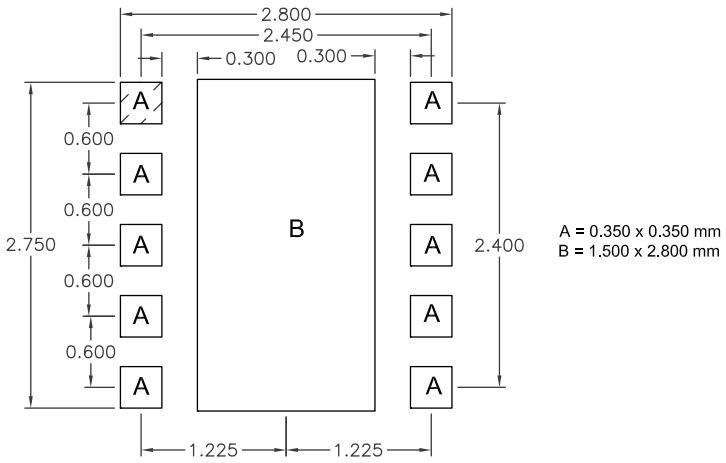
PCB Surface Finish

The PCB surface finish used for RFMD's qualification process is electroless nickel, immersion gold. Typical thickness is 3μinch to 8μinch gold over 180μinch nickel.

PCB Land Pattern Recommendation

PCB land patterns for RFMD components are based on IPC-7351 standards and RFMD empirical data. The pad pattern shown has been developed and tested for optimized assembly at RFMD. The PCB land pattern has been developed to accommodate lead and package tolerances. Since surface mount processes vary from company to company, careful process development is recommended.

PCB Metal Land Pattern



PCB METAL LAND PATTERN

Notes:
1. Shaded area represents Pin 1 location

PCB Metal Land Pattern

PCB Solder Mask Pattern

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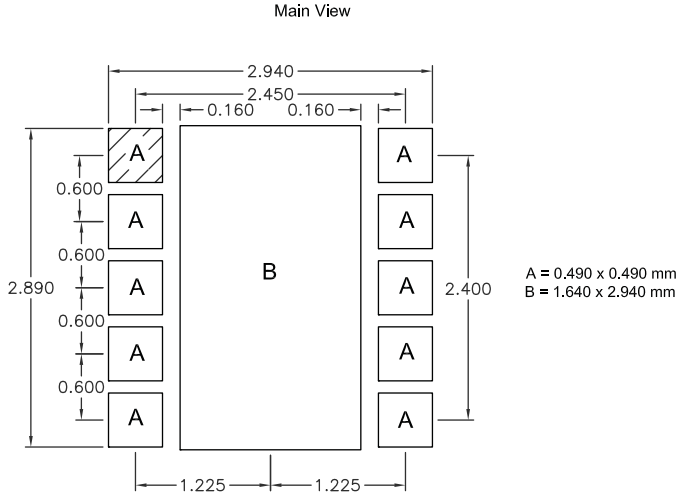
Liquid Photo-Imageable (LPI) solder mask is recommended. The solder mask footprint will match what is shown for the PCB metal land pattern with a 2mil to 3mil expansion to accommodate solder mask registration clearance around all pads. The center-grounding pad shall also have a solder mask clearance. Expansion of the pads to create solder mask clearance can be provided in the master data or requested from the PCB fabrication supplier.



Notes:
1. Shaded area represents Pin 1 location

PCB Solder Mask Pattern

Thermal Pad and Via Design

The PCB land pattern has been designed with a thermal pad that matches the die paddle size on the bottom of the device.

Thermal vias are required in the PCB layout to effectively conduct heat away from the package. The via pattern has been designed to address thermal, power dissipation and electrical requirements of the device as well as accommodating routing strategies.

The via pattern used for the RFMD qualification is based on thru-hole vias with 0.203mm to 0.330mm finished hole size on a 0.5mm to 1.2mm grid pattern with 0.025mm plating on via walls. If micro vias are used in a design, it is suggested that the quantity of vias be increased by a 4:1 ratio to achieve similar results.