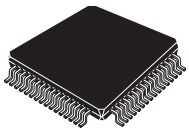
TDA7580

FM/AM digital IF sampling processor

Features

- FM/AM IF sampling DSP
- ON-CHIP analogue to digital converter for 10.7MHz IF signal conversion
- FM channel equalization
- FM adjacent channel suppression
- Reception enhancement in multipath condition
- Stereo decoder and weak signal processing
- 2 Channel serial audio interface (SAI) with sample rate converter
- I^2C and buffer SPI control interfaces
- RDS filter, demodulator & decoder
- Inter processor transport interface for antenna and tuner diversity
- Front-end AGC feedback



LQFP64

Description

The TDA7580 is an integrated circuit implementing an advanced mixed analogue and digital solution, to perform the signal processing of an AM/FM channel. The HW & SW architecture has been devised to perform a digital equalization of the FM/AM channel, and a real rejection of adjacent channels and any other signals, interfering with the listening of the desired station. In severe multiple path conditions, the reception is improved to get high quality audio.

Table 1. Device summary

Part number	Package	Packing
TDA7580	LQFP64	Tube
TDA7580I3TR	LQFP64	Tape and reel

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1 Overview

The algorithm is self-adaptive, thus it requires no “on-the-field” adjustments after the parameters optimization.

The chip embeds a *Band Pass Sigma Delta Analogue to Digital Converter* for 10.7MHz IF conversion from a “tuner device” (the TDA7515 is highly recommended).

The 24bit DSP allows flexibility in the algorithms implementation, thus giving some freedom for customer required features. The total processing power offers a significant headroom for customer’s software requirement, even when the channel equalization and the decoding software is running. the program and data memory space can be loaded from an external non volatile memory via I^2C or SPI.

The oscillator module works with an external 74.1MHz quartz crystal. It has very low electro magnetic interference, as it introduces very low distortion, and in any case harmonics fall outside the radio bandwidth.

The companion tuner device receives the reference clock through a differential ended interface, which works off the oscillator module by properly dividing down the master clock frequency. That allows the overall system saving an additional crystal for the tuner.

After the IF conversion, the digitized baseband signal passes through the base band processing section, either FM or AM, depending on the listener selection. The FM base band processing comprises of stereo decoder, spike detection and noise blanking. The AM noise blanking is fully software implemented.

The internal RDS filter, demodulator and decoder features complete functions to have the output data available through either I^2C or SPI interface. No DSP support is needed but at start-up, so that RDS can work in background and in parallel with other DSP processing. This mode (RDS only) allows current consumption saving for low power application modes.

An I^2C/SPI interface is available for any control and communication with the main micro, as well as RDS data interface. The DSP SPI block embeds a 10 words FIFO for both transmit and receive channels, to lighten the DSP task and frequently respond to the interrupt from the control interface.

Serial audio interface (SAI) is the ideal solution for the audio data transfer, both transmit and receive: either master or slave. The flexibility of this module gives a wide choice of different protocols, including I^2S. Two fully independent bidirectional data channels, with separate clocks allows the use of TDA7580 as general purpose digital audio processor.

A fully asynchronous sample rate converter (ASRC) is available as a peripheral prior to sending audio data out via the SAI, so that internal audio sampling rate (~36kHz and FM/AM mode) can be adapted by upconversion to any external rate.

An inter processor transport interface (HS^3I, high speed synchronous serial interface) is also available for a modular system which implements *Dual Tuner Diversity*, thus enhancing the overall system performance. It is about a synchronous serial interface which exchanges data up to the MPX rate. It has been designed to reduce the electro magnetic interference toward the sensitive analogue signal from the tuner.

General purpose I/O registers are connected to and controlled by the DSP, by means of memory map.

A debug and test interface is available for on chip software debug as well as for internal registers read/write operation.

2 Block diagram and electrical specifications

Figure 1. Block diagram

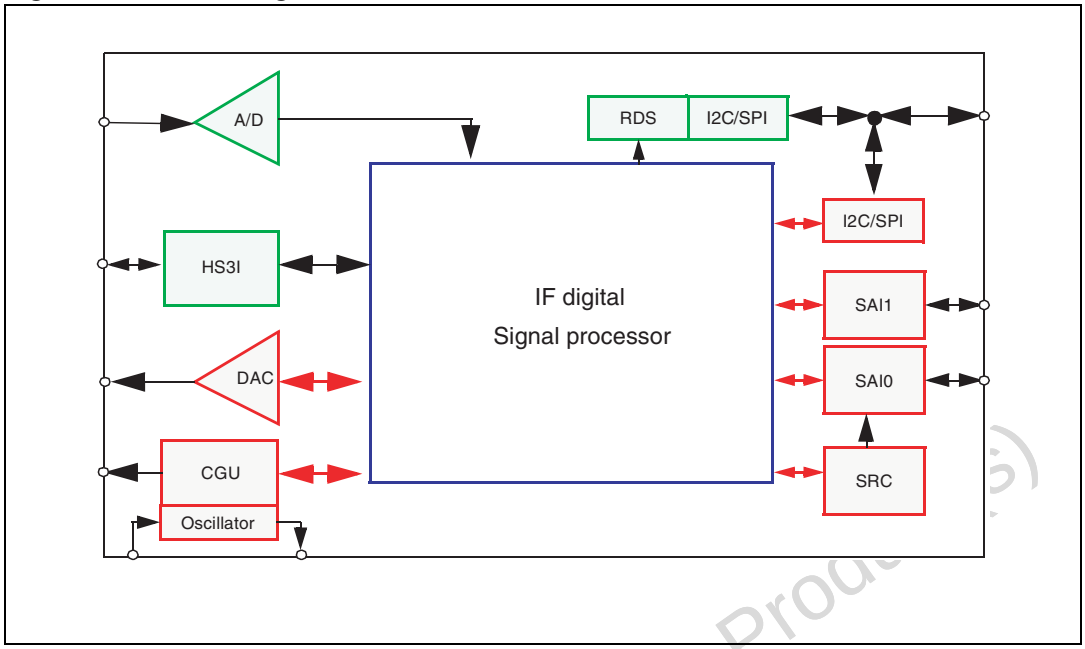


Table 2. Absolute maximum ratings

Symbol	Parameter		Value	Unit
V_{DD} V_{DD3}	Power supplies (1)	Nom. 1.8V Nom. 3.3V	-0.5 to 2.5 -0.5 to 4.0	V V
	Analog input or output voltage belonging to 3.3V IO ring (V_{DDSD}, V_{DDOSC})		-0.5 to 4.0	V
	Digital input or output voltage, 5V tolerant	Normal(2) Failsafe(3)	-0.5 to 6.50 -0.5 to 3.80	V V
	All remaining digital input or output voltage	Nom. 1.8V Nom. 3.3V	-0.5 to (VDD+0.5) -0.5 to (VDD3+0.5)	V
T_j	Operating junction temperature range		-40 to 125	°C
T_{stg}	Storage temperature		-55 to 150	°C

1. V_{DD3} refers to all of the nominal 3.3V power supplies (V_{DDH}, V_{OSC}, V_{DDSD}). V_{DD} refers to all of the nominal 1.8V power supplies (V_{DD}, V_{MTR}).
2. During Normal Mode operation V_{DD3} is always available as specified.
3. During Fail-safe Mode operation V_{DD3} may be not available.

Warning: Operation at or beyond these limits may result in permanent damage to the device. Normal operation is not guaranteed at these extremes.

Table 3. Recommended DC operating conditions (T_j = -40°C to 125°C)

Symbol	Parameter	Comment	Min.	Typ.	Max.	Unit
V_{DD}	1.8V Power supply voltage	Core power supply	1.7	1.80	1.9	V
V_{DDH}	3.3V Power supply voltage (1)	IO Rings power supply (with G_{NDH})	3.15	3.30	3.45	V
V_{OSC}	3.3V Power supply voltage (1)	Oscillator power supply (GND_{OSC})	3.15	3.30	3.45	V
V_{DDSD}	3.3V Power supply voltage (1)	IF ADC power supply (with G_{NDSD})	3.15	3.30	3.45	V
V_{MTR}	1.8V Power supply voltage	DAC keying and tuner clock power supply (with GND_{MTR})	1.7	1.80	1.9	V

1. V_{DDH}, V_{OSC}, V_{DDSD} are also indicated in this document as V_{DD3}. All others as V_{DD}.

Table 4. Thermal data

Symbol	Parameter	Value	Unit
$R_{th\ j\text{-}amb}$	Thermal resistance junction to ambient	68	°C/W

2.1 Pin description

Figure 2. PIN connection (top view)

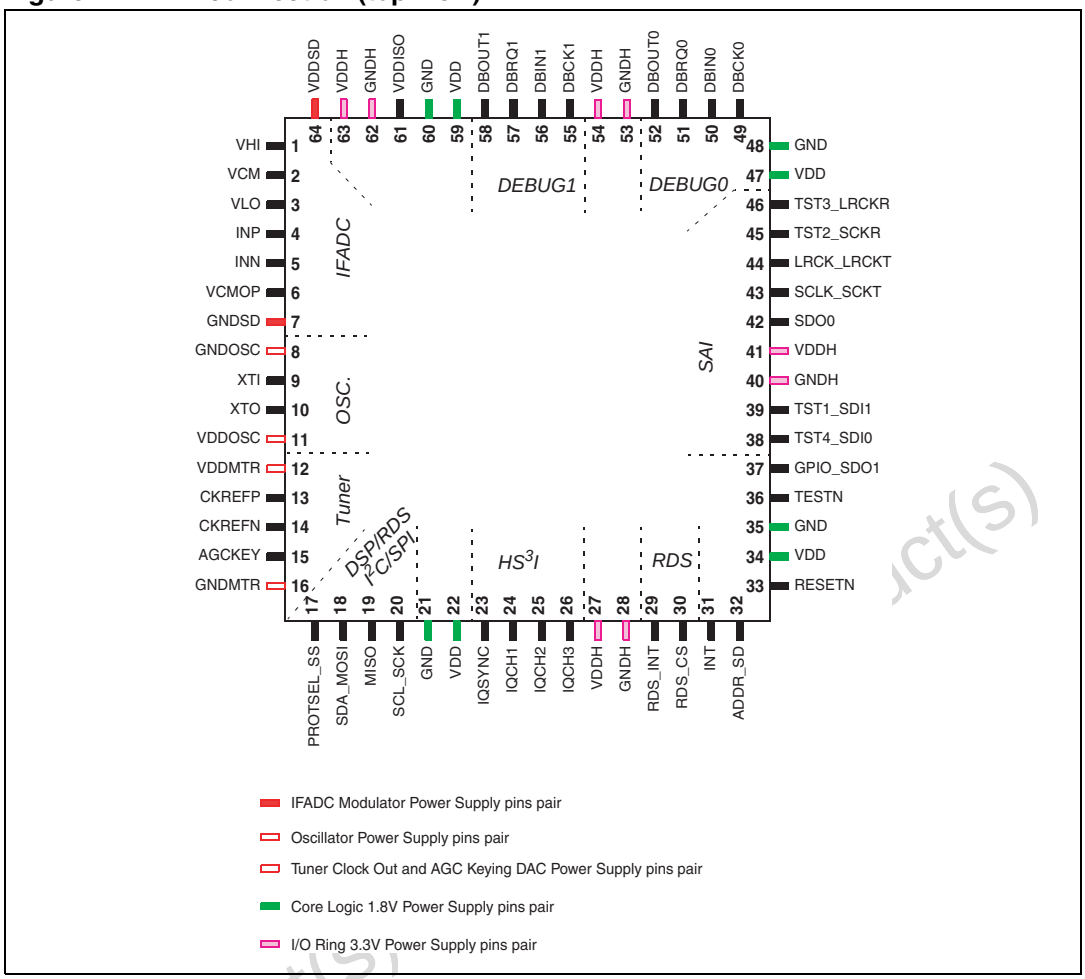


Table 5. Pin description

N°	Name	Type	Description	Notes	After Reset
1	VHI	A	Internally generated IFADC Opamps 2.65V (@V_{DD}=3.3V) reference voltage pin for external filtering	It needs external minimum 4.7µF ceramic capacitor	
2	VCM	A	Internally generated common mode 1.65V (@V_{DD}=3.3V) reference voltage pin for external filtering	It needs external minimum 10µF ceramic capacitor	
3	VLO	A	Internally generated IFADC opamps 0.65V (@V_{DD}=3.3V) reference voltage pin for external filtering	It needs external minimum 4.7µF ceramic capacitor	
4	INP	A	Positive IF signal input from tuner	2.0Vpp @VDD=3.3V	
5	INN	A	Negative IF signal input from tuner	2.0Vpp @VDD=3.3V	
6	VCMOP	-	Not connected.		

Table 5. Pin description (continued)

N°	Name	Type	Description	Notes	After Reset
7	GNDSD	G	IFADC modulator analogue ground	Clean ground, to be star connected to voltage regulator ground	
8	GNDOSC	G	Oscillator ground	Clean ground, to be star connected to voltage regulator ground	
9	XTI	I	High impedance oscillator input (quartz connection) or clock input when in Antenna Diversity slave mode	Maximum voltage swing is VDD=3.3V	
10	XTO	O	Low impedance oscillator output (quartz connection)		
11	VDDOSC	P	Oscillator power supply	3.3V	
12	VDDMTR	P	Tuner reference clock and AGC keying DAC power supply	1.8V	
13	CKREFP	B	Tuner reference clock positive output.	FM 100kHz AM_{EU} 18kHz With internal pull-up, on at reset [PP]	Output
14	CKREFN	B	Tuner reference clock negative output.	FM 100kHz AM_{EU} 18kHz With internal pull-up, on at reset [PP]	Output
15	AGCKEY	A	DAC output for Tuner AGC keying	1.5kohm ±30% output impedance. 1Vpp ±1% output dynamic range	
16	GNDMTR	G	Ground of the tuner reference clock buffer and the AGC keying DAC		
17	PROTSEL_SS	B	DSP0 GPIO for control serial interface (low: SPI or high: I^2C) selection at device Bootstrap. In SPI protocol mode, after boot procedure, SPI slave select, otherwise DSP0 GPIO0	DSP0 GPIO0 5V tolerant With internal pull-up, on at reset [PP]	Input
18	SDA_MOSI	B	Control serial interface and RDS IO: - SPI mode: slave data in or master data out for main SPI & RDS SPI data in - I^2C mode: data for main I^2C or RDS I^2C	5V tolerant With internal pull-up, on at reset [PP]	Input
19	MISO	B	SPI slave data out or master data in for main SPI and RDS SPI data out	DSP0 GPIO1 5V tolerant. With internal pull-up, on at reset [PP]	Input
20	SCL_SCK	B	Bit clock for Control Serial Interface and RDS	5V tolerant. With internal pull-up, on at reset [PP]	Input

Table 5. Pin description (continued)

N°	Name	Type	Description	Notes	After Reset
21	GND	G	Digital core power ground		
22	VDD	P	Digital core power supply	1.8V	
23	IQSYNC	B	High speed synchronous serial interface (HS^3I) clock if HS^3I master mode, else DSP1 GPIO or DSP1 debug port clock (DBOUT1)	DSP1 GPIO0 5V tolerant. With internal pull-up, on at reset	Input
24	IQCH1	B	High speed synchronous serial interface (HS^3I) channel 1 data if HS^3I master mode, else DSP1 GPIO or DSP1 debug port request (DBRQ1)	DSP1 GPIO1 5V tolerant. With internal pull-up, on at reset [PP]	Input
25	IQCH2	B	High speed synchronous serial interface (HS^3I) channel 2 data if HS^3I master mode, else DSP1 GPIO or DSP1 debug port data In (DBIN1)	DSP1 GPIO2 5V tolerant. With internal pull-down, on at reset [PP]	Input
26	IQCH3	B	High speed synchronous serial interface (HS^3I) channel 3 data if HS^3I master mode, else DSP1 GPIO or DSP1 debug port data out (DBCK1)	DSP1 GPIO3 5V tolerant With internal pull-down, on at reset [PP]	Input
27	VDDH	P	3.3V IO ring power supply (HS^3I, I^2C/SPI, RDS, INT)		
28	GNDH	G	3.3V IO ring power ground (HS^3I, I^2C/SPI, RDS, INT)		
29	RDS_INT	B	RDS interrupt to external main microprocessor in case of traffic information	DSP1 GPIO4. 5V tolerant, open drain With internal pull-up, on at reset [OD]	Input
30	RDS_CS	B	RDS chip select. When RESETN rising, If RDS_CS 0, the RDS's SPI is selected; else RDS's I^2C	DSP1 GPIO5. 5V tolerant. With internal pull-up, on at reset [PP]	Input
31	INT	I	DSP0 external interrupt	5V tolerant. With internal pull-up, on at reset	
32	ADDR_SD	B	IFS chip master (Low) or slave (High) mode selection, latched in upon RESETN release. It selects the LSB of the I^2C addresses. Station detector output	DSP0 GPIO2 5V tolerant With internal pull-down, on at reset [PP]	Input
33	RESETN	I	Chip hardware reset, active low	5V tolerant With internal pull-up	
34	VDD	P	Digital power supply	1.8V	
35	GND	G	Digital power ground		
36	TESTN	I	Test enable pin, active low	With internal pull-up	

Table 5. Pin description (continued)

N°	Name	Type	Description	Notes	After Reset
37	GPIO_SDO1	B	DSP0 GPIO for boot selection or audio SAI0 output.	5V tolerant. DSP0 GPIO3. With internal pull-up, on at reset [PP]	Input
38	TST4_SDI0	B	Audio SAI0 data input or test selection pin in test mode	5V tolerant. DSP0 GPIO5. With internal pull-up, on at reset [PP]	Input
39	TST1_SDI1	B	DSP0 GPIO for boot selection or audio SAI1 input. Test selection pin in test mode.	5V tolerant. DSP0 GPIO4. With internal pull-up, on at reset [PP]	Input
40	GNDH	G	3.3V IO ring power ground (audio SAI, ResetN, test pins)		
41	VDDH	P	3.3V IO ring power supply (audio SAI, ResetN, test pins)		
42	SDO0	B	Radio or audio SAI0 data output	5V tolerant. With internal pull up, @0V at reset [PP]	Output
43	SCLK_SCKT	B	SAI0 receive and transmit bit clock (master or slave with ASRC); SAI1 transmit bit clock	5V tolerant With internal pull up, on at reset [PP]	Input
44	LRCK_LRCKT	B	SAI0 receive and transmit left/right clock (master or slave with ASRC); SAI1 transmit left/right clock	5V tolerant With internal pull up, on at reset [PP]	Input
45	TST2_SCKR	B	SAI0 Transmit bit clock; SAI1 receive and transmit bit clock. Or test selection pin in test mode	5V tolerant. DSP0 GPIO6. With internal pull up, on at reset [PP]	Input
46	TST3_LRCKR	B	SAI0 Transmit LeftRight clock; SAI1 Receive and Transmit bit clock. Or Test selection pin in Test Mode	DSP0 GPIO7. 5V tolerant. With internal pull up, on at reset [PP]	Input
47	VDD	P	Digital core power supply	1.8V	
48	GND	G	Digital core power ground		
49	DBCK0	B	Debug port clock of DSP0 (DBCK0)	DSP0 GPIO. 9. 5V tolerant. With internal pull down, on at reset [PP]	Input
50	DBIN0	B	Debug port data input of DSP0 (DBIN0)	DSP0 GPIO. 11. 5V tolerant. With internal pull down, on at reset [PP]	Input
51	DBRQ0	B	Debug port request of DSP0 (DBRQ0)	DSP0 GPIO. 5V tolerant With internal pull up, on at reset [PP]	Input
52	DBOUT0	B	Debug port data output of DSP0 (DBOUT0)	DSP0 GPIO10. 5V tolerant. With internal pull up, on at reset [PP]	Input

Table 5. Pin description (continued)

N°	Name	Type	Description	Notes	After Reset
53	GNDH	G	3.3V IO ring power ground (debug interface, GPIO)		
54	VDDH	P	3.3V IO ring power supply (Debug interface, GPIO)		
55	DBCK1	B	DSP1 debug port clock (DBCK1) if HS^{3}I master mode, else high speed synchronous serial interface (HS^{3}I) channel3 data	DSP1 GPIO9. 5V tolerant. With internal pull down, on at reset [PP]	Input
56	DBIN1	B	DSP1 GPIO or DSP1 debug port data in (DBIN1) if HS^{3}I master mode, else high speed synchronous serial interface (HS^{3}I) channel2 data i	DSP1 GPIO11 5V tolerant With internal pull down, on at reset [PP]	Input
57	DBRQ1	B	DSP1 GPIO or DSP1 debug port request (DBRQ1) if HS^{3}I master mode, else high speed synchronous serial interface (HS^{3}I) channel1 data	5V tolerant. With internal pull up, on at reset [PP]	Input
58	DBOUT1	B	DSP1 GPIO or DSP1 debug port data out (DBOUT1) if HS^{3}I master mode, else high speed synchronous serial interface (HS^{3}I) clock	DSP1 GPIO10 5V tolerant With internal pull up, on at reset [PP]	Input
59	VDD	P	Digital core power supply	1.8V	
60	GND	G	Digital core power ground		
61	VDDISO	P	3.3V N-isolation biasing supply	Clean 3.3V supply to be star connected to voltage regulator	
62	GNDH	G	3.3V IO ring power ground (modulator digital section)		
63	VDDH	P	3.3V IO ring power supply (modulator digital section)		
64	VDDSD	P	3.3V IFADC modulator analogue power supply	Clean power supply, to be star connected to 3.3V voltage regulator	

I/O Type

P: Power supply from voltage regulator
G: Power ground from voltage regulator
A: Analogue I/O
I: Digital input
O: Digital output
B: Bidirectional I/O

I/O Definition and status

Z: high impedance (input)
O: logic low output
X: undefined output
1: logic high output
Output **PP**: Push pull / **OD**: Open drain

2.2 Electrical characteristics

Table 6. General interface electrical characteristics
(T_j =-40°C to 125°C; V_{DD}=1.8V, V_{DD3}= 3.3V)

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
I_{ilh}	Low level input current I/Os@V_{DD3} (absolute value)	V_i = 0V (1) (2) without pull-up-down device			1	µA
I_{ihh}	High level input current I/Os@V_{DD3} (absolute value)	V_i = V_{DD3} (1) (2) without pull-up-down device			1	µA
I_{il}	Low level input current I/Os@V_{DD} (absolute value)	V_i = 0V (1) (3) (4) without pull-up-down device			1	µA
I_{ih}	High level input current I/Os@V_{DD} (absolute value)	V_i = V_{DD} (1) (3) (4) without pull-up device			1	µA
I_{ipdh}	Pull-down current I/Os @ V_{DD3}	V_i = V_{DD3} (5) with pull-down device	35	60	85	µA
I_{opuh}	Pull-up current I/Os @ V_{DD3}	V_i = 0V (6) with pull-up device	-100	-70	-40	µA
I_{opul}	Pull-up current I/Os @ V_{DD}	V_i = 0V (3) with pull-up device	-40	-30	-20	µA
I_{aihop}	Analogue pin sunk / drawn current on pin1	V_i = V_{DD3}	0.95	1.25	1.55	mA
		V_i = 0V	-6.25	-5.0	-3.75	mA
I_{acm}	Analogue pin sunk / drawn current on pin 2	V_i = V_{DD3}	6.0	8.0	10.0	mA
		V_i = 0V	-10.0	-8.0	-6.0	mA
I_{ail}	Analogue pin sunk / drawn current on pin 3	V_i = V_{DD3}	3.75	5.0	6.25	mA
		V_i = 0V	-1.55	-1.25	-0.95	mA
I_{ain}	Analogue pin sunk / drawn current on pin 4 and pin 5	V_i = V_{DD3}	24	32	40	µA
		V_i = 0V	-40	-32	-24	µA
I_{aih6}	Analogue pin current on pin 6	V_o = 0V or V_{DD3}			5	µA
I_{aik}	Analogue pin sunk / drawn current on pin 15	V_i = V_{DD}	0.8	1.2	1.6	mA
		V_i = 0V (spec absolute value)			1	µA
I_{oz}	Tri-state output leakage	V_o = 0V or V_{DD3} without pull up / down device (1)			1	µA
I_{ozFT}	5V tolerant tri-state output leakage	V_o = 0V or V_{DD} (1)			1	µA
		V_o = 5V			80	µA
$I_{latchup}$	I/O latch up current	V < 0V, V > V_{DD}	200			mA
V_{esd}	Electrostatic protection	Leakage, 1µA	2000			V

1. The leakage currents are generally very small, <1nA. The value given here, 1mA, is the maximum that can occur after an electrostatic stress on the pin.
2. On pins: 17 to 20, 23 to 26, 29 to 33, 36 to 39, 42 to 46, 49 to 52, 55 to 58.
3. On pins: 13 and 14.
4. Same check on the analogue pin 15 (physically without pull-up-down)
5. On pins: 25, 26, 32, 49, 50, 55, 56
6. On pins: 17 to 20, 23 to 24, 29 to 31, 33, 36 to 39, 42 to 46, 51, 52, 57, 58

Table 7. Low voltage interface CMOS DC electrical characteristics
(T_j =-40°C to 125°C; V_{DD3}= 3.3V)

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
V_{il}	Low level input voltage	1.70V<=V_{DD}<=1.90V			0.2*V_{DD}	V
V_{ih}	High level input voltage	1.70V<=V_{DD}<=1.90V	0.8*V_{DD}			V
V_{ol}	Low level output voltage	I_{ol} = 4mA (1)			0.15	V
V_{oh}	High level output voltage	I_{ol} = -4mA (1)	V_{DD}-0,15			V

1. It is the source/sink current under worst case conditions and reflects the name of the I/O cell according to the drive capability.

Table 8. High voltage CMOS interface DC electrical characteristics
(T_j =-40°C to 125°C; V_{DD}=1.8V)

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
V_{il}	Low level input voltage	3.15V<=V_{DD3}<=3.45V			0.8	V
V_{ih}	High level input voltage	3.15V<=V_{DD3}<=3.45V	2.0			V
V_{ol}	Low level output voltage	I_{ol} = XmA (1) (2)			0.15	V
V_{oh}	High level output voltage	I_{ol} = -XmA (1) (2)	V_{DD3}-0.15			V

1. It is the source/sink current under worst case conditions & reflects the name of the I/O cell according to the drive capability
2. X=4mA for pins 17 to 20, 29, 30, 32, 37 to 39, 42 to 46; X=8mA for pins 23 to 26, 49 to 52, 55 to 58.

Table 9. Current consumption (T_j =-40°C to 125°C)

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
I_{DD}	Current through V_{DD} power supply	V_{DD}=1.8V,V_{DD3}=3.3V All digital blocks working		120	150	mA
I_{DDHdc}	Static current through V_{DDH} power supply	V_{DD}=1.8V,V_{DD3}=3.3V	10	13	16	mA
I_{DDHac}	Current through V_{DDH} power supply	V_{DD}=1.8V,V_{DD3}=3.3V I/Os working with 5pF load			50	mA
I_{SD}	Current through V_{SD} power supply	V_{DD}=1.8V,V_{DD3}=3.3V	25	35	45	mA
I_{OSCdc}	Current through V_{OSC} power supply	V_{DD}=1.8V,V_{DD3}=3.3V without quartz	5.5	8	10.5	mA
I_{OSCac}	Current through V_{OSC} power supply	V_{DD}=1.8V,V_{DD3}=3.3V with quartz	6.5	9	11.5	mA
I_{MTR}	Current through V_{MTR} power supply	V_{DD}=1.8V,V_{DD3}=3.3V	0.5	1.3	2.0	mA

Note: 74.1MHz internal DSP clock, at T_{amb} = 25°C. Current due to external loads not included.

Table 10. Oscillator characteristics
(T_j =-40°C to 125°C; V_{DD} =1.7V to 1.9V, V_{DD3} = 3.15V to 3.45V)

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
F_{OSCFM}	Oscillator frequency (XTI/XTO)			74.1		MHz

Note: The accuracy depends on the quartz frequency precision: high stability oscillator

Table 11. Crystal characteristics for 1 and 2 chip load

Parameter name	Parameter value	
	1 chip load	2 chips load
Temperature range	-55°C÷125°C	-55°C÷125°C
Adjustment tolerance (@ 25°C ± 3°C)	± 30 ppm	± 30 ppm
Frequency stability (-20°C÷+70°C)	± 50 ppm	± 50 ppm
Aging @ 25°C	5 ppm/year	5 ppm/year
Shunt (static) capacitance [Co]	<5pF	<5pF
Motional capacitance	1fF ± 30%	1fF ± 30%
Mode of oscillation	AT-3rd	AT-3rd
Resonance resistance	< 75 ohm	< 45 ohm
Capacitive load for oscillation frequency = 74.1MHz	10pF	12pF

Table 12. External clock signal on XTI (In case the device is driven by an external clock through the XTI pin, the characteristics reported in this table have to be met)

Parameter name	Parameter value			
	Min	Typ	Max	Unit
Clock frequency		74.10		MHz
Frequency stability (-20°C÷+70°C)	-50		50	ppm
Clock jitter			10	ps_{rms}
Start up time			5	ms
Clock level (sine wave) (1)	220		640	mV rms
Clock level (square wave) (1)	0.50		1.80	V p-p
Clock duty cycle (square wave)	45		55	%
Clock rise / fall time (square wave) (1)			500	ps

1. specified @ XTI pin of TDA7580

Table 13. DSP core (T_j =-40°C to 125°C)

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
F_{dspMax}	Maximum DSP clock frequency	V_{DD}=1.7V, V_{DD3}= 3.3V	81.5			MHz

Table 14. FM stereo decoder characteristics
(T_j =-40°C to 125°C; V_{DD} =1.7V to 1.9V, V_{DD3} = 3.15V to 3.45V; BW for measurements 20Hz to 15KHz)

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
a_ch	Channel separation	(Adjustble by SW from 0 to -45dB)	-45		0	dB
THD	Total harmonic distortion	1KHz; mono; Δf=75KHz;		0.02	0.04	%
(S+N)/N	Signal plus noise to noise ratio	1KHz; mono; Δf=40KHz;	78	80	82	dB

MCK = 18.525MHz, F_{sin}/F_{sout} = 0.820445366

Table 15. Sample rate converter
(T_j =-40°C to 125°C; V_{DD} =1.7V to 1.9V, V_{DD3} = 3.15V to 3.45V);
BW for measurements 20Hz to 20KHz

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
THD+N	Total harmonic distortion + noise	20Hz to 20kHz, full scale, 16 bit inp.		-95	-92	dB
		20Hz to 20kHz, full scale, 20 bit inp.		-98	-95	dB
		1 kHz full scale, 16 bit inp.		-98	-95	dB
		2 kHz full scale, 16 bit inp.		-98	-95	dB
		5 kHz full scale, 16 bit inp.		-98	-95	dB
		10 kHz full scale, 16 bit inp		-98	-95	dB
		15 kHz full scale, 16 bit inp		-98	-95	dB
		1 kHz full scale, 20 bit inp.		-119	-116	dB
		2 kHz full scale, 20 bit inp.		-116	-113	dB
		5 kHz full scale, 20 bit inp.		-112	-109	dB
		10 kHz full scale, 20 bit inp		-108	-105	dB
		15 kHz full scale, 20 bit inp		-105	-102	dB
DR	Dynamic Range	1 kHz -60 dB - 16 bit inp. A-weighted	97	100		dB
	fratio = 0.82	1 kHz -60 dB - 24 bit inp. A-weighted	141	145		dB
R_p	Pass band ripple	from 20Hz to 15kHz		0.4	0.5	dB
F_{ratio}	Sampling frequency in/out ratio	Fsout = 44.1 kHz	0.7		1.13	

Figure 3. Power on and boot sequence using I²C

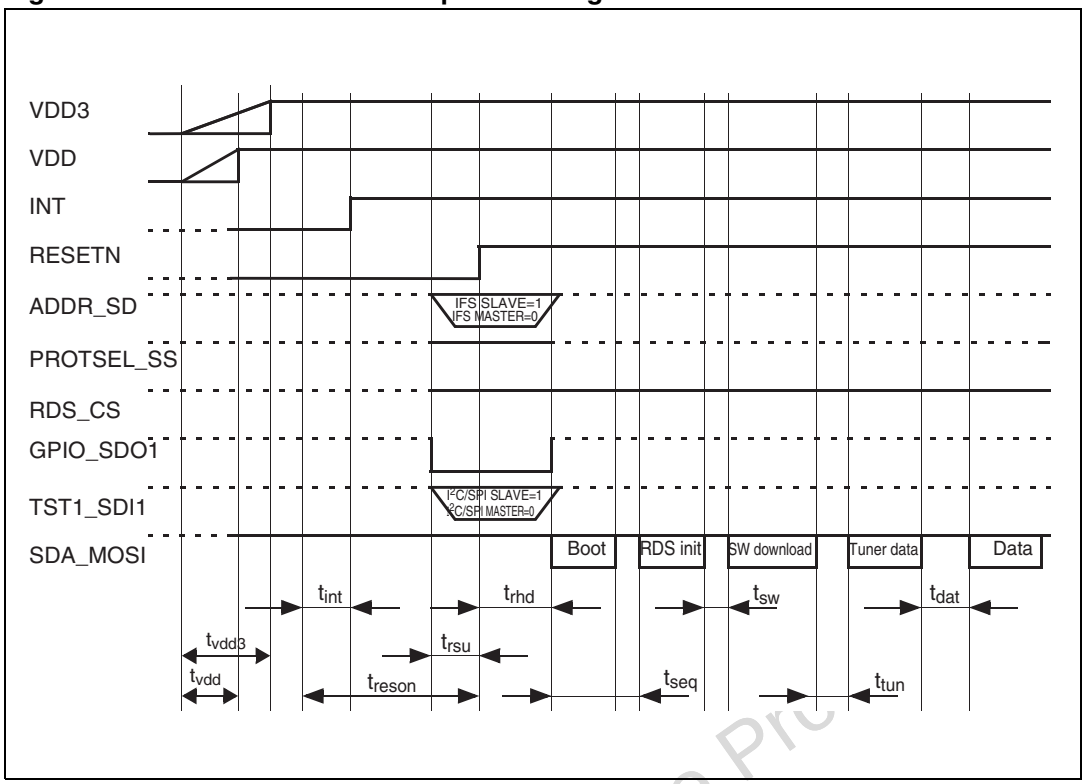


Figure 4. Power on and boot sequence using SPI

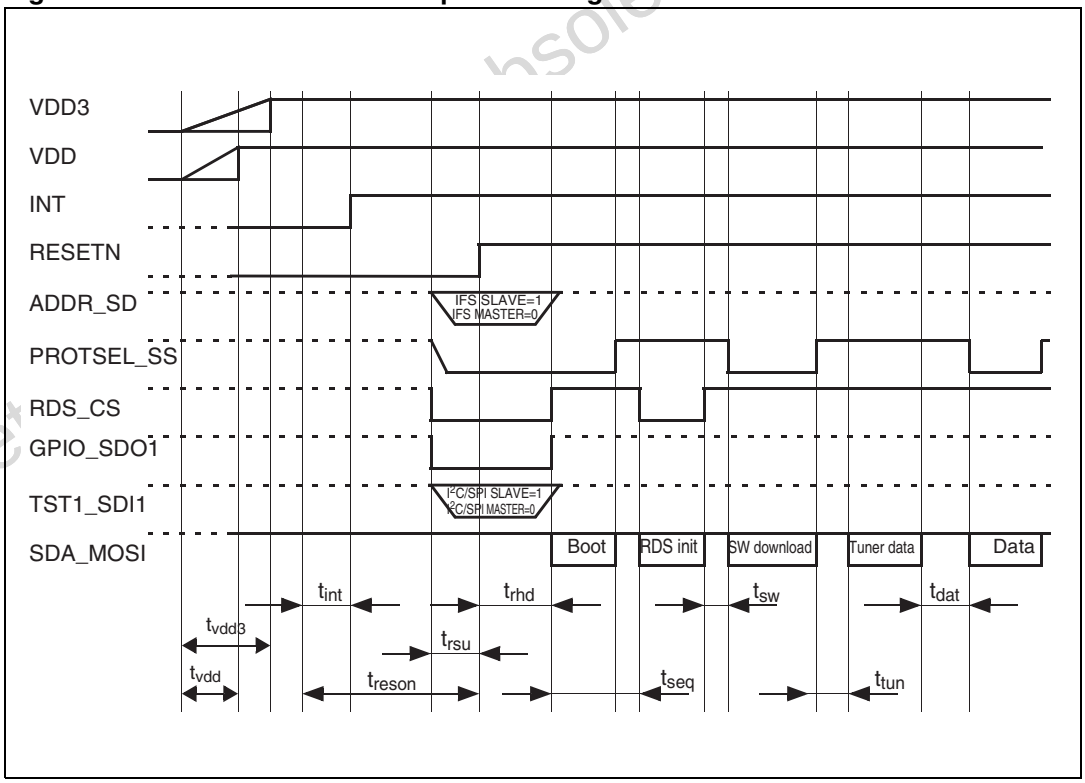


Table 16. SPI and I²C timing table
(T_j =-40°C to 125°C; V_{DD} =1.7V to 1.9V, V_{DD3} = 3.15V to 3.45V)

Timing	Description	Min	Typ	Max	Unit
t_{vdd3}	Rise time of 3.3V supply	1	13	25	ms
t_{vdd}	Rise time of 1.8V supply	1	6	10	ms
t_{int}	Maximux delay for INT signal	-	-	1	ms
t_{reson}	Minimum RESETN hold time at 0 after the start-up	40	-	-	ms
t_{rsu}	Minimum data set-up time	250			µs
t_{rhd}	Minimum data hold time	250			µs
t_{seq}	Minimum wait time including boot	4			ms
t_{sw}	Minimum wait time before downloading the program software	30			µs
t_{tun}	Minimum wait time before downloading the software to the FE	1			µs
t_{dat}	Minimum wait time before using interface protocols	1			µs

3 SAI Interface

Figure 5. SAI Timings

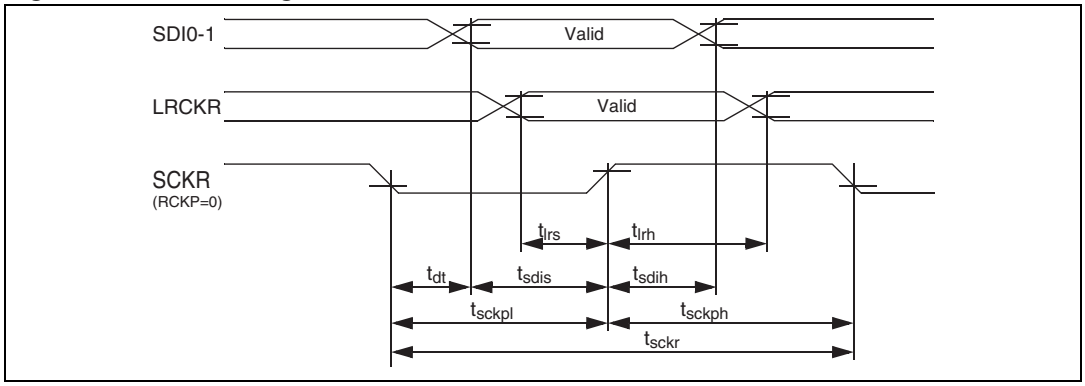


Table 17. SAI Timing table
(T_j =-40°C to 125°C; V_{DD} =1.7V to 1.9V, V_{DD3} = 3.15V to 3.45V) C_{load} The values on the table are consistent with a capacitance load on SAI lines of 160pF

Timing	Description	Min	Typ	Max	Unit
t_{sckr}	Clock Cycle	302		976	ns
t_{dt}	SCKR active edge to data out valid	48		65	ns
t_{lrs}	LRCK setup time	25			ns
t_{lrh}	LRCK hold time	25			ns
t_{sdis}	SDI setup time	65			ns
t_{sdih}	SDI hold time	65			ns
t_{sckph}	SCK high time	146			ns
t_{sckpl}	SCK low time	146			ns

Note: *T_{DSP} = DSP master clock cycle time = 1/F_{DSP}*

Figure 6. SAI protocol (when: RLRS=0; RREL=0; RCKP=1; RDIR=0)

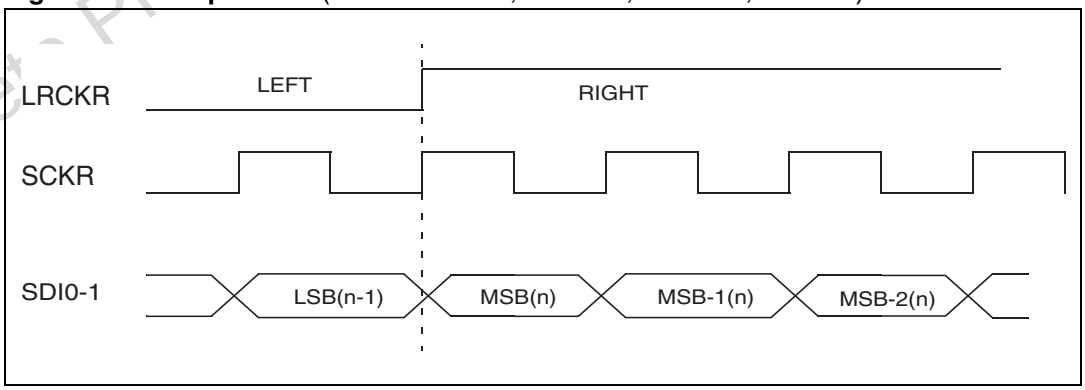


Figure 7. SAI protocol (when: RLRS=1; RREL=0; RCKP=1; RDIR=1)

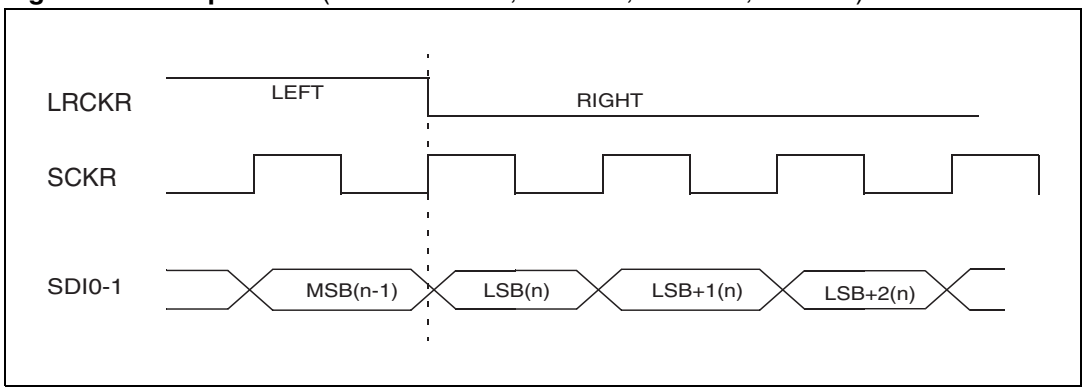


Figure 8. SAI protocol (when: RLRS=0; RREL=0; RCKP=0; RDIR=0)

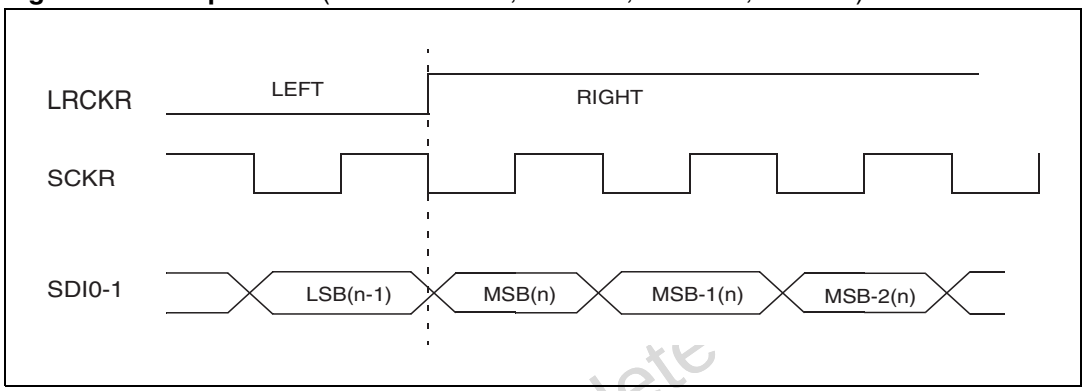
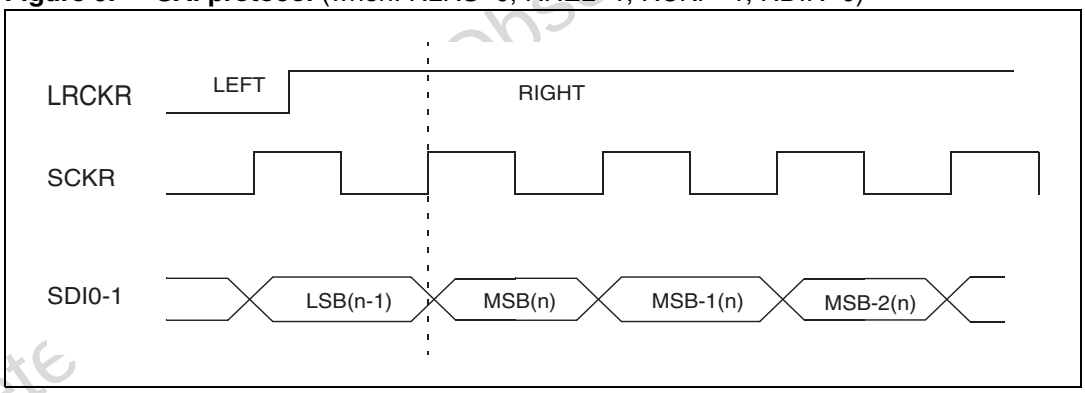


Figure 9. SAI protocol (when: RLRS=0; RREL=1; RCKP=1; RDIR=0)



4 RDS SPI interface

Figure 10. RDS SPI timings

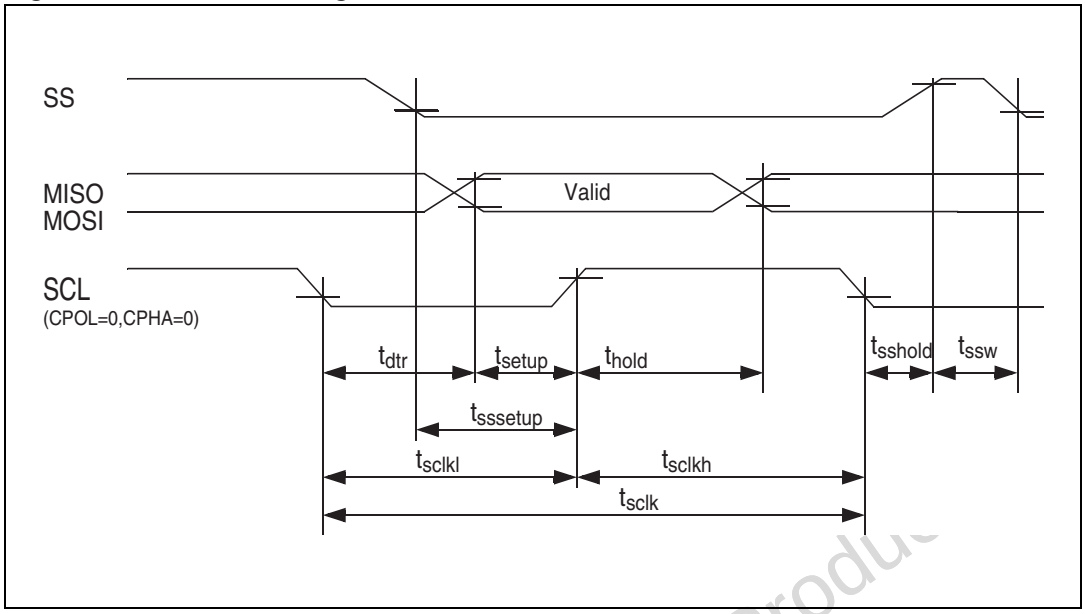
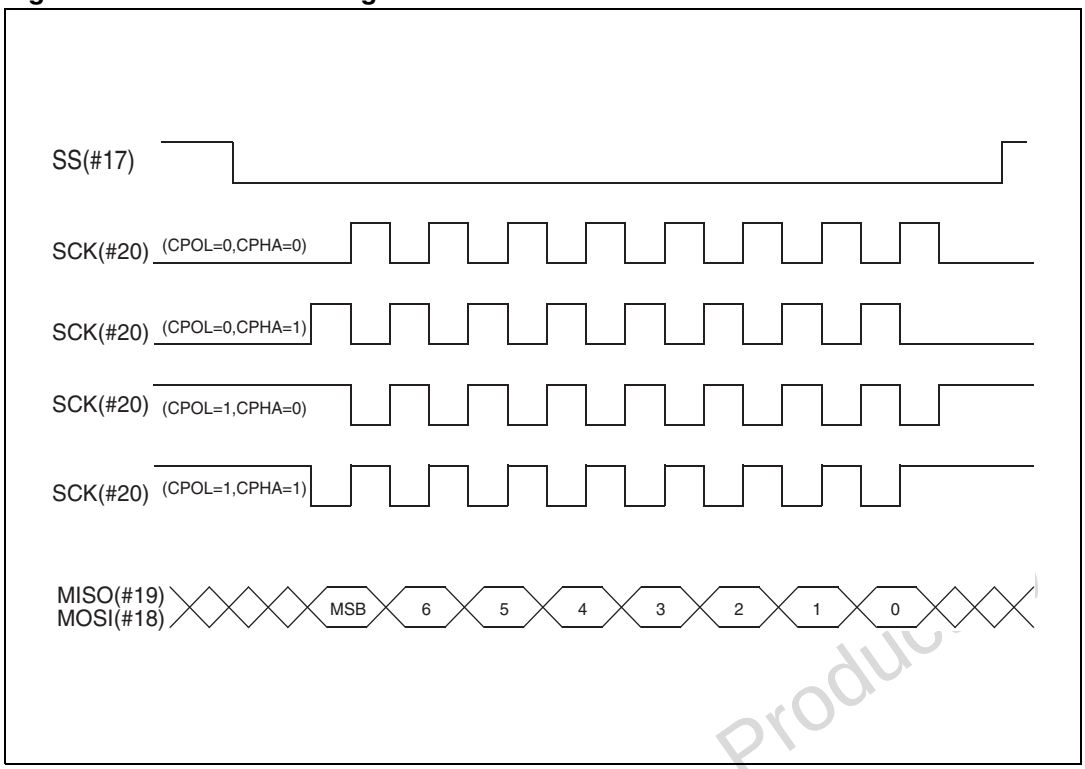


Table 18. RDS SPI timing table

(T_j =-40°C to 125°C; V_{DD} =1.7V to 1.9V, V_{DD3} = 3.15V to 3.45V) C_{load} The values on the table are consistent with a capacitance load on RDS SPI lines of 80pF

Symbol	Description	Min	Typ	Max	Unit
Slave configured					
t_{sclk}	Clock cycle	1240			ns
t_{dtr}	Sclk edge to MISO valid	239		365	ns
t_{setup}	MOSI setup time	255			ns
t_{hold}	MOSI hold time	365			ns
t_{sclkh}	SCK high time width	620			ns
t_{sclkl}	SCK low time width	620			ns
$t_{sssetup}$	SS setup time	620			ns
t_{sshold}	SS hold time	620			ns
t_{ssw}	SS pulse width	1240			ns

Figure 11. RDS SPI clocking scheme



5 BSPI interface

(T_j =-40°C to 125°C; V_{DD} =1.7V to 1.9V, V_{DD3} = 3.15V to 3.45V) C_{load}
The values on the table are consistent with a capacitance load on BSPI lines of 160pF)

Figure 12. BSPI timings

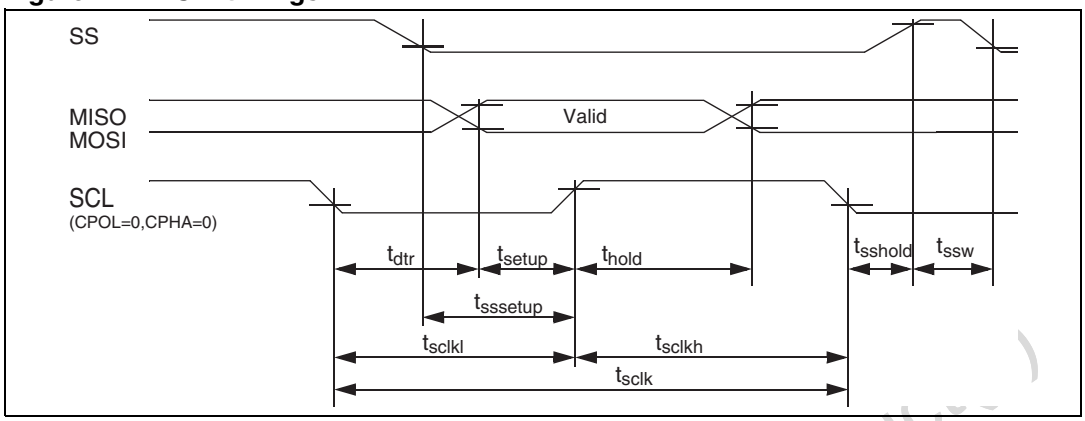
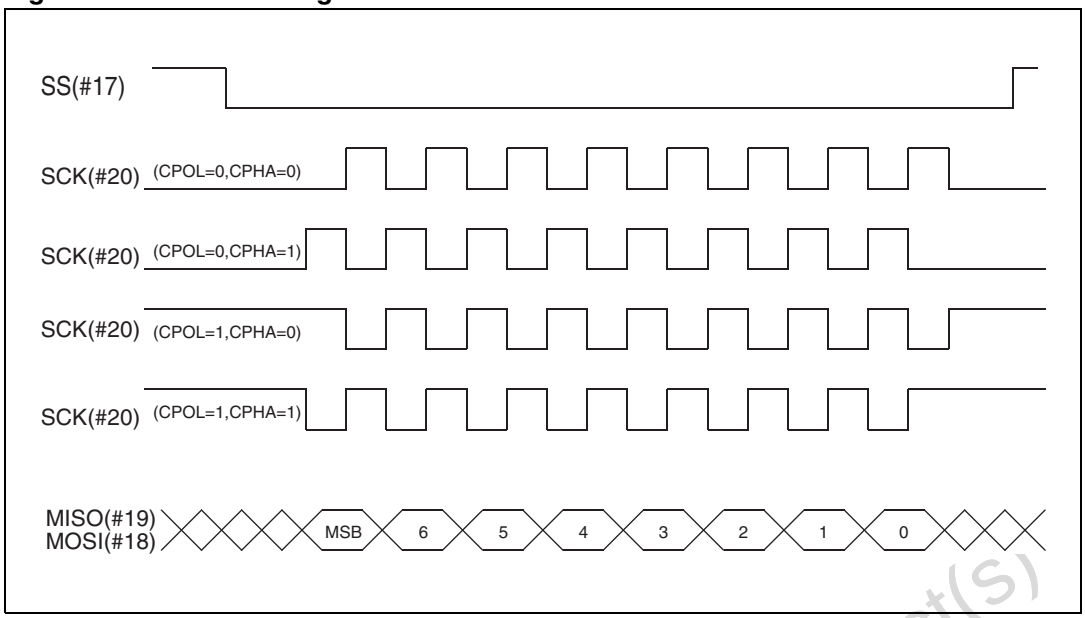


Table 19. BSPI timing table

Symbol	Description	Min	Typ	Max	Unit
Master configured					
t_{sclk}	Clock cycle	184			ns
t_{dtr}	Sclk edge to MOSI valid	61		92	ns
t_{setup}	MISO setup time	52			ns
t_{hold}	MISO hold time	52			ns
t_{sclkh}	SCK high time	92			ns
t_{sclkl}	SCK low time	92			ns
$t_{sssetup}$	SS setup time	92			ns
t_{sshold}	SS hold time	92			ns
t_{ssw}	SS pulse width	184			ns
Slave configured					
t_{sclk}	Clock cycle	238			ns
t_{dtr}	Sclk edge to MISO valid	88		119	ns
t_{setup}	MOSI setup time	65			ns
t_{hold}	MOSI hold time	65			ns
t_{sclkh}	SCK high time	119			ns
t_{sclkl}	SCK high low	119			ns
$t_{sssetup}$	SS setup time	119			ns
t_{sshold}	SS hold time	119			ns
t_{ssw}	SS pulse width	238			ns

Figure 13. BSPI clocking scheme



6 Inter processor transport interface for antenna diversity

(T_j =-40°C to 125°C; V_{DD} =1.7V to 1.9V, V_{DD3} = 3.15V to 3.45V) C_{load}. The values on the table are consistent with a capacitance load on HS^{3}I lines of 20pF

Figure 14. High speed synchronous serial interface - HS^{3}I

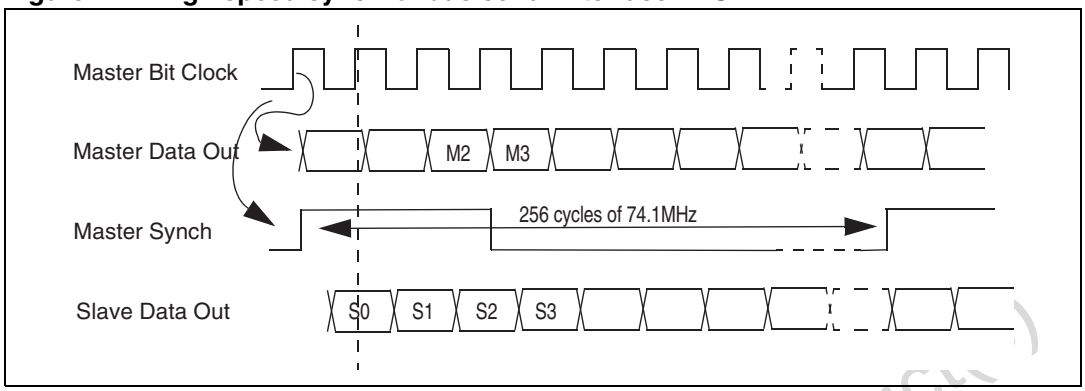


Figure 15. HS^{3}I clocking scheme

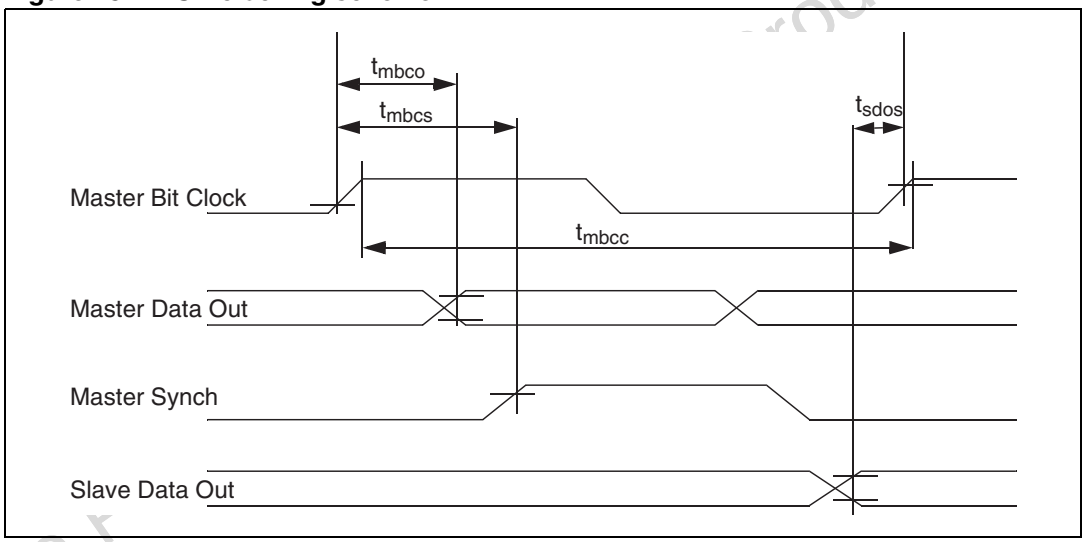


Table 20. HS^{3}I timing table

Timing	Description	Min	Typ	Max	Unit
t_{sclk}	MBC clock cycle	107.95		107.97	ns
t_{dtr}	MBC active edge to master data out valid	4			ns
t_{setup}	MBC active edge to master synch valid	4			ns
t_{hold}	Slave data out setup time	6			ns

Note: *T_{DSP} = DSP master clock cycle time = 1/F_{DSP}*

7 I²C timing

Figure 16. DSP and RDS I²C BUS timings

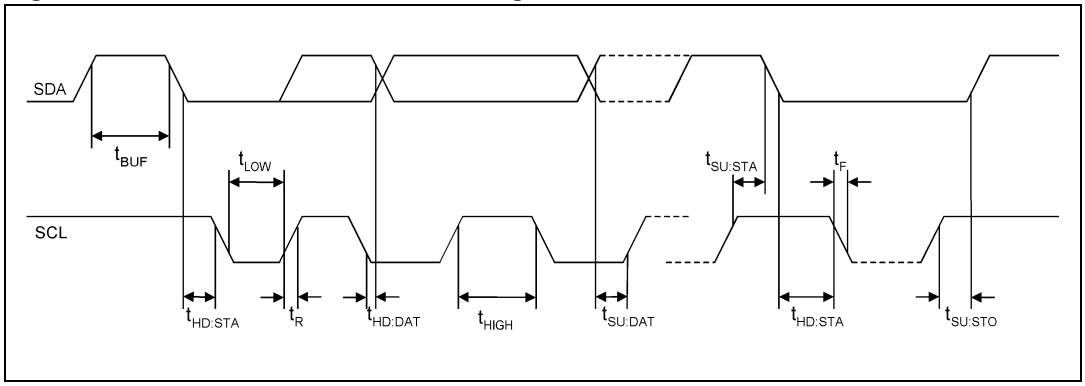


Table 21. I²C BUS timing table

(T_j =-40°C to 125°C; V_{DD} =1.7V to 1.9V, V_{DD3} = 3.15V to 3.45V)

Symbol	Parameter	Test condition	Standard mode I²C BUS		Fast mode I²C BUS		Unit
			Min.	Max.	Min.	Max.	
F_{SCL}	SCLI clock frequency		0	100	0	400	kHz
t_{BUF}	Bus free between a stop and start condition		4800	–	1300	–	ns
$t_{HD:STA}$	Hold time (repeated) START condition. After this period, the first clock pulse is generated		4800	–	600	–	ns
t_{LOW}	LOW period of the SCL clock		4800	–	1300	–	ns
t_{HIGH}	HIGH period of the SCL clock		4800	–	600	–	ns
$t_{SU:STA}$	Set-up time for a repeated start condition		4800	–	600	–	ns
$t_{HD:DAT}$	DATA hold time		0	-	0	900	ns
t_R	Rise time of both SDA and SCL signals	Cb in pF	–	300	12+0.1C_b	300	ns
t_F	Fall time of both SDA and SCL signals	Cb in pF	–	300	12+0.1C_b	300	ns
$t_{SU;STO}$	Set-up time for STOP condition		4800	–	600	–	ns
$t_{SU:DAT}$	Data set-up time		250	–	250	–	ns
C_b	Capacitive load for each bus line		10	400	10	400	pF

8 Functional description

The TDA7580 IC offers a solution for high performance FM/AM car radio receivers. The high processing power allows audio processing of both internal and external audio source.

The processing engine is based on a 24bit programmable DSP, with separate banks of program and data RAMs. A number of hardware modules (peripherals) help in the algorithm implementation of channel equalization and FM/AM baseband post processing.

The HW architecture allows to perform dual tuner diversity. In this case two TDA7580 are needed: one device must be configurated as master, generates the clock and controls the main data interfaces. The second device becomes the slave and converts the second IF path, as well as helps the first chip as co-processor.

8.1 24 bit DSP core

Some capabilities of the DSP are listed below:

- Single cycle multiply and accumulate with convergent rounding and condition code generation
- 24 x 24 to 56-bit MAC Unit
- Double precision multiply
- Scaling and saturation arithmetic
- 48-bit or 2 x 24-bit parallel moves
- 64 interrupt vector locations
- Fast or long interrupts possible
- Programmable interrupt priorities and masking
- Repeat instruction and zero overhead DO loops
- Hardware stack capable of nesting combinations of 7 DO loops or 15 interrupts / subroutines
- Bit manipulation instructions possible on all registers and memory locations, also jump on bit test
- 4 pin serial debug interface
- Debug access to all internal registers, buses and memory locations
- 5 word deep program address history FIFO
- Hardware and software breakpoints for both program and data memory accesses
- Debug single stepping, instruction injection and disassembly of program memory

8.2 DSP peripherals

- Clock generation unit (CGU)
- Stereo decoder (HWSTER)
- Serial audio interface (SAI)
- Tuner AGC keying DAC (KEYDAC)
- Programmable I/O interface (I^2C/BSPI)
- Asynchronous sample rate converter (ASRC)
- IF band pass sigma delta modulator (IFADC)
- Digital down converter (DDC)
- Discriminator (CORDIC)
- RDS
- Tuner diversity HS3I

The peripherals are mapped in the X memory space.

Most of them can be handled by interrupt, with software programmable priority.

Peripherals running at very high rate have direct access to X and Y data bus for very fast movement from or to the core, by mean of single cycle instruction.

8.3 Clock generation unit (CGU) and oscillator

This unit is responsible for supplying all necessary clocks and synchronization signals to the whole chip.

The control status register of this unit contains information about the current working mode (oscillator [master mode] or clock buffer [slave mode]), the tuner clock frequency setting, the general setup of the oscillator. This last function is performed inside the CGU, that establishes using a self trimming algorithm, which is the current values that can bias the oscillator: this feature lets the oscillator be independent from process parameters variation. The values of bias current are stored in the control status register of the CGU: 4 bits for the coarse current steps and 6 bits for the fine current steps.

In slave mode the oscillator behaves as a buffer: the chip can be then driven using an external clock. The clock divider, placed in this unit, generates the tuner the reference clock and can be programmed for frequencies down to 9KHz with selectable duty cycle and from 4.4Hz to 9KHz with duty cycle 50%.

An external clock can drive the XTI pin (please see *Table 12* for reference).

8.4 Stereo decoder (HWSTER)

The fully digital hardware stereo decoder does all the signal processing necessary to demodulate an FM MPX signal which is prepared by the channel equalization algorithm in the digital IF sampling device, providing pilot tone dependent mono/stereo switching, as well as stereo-blend and highcut functionality.

Selectable de-emphasis time constant allow the use of this module for different FM radio receiver standards.

There are built in filters for field strength processing. In order to obtain the maximum flexibility the field strength processing and noise cancellation, however, are implemented as software inside the programming DSP, which has to provide control signals for the stages softmute, stereoblend, and highcut.

8.5 Serial audio interface (SAI)

The two SAI modules have been embedded in such a way great flexibility is available in their use.

The two modules are fully separate and they each have a receive and a transmit channel, as well as they can be selected as either master or slave.

The bit clocks and left & right clocks are routed through the pins, so the audio interface can be chosen to be adapted to a large variety of application.

One SAI transmit channel can have the asynchronous sample rate converter in front, thus separate different audio rate domains.

Additional feature are:

- support of 16/24/32 bit word length
- programmable left/right clock polarity
- programmable rising/falling edge of the bit clock for data valid
- programmable data shift direction, MSB or LSB received / transmitted first

8.6 I^2C interfaces

The inter integrated circuit bus is a single bidirectional two wire bus used for efficient inter IC control. All I^2C bus compatible devices incorporate an on-chip interface which allows them communicate directly with each other via the I^2C bus.

Every component hooked up to the I^2C bus has its own unique address whether it is a CPU, memory or some other complex function chip. Each of these chips can act as a receiver and /or transmitter on its functionality.

Two pins are used to interface both I^2C of the DSP and RDS, which have different internal I^2C address, thus reducing the on board pin interconnections.

8.7 Serial peripheral interfaces

The DSP and RDS can have this serial interface, alternative to the I^2C one. DSP and RDS SPI modules have separate pin for chip select.

The DSP SPI has a ten 24 bit words deep FIFO for both receive and transmit sections, which reduces DSP processing overhead even at high data rate.

The serial interface is needed to exchange commands and data over the LAN. During an SPI transfer, data is transmitted and received simultaneously. A serial clock line synchronizes shifting and sampling of the information on the two serial data lines. A slave select line allows individual selection of a slave SPI device.

When an SPI transfer occurs an 8-bit word is shifted out one data pin while another 8-bit character is simultaneously shifted in a second data pin. The central element in the SPI

system is the shift register and the read data buffer. The system is single buffered in the transfer direction and double buffered in the receive direction.

8.8 High speed serial synchronous interface (HS^{3}I)

The high speed serial synchronous interface is a module to send and receive data at high rate (up to 9.25Mbit/s per channel) in order to exchange data between 2 separate TDA7580 chip.

The exchanged data are related to signals that are used to increase reception quality in car radio systems, which make use of antenna diversity based upon two separate antenna and tuner sections.

The channel synchronization clock has a programmable duty cycle, so to reduce in band harmonics noise.

8.9 Tuner AGC keying DAC (KEYDAC)

This DAC provides the front-end tuner with an analogue signal to be used to control the automatic gain controlled stage, thus giving all time the best voltage dynamic range at the IFADC input.

8.10 Asynchronous sample rate converter (ASRC)

This hardware module provides a very flexible way to adapt the internal audio rate, to the one of an external source. It does not require further work off the DSP.

There is no need to explicitly configure the input and the output sample rates, as the ASRC solves this problem with an automatic digital ratio locked loop.

Main features are:

- Automatic tracking of sample frequency
- Fully digital ratio locked loop
- Sampling clock jitter rejection
- Up conversion up to 1:2 Ratio
- Linear phase

8.11 IF band pass $\Sigma\,\Delta$ analogue to digital converter (IFADC)

The IFADC is a band pass Sigma Delta A to D converter with sampling rate of 37.05MHz (nominal) and notch frequency of 10.7MHz. The structure is a second order switched capacitor multi bit modulator with self calibration algorithm to adjust the notch frequency.

The differential ended input allows 4.0Vpp voltage dynamic range, and reduces the inferred noise back to the previous stage (tuner), and in turn gives high rejection to common mode noises.

The high linearity (very high IMD) is needed to fulfill good response of the channel equalization algorithm.

Low thermal and 1/f noise assures high dynamic range.

8.12 Digital down converter (DDC)

The DDC module allows to evaluate the in-phase and quadrature components of the incoming digital IF signal.

The I and Q computation is performed by the DDC block, which at the same time shifts down to 0-IF frequency the incoming digital signal.

After the down conversion the rate is still very high (at the 37.05MHz rate); a SincK filter samples data down by a factor of 32, decreasing it to 1.1578MHz. An additional decimation is performed by the subsequent FIR filters, thus lowering the data rate at the final 289.45kHz, being the MPX data rate.

8.13 RDS

The RDS block is an hardware cell able to process RDS/RBDS signal, intended for recovering the inaudible RDS/RBDS information which are transmitted by most of FM radio broadcasting stations.

It comprises of the following:

- Demodulation of the european radio data system (RDS)
- Demodulation of the US radio broadcast data system (RDBS)
- Automatic group and block synchronisation with flywheel mechanism
- Error detection and correction
- RAM buffer with a storage capacity of 24 RDS blocks and related status information
- I^2C and SPI interface, with pins shared with the DSP I^2C/SPI

After filtering the oversampled MPX signal, the RDS/RDBS demodulator extracts the RDS data clock, RDS data signal and the quality information.

The following RDS/RBDS decoder synchronizes the bitwise RDS stream to a group and block wise information. This processing also includes error detection and error correction algorithms.

In addition, an automatic flywheel control avoids exhausting the data exchange between RDS/RDBS processor and the host.

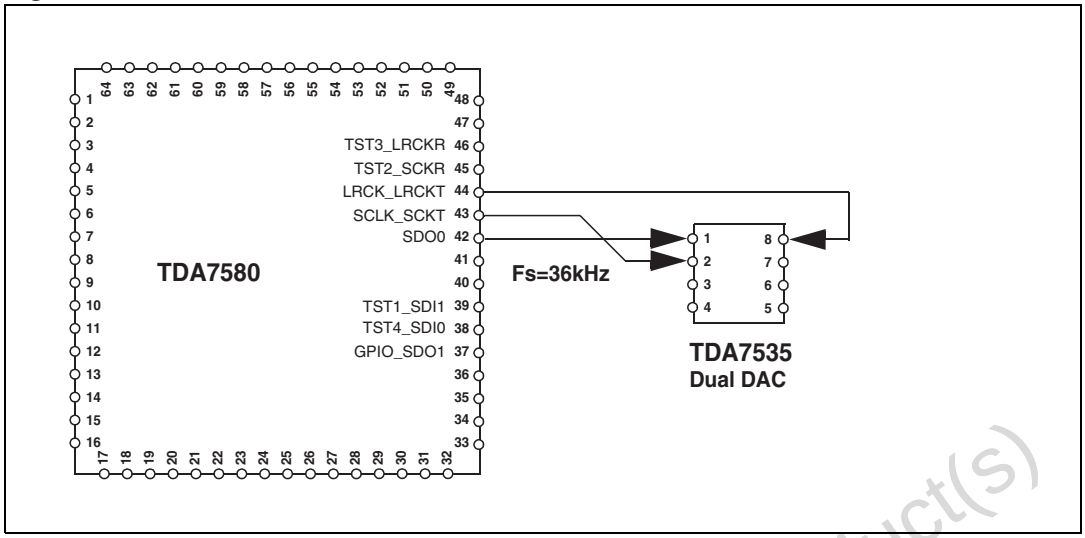
8.14 AM/FM Detector (CORDIC)

The AM/FM detector is a fully programmable peripheral used to detect the phase, amplitude and frequency information of an input complex signal (in-phase and quadrature signals). It can be used to demodulate PM, AM and FM modulated signals. The detection is performed using a high accuracy CORDIC algorithm, working essentially as a cartesian to polar transformer.

Four CORDICs are available to allow concurrent software calls.

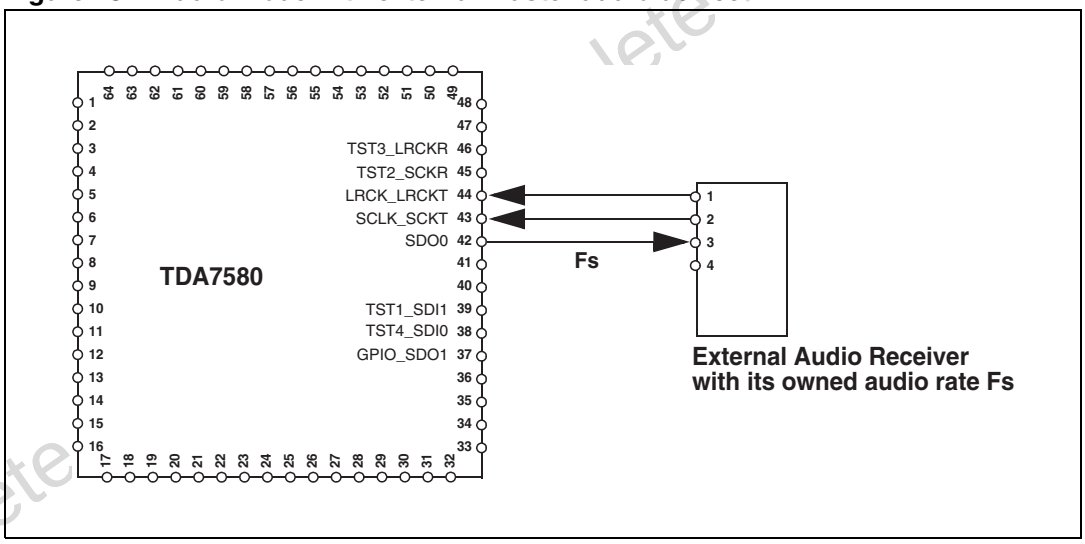
9 Application diagrams

Figure 17. Radio mode with external slave audio DAC



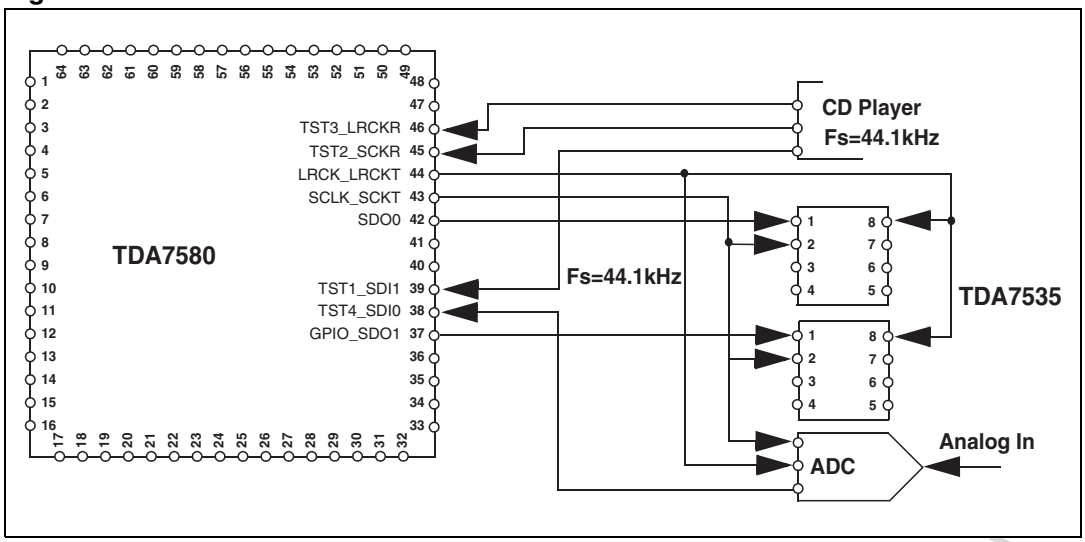
In this mode an external slave stereo DAC, like the ST TDA7535, can be easily connected and the TDA7580 outputs the audio from radio station at 36kHz rate.

Figure 18. Radio mode with external master audio device



An external digital audio device is connected externally as a digital audio master, and the internal TDA7580 sample rate converter is responsible for the conversion from internal 36kHz to the external audio rate.

Figure 19. Audio mode with external slave audio device



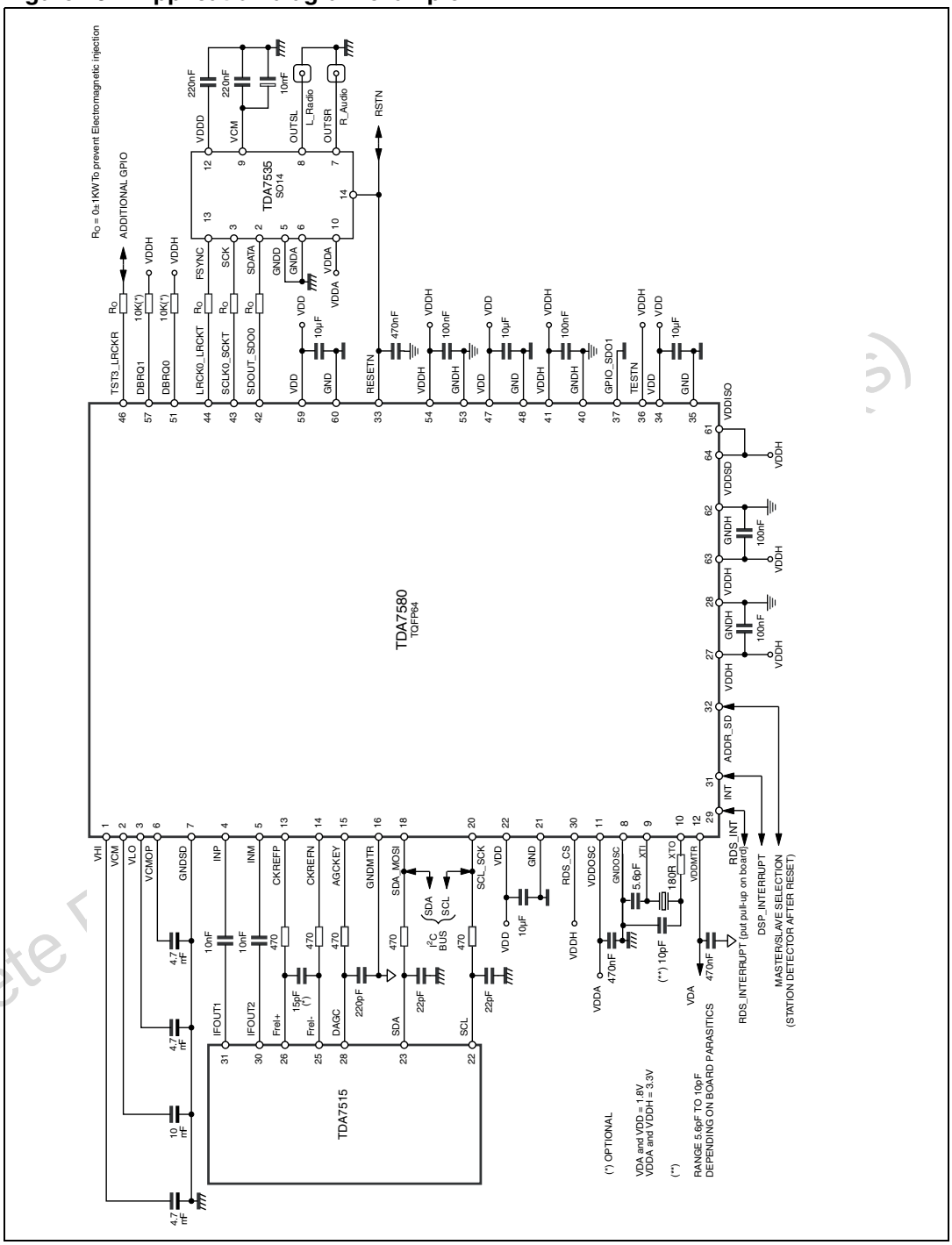
The 2 stereo channel serial audio interface of the TDA7580 chip allows a very flexible application in which external audio source/sinks can be connected.

The example shows an external CD player digital output giving the main Fs audio rate of the whole system. This rate is also the one of the external DACs and an ADC, being configured as slave.

9.1 Electrical application scheme

The following application diagram is only an example. For real application setup, it is necessary to refer to the application notes.

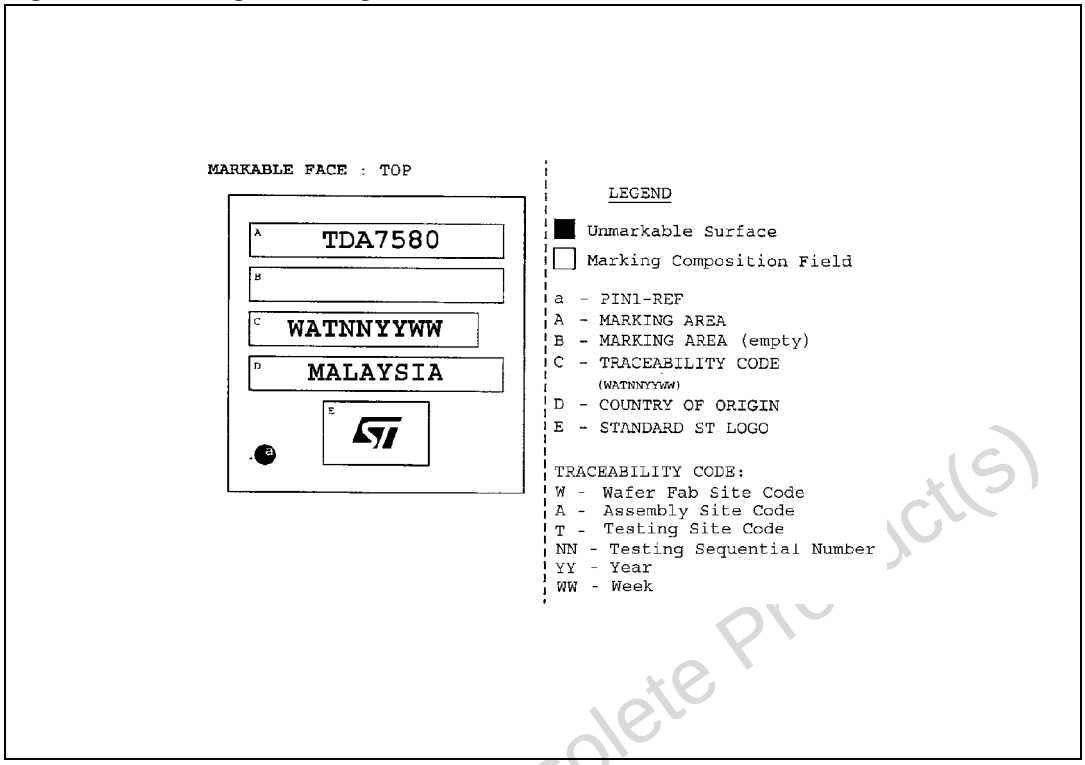
Figure 20. Application diagram example



Note: VCMOP capacitor (4.7uF) is only needed for CA silicon. This is needed to be consistent with "pin description " in Table 6

10 Package marking

Figure 21. Package marking



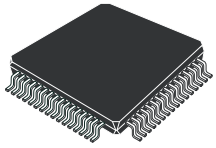
11 Package information

In order to meet environmental requirements, ST offers these devices in ECOPACK® packages. These packages have a lead-free second level interconnect. The category of second level interconnect is marked on the package and on the inner box label, in compliance with JEDEC standard JESD97. The maximum ratings related to soldering conditions are also marked on the inner box label.
ECOPACK is an ST trademark. ECOPACK specifications are available at: www.st.com.

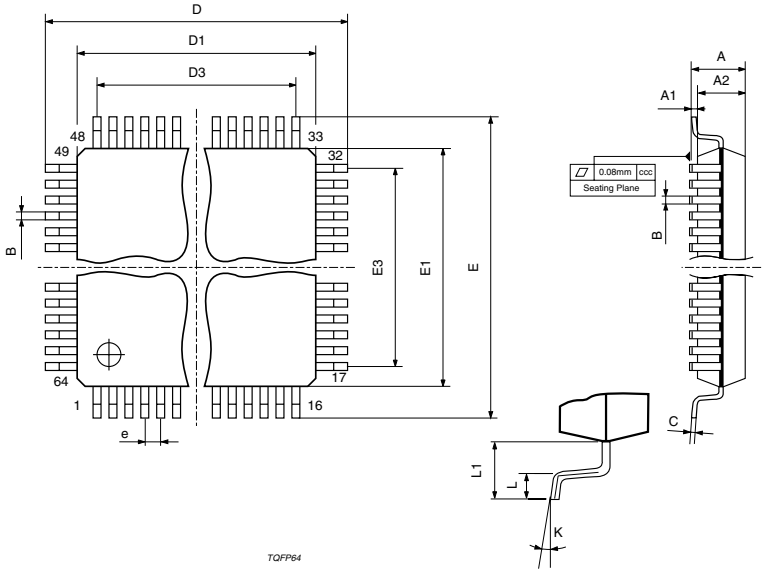
Figure 22. Mechanical, data and package dimensions

DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A			1.60			0.063
A1	0.05		0.15	0.002		0.006
A2	1.35	1.40	1.45	0.053	0.055	0.057
B	0.17	0.22	0.27	0.0066	0.0086	0.0106
C	0.09		0.20	0.0035		0.0079
D	11.80	12.00	12.20	0.464	0.472	0.480
D1	9.80	10.00	10.20	0.386	0.394	0.401
D3		7.50			0.295	
e		0.50			0.0197	
E	11.80	12.00	12.20	0.464	0.472	0.480
E1	9.80	10.00	10.20	0.386	0.394	0.401
E3		7.50			0.295	
L	0.45	0.60	0.75	0.0177	0.0236	0.0295
L1		1.00			0.0393	
K	0° (min.), 3.5° (min.), 7° (max.)					
ccc			0.080			0.0031

OUTLINE AND MECHANICAL DATA



LQFP64 (10 x 10 x 1.4mm)



12 Revision history

Table 22. Document revision history

Date	Revision	Changes
24-Jan-06	1	Initial release.
01-Jun-04	2	Changed the style look following the “Corporate technical publications design guide. Changed the maturity from product preview to final.
01-Dec-04	3	Included legend for I/O definition. Included separated specification for the 2 SPI (BSPI and RDS-SPI). Upgraded all tables with temperature range and electrical / timing parameters. Changed description of PIN 6 in PIN description table. Added new sub section titled AM/FM Detector (CORDIC).
01-Jan-06	4	Updated all tables.
09-Mar-07	5	Package changed, layout and text modifications

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