TH71111

868/915MHz Receiver
FSK/FM/ASK Receiver

Features

- ❑ Single superhet architecture for low external component count
- ❑ FSK for digital data and FM reception for analog signal transmission
- ❑ FSK/FM demodulation with phase-coincidence demodulator
- ❑ Low current consumption in active mode and very low standby current
- ❑ Switchable LNA gain for improved dynamic range
- ❑ RSSI allows signal strength indication and ASK detection
- ❑ Surface mount package LQFP32

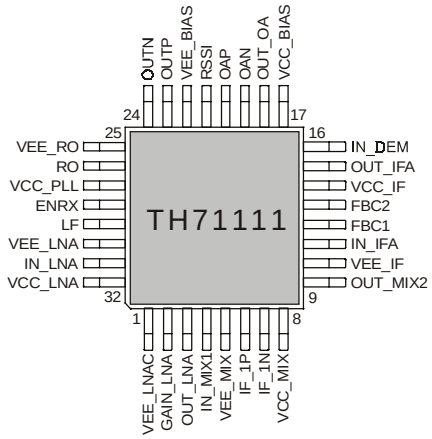
Ordering Information

Part No.	***Temperature Code***	***Package Code***
TH71111	E (-40 °C to 85 °C)	NE (LQFP32)

Application Examples

- ❑ General digital and analog 868 MHz or 915 MHz ISM band usage
- ❑ Low-power telemetry
- ❑ Alarm and security systems
- ❑ Remote Keyless Entry (RKE)
- ❑ Tire Pressure Monitoring System (TPMS)
- ❑ Garage door openers
- ❑ Home automation
- ❑ Pagers

Pin Description



General Description

The TH71111 FSK/FM/ASK single-conversion superheterodyne receiver IC is designed for applications in the European 868 MHz industrial-scientific-medical (ISM) band, according to the EN 300 220 telecommunications standard. It can also be used for any other system with carrier frequencies ranging from 800 MHz to 930 MHz (e.g. for applications in the US 915 MHz ISM band).

Document Content

1 Theory of Operation

1.1 General

With the TH71111 receiver chip, various circuit configurations can be arranged in order to meet a number of different customer requirements. For FSK/FM reception the IF tank used in the phase coincidence demodulator can be constituted either by a ceramic resonator or an LC tank (optionally with a varactor diode to create an AFC circuit). In ASK configuration, the RSSI signal is feed to an ASK detector, which is constituted by the operational amplifier.

Demodulation	Type of receiver
FSK / FM	narrow-band RX with ceramic demodulation tank
FSK / FM	wide-band RX with LC demodulation tank
ASK	RX with RSSI-based demodulation

A double-conversion variant, called TH71112, is also available. This receiver IC allows a higher degree of image rejection, achieved in conjunction with an RF front-end filter. Both RXICs have the same die. At the TH71112, the second mixer (MIX2) is used to down-convert the first IF (IF1) to the second IF (IF2). At the TH71111, MIX2 operates as an amplifier.

Efficient RF front-end filtering is realized by using a SAW, ceramic or helix filter in front of the LNA and by adding an LC filter at the LNA output.

The TH71111 receiver IC consists of the following building blocks:

- PLL synthesizer (PLL SYNTH) for generation of the local oscillator signal LO
- Parts of the PLL SYNTH are the high-frequency VCO1, the feedback divider DIV_32, a phase-frequency detector (PFD) with charge pump (CP) and a crystal-based reference oscillator (RO)
- Low-noise amplifier (LNA) for high-sensitivity RF signal reception
- First mixer (MIX1) for down-conversion of the RF signal to the IF
- IF pre amplifier which is a mixer cell (MIX2) that operates as an amplifier
- IF amplifier (IFA) to amplify and limit the IF signal and for RSSI generation
- Phase coincidence demodulator (DEMOD) with third mixer (MIX3) to demodulate the IF signal
- Operational amplifier (OA) for data slicing, filtering and ASK detection
- Bias circuitry for bandgap biasing and circuit shutdown

1.2 Technical Data Overview

- ❑ Input frequency range: 800 MHz to 930 MHz
- ❑ Power supply range: 2.3 V to 5.5 V @ ASK
- ❑ Temperature range: -40 °C to +85 °C
- ❑ Standby current: 50 nA
- ❑ Operating current: 7.5 mA at low gain mode
  9.2 mA at high gain mode
- ❑ Sensitivity: -112 dBm [1] with 40 kHz IF filter BW
- ❑ Sensitivity: -105 dBm [2] with 150 kHz IF filter BW
- ❑ Range of IF: 400 kHz to 22 MHz
- ❑ Maximum data rate: 80 kbit/s NRZ
- ❑ Maximum input level: -10 dBm at ASK
  0 dBm at FSK
- ❑ Image rejection: > 55 dB (e.g. with SAW front-end filter and at 10.7 MHz IF)
- ❑ Spurious emission: < -70 dBm
- ❑ Input frequency acceptance: ±50 kHz (with AFC option)
- ❑ RSSI range: 70 dB
- ❑ Frequency deviation range: ±4 kHz to ±120 kHz
- ❑ Maximum analog modulation frequency: 15 kHz

1) at ± 8 kHz FSK deviation, BER = $3 \cdot 10^{-3}$ and phase-coincidence demodulation
2) at ± 50 kHz FSK deviation, BER = $3 \cdot 10^{-3}$ and phase-coincidence demodulation

1.3 Block Diagram

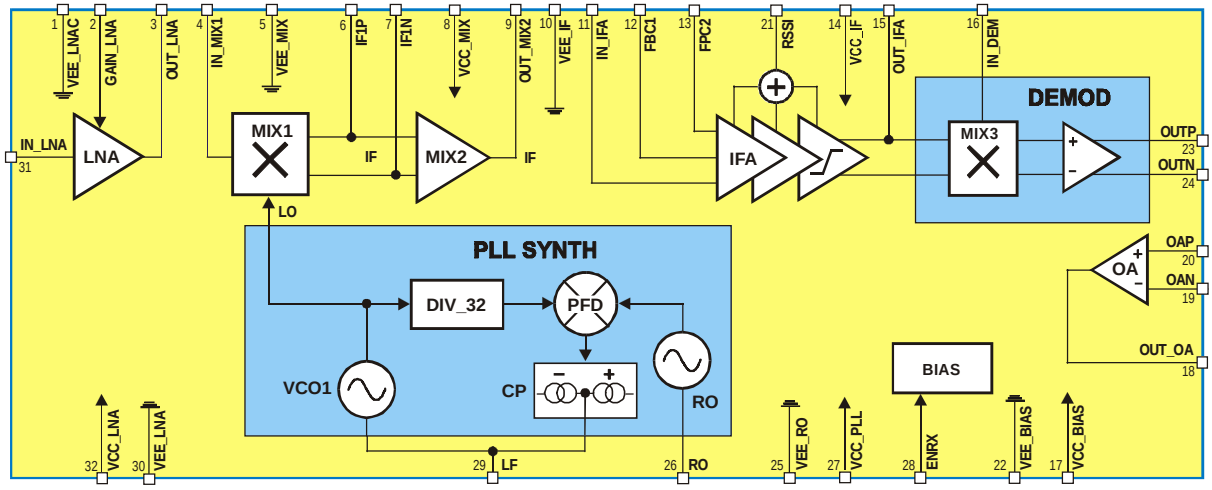


Fig. 1: TH71111 block diagram

1.4 Mode Configurations

ENRX	Mode	Description
0	RX standby	RX disabled
1	RX active	RX enable

Note: ENRX are pulled down internally

1.5 LNA GAIN Control

V_{GAIN_LNA}	Mode	Description
< 0.8 V	HIGH GAIN	LNA set to high gain
> 1.4 V	LOW GAIN	LNA set to low gain

Note: hysteresis between gain modes to ensure stability

1.6 Frequency Planning

Frequency planning is straightforward for single-conversion applications because there is only one IF that might be chosen, and then the only possible choice is low-side or high-side injection of the LO signal (which is now the one and only LO signal in the receiver).

The receiver's single-conversion architecture requires careful frequency planning. Besides the desired RF input signal, there are a number of spurious signals that may cause an undesired response at the output. Among them is the image of the RF signal that must be suppressed by the RF front-end filter.

By using the internal PLL synthesizer of the TH71111 with the fixed feedback divider ratio of N = 32 (DIV_32), two types of down-conversion are possible: low-side injection of LO and high-side injection of LO. The following table summarizes some equations that are useful to calculate the crystal reference frequency (REF), the IF and the LO frequency respectively, for a given RF.

Injection type	low	high
REF	(RF – IF)/32	(RF + IF)/32
LO	32 • REF	32 • REF
IF	RF – LO	LO – RF
RF image	RF – 2IF	RF + 2IF

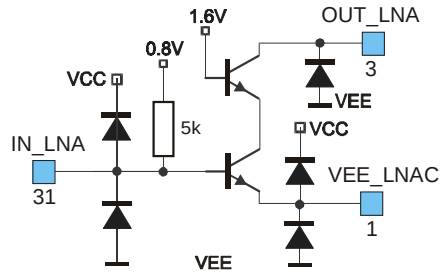
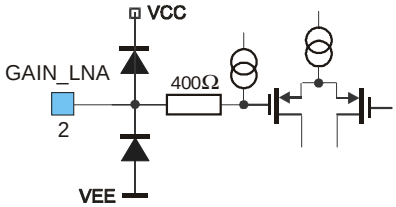
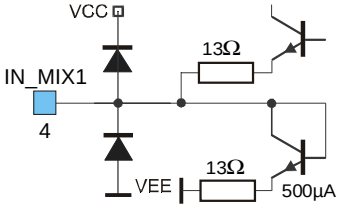
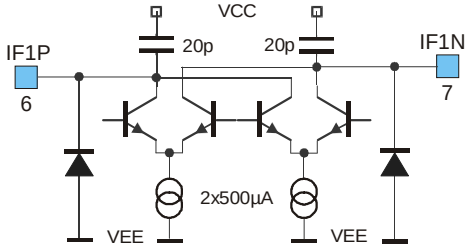
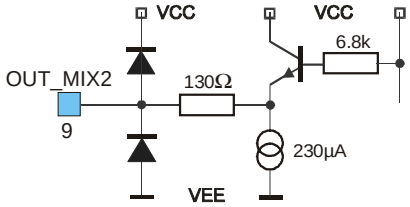
1.6.1 Selected Frequency Plans

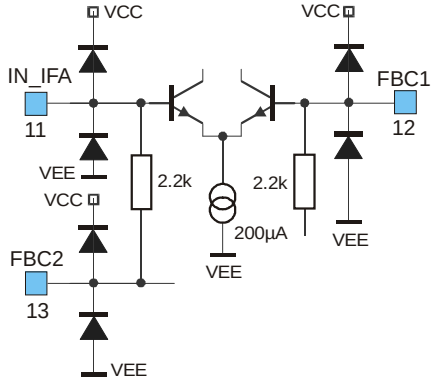
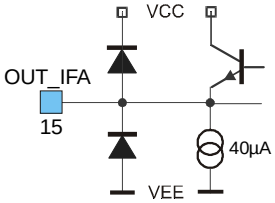
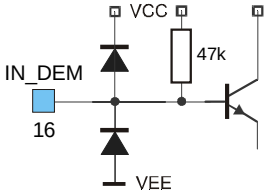
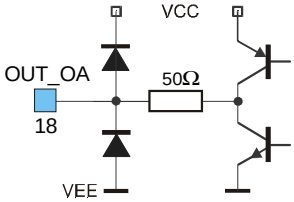
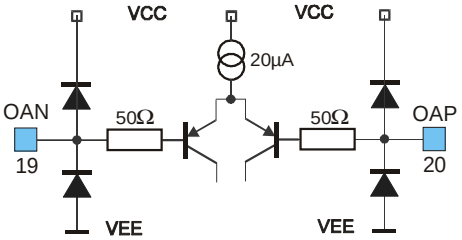
The following table depicts crystal, LO and image signals considering the examples of 868.3 MHz and 915 MHz RF reception at IF = 10.7 MHz.

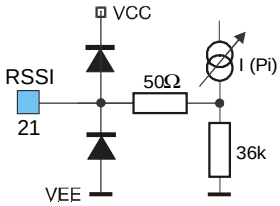
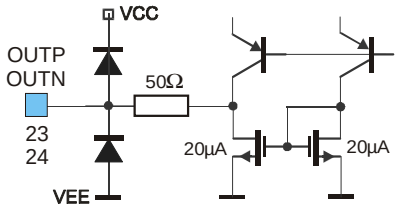
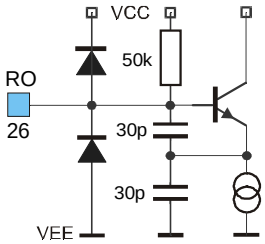
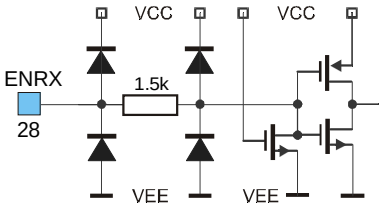
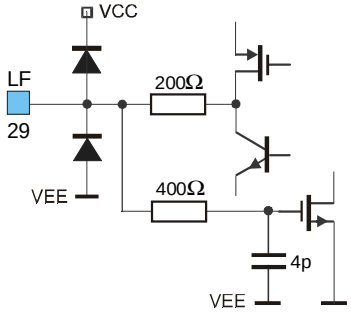
Signal type	RF = 868.3 MHz	RF = 868.3 MHz	RF = 915 MHz	RF = 915 MHz
Injection type	**low**	high	**low**	high
REF / MHz	**26.80000**	27.46875	**28.25938**	28.92813
LO / MHz	**857.6**	879.0	**904.3**	925.7
RF image / MHz	**846.9**	889.7	**893.6**	936.4

The selection of the reference crystal frequency is based on some assumptions. As for example: the image frequency should not be in a radio band where strong interfering signals might occur (because they could represent parasitic receiving signals), the LO signal should be in the range of 800 MHz to 930 MHz (because this is the optimum frequency range of the VCO1). Furthermore the IF should be as high as possible to achieve highest RF image rejection. The columns in bold depict the selected frequency plans to receive at 868.3 MHz and 915 MHz, respectively.

2 Pin Definitions and Descriptions

Pin No.	Name	I/O Type	Functional Schematic	Description
3	OUT_LNA	analog output		LNA open-collector output, to be connected to external LC tank that resonates at RF
31	IN_LNA	analog input		LNA input, approx. 26Ω single-ended
1	VEE_LNAC	ground		ground of LNA core (cascode)
2	GAIN_LNA	analog input		LNA gain control (input with hysteresis) RX standby: no pull-up RX active: pull-up
4	IN_MIX1	analog input		MIX1 input, approx. 33Ω single-ended
5	VEE_MIX	ground		ground of MIX1 and MIX2
6	IF1P	analog I/O		open-collector output, to be connected to external LC tank that resonates at first IF
7	IF1N	analog I/O		open-collector output, to be connected to external LC tank that resonates at first IF
8	VCC_MIX	supply		positive supply of MIX1 and MIX2
9	OUT_MIX2	analog output		MIX2 output, approx. 330Ω output impedance
10	VEE_IF	ground		ground of IFA and DEMOD

Pin No.	Name	I/O Type	Functional Schematic	Description
11	IN_IFA	analog input		IFA input, approx. 2.2kΩ input impedance
12	FBC1	analog I/O		to be connected to external IFA feedback capacitor
13	FBC2	analog I/O		to be connected to external IFA feedback capacitor
14	VCC_IF	supply		positive supply of IFA and DEMOD
15	OUT_IFA	analog I/O		IFA output and MIX3 input (of DEMOD)
16	IN_DEM	analog input		DEMOD input, to MIX3 core
17	VCC_BIAS	supply		positive supply of general bias system and OA
18	OUT_OA	analog output		OA output, 40uA current drive capability
19	OAN	analog input		negative OA input
20	OAP	analog input		positive OA input

Pin No.	Name	I/O Type	Functional Schematic	Description
21	RSSI	analog output		RSSI output, for RSSI and ASK detection, approx. 36kΩ output impedance
22	VEE_BIAS	ground		ground of general bias system and OA
23	OUTP	analog output		FSK/FM positive output, output impedance of 100kΩ to 300kΩ
24	OUTN	analog output		FSK/FM negative output, output impedance of 100kΩ to 300kΩ
25	VEE_RO	ground		ground of DIV, PFD, RO and charge pump
26	RO	analog input		RO input, Colpitts type oscillator with internal feed-back capacitors
27	VCC_PLL	supply		positive supply of DIV, PFD, RO and charge pump
28	ENRX	digital input		mode control input, CMOS-compatible with internal pull-down circuit
29	LF	analog I/O		charge pump output and VCO1 control input
30	VEE_LNA	ground		ground of LNA biasing
32	VCC_LNA	supply		positive supply of LNA biasing

3 Technical Data

3.1 Absolute Maximum Ratings

Parameter	Symbol	Condition / Note	Min	Max	Unit
Supply voltage	V_{CC}		0	7.0	V
Input voltage	V_{IN}		- 0.3	V_{cc}+0.3	V
Input RF level	P_{iRF}	@ LNA input		10	dBm
Storage temperature	T_{STG}		-40	+125	°C
Junction temperature	T_J			+150	°C
Thermal Resistance	R_{thJA}			60	K/W
Power dissipation	P_{diss}			0.1	W
Electrostatic discharge	V_{ESD1}	human body model, 1)	-1.0	+1.0	kV
	V_{ESD2}	human body model, 2)	-0.75	+0.75	

1) all pins except OUT_LNA, IF1P and IF1N
2) pin OUT_LNA, IF1P and IF1N

3.2 Normal Operating Conditions

Parameter	Symbol	Condition	Min	Max	Unit
Supply voltage	$V_{CC, FSK}$	0 °C to 85 °C	2.5	5.5	V
		-20 °C to 85 °C	2.6	5.5	
		-40 °C to 85 °C	2.7	5.5	
	$V_{CC, ASK}$	-40 °C to 85 °C	2.3	5.5	
Operating temperature	T_A		-40	+85	ºC
Input low voltage (CMOS)	V_{IL}	ENRX pin		0.3*V_{CC}	V
Input high voltage (CMOS)	V_{IH}	ENRX pin	0.7*V_{CC}		V
Input frequency range	f_i		800	930	MHz
IF range	f_{IF}		0.4	22	MHz
XOSC frequency	f_{ref}	set by the crystal	25	29.063	MHz
VCO frequency	f_{LO}	$f_{LO} = 32 \bullet f_{ref}$	800	930	MHz
Frequency deviation	Δf	at FSK or FM	±4	±120	kHz
FSK data rate	R_{FSK}	NRZ		40	kbit/s
ASK data rate	R_{ASK}	NRZ		80	kbit/s
FM bandwidth	f_m			15	kHz

3.3 Crystal Parameters

Parameter	Symbol	Condition	Min	Max	Unit
Crystal frequency	f_0	fundamental mode, AT	See para. 1.6.1		MHz
Load capacitance	C_L		10	15	pF
Static capacitance	C_0			7	pF
Series resistance	R_1			50	Ω

3.4 DC Characteristics

all parameters under normal operating conditions, unless otherwise stated;
typical values at T_A= 23 °C and V_{CC} = 3 V

Parameter	Symbol	Condition	Min	Typ	Max	Unit
Operating Currents						
Standby current	I_{SBY}	ENRX=0		50	100	nA
Supply current at low gain	$I_{CC, low}$	ENRX=1 GAIN_LNA=1	4.5	7.5	12.0	mA
Supply current at high gain	$I_{CC, high}$	ENRX=1 GAIN_LNA=0	5.0	9.2	14.0	mA
Digital Pin Characteristics						
Input low voltage CMOS	V_{IL}	ENRX pin	-0.3		$0.3*V_{cc}$	V
Input high voltage CMOS	V_{IH}	ENRX pin	$0.7*V_{CC}$		V_{CC}+0.3	V
Pull down current ENRX pin	I_{PDEN}	ENRX=1	0.1	2	10	µA
Low level input current ENRX pin	I_{INLEN}	ENRX=0			0.05	µA
Analog Pin Characteristics						
High level input current GAIN_LNA pin	$I_{INHGAIN}$	GAIN_LNA=1			0.05	µA
Pull up current GAIN_LNA pin active	$I_{PUGAINa}$	GAIN_LNA=0 ENRX=1	0.08	0.15	0.3	µA
Pull up current GAIN_LNA pin standby	$I_{PUGAINs}$	GAIN_LNA=0 ENRX=0			0.05	µA
High gain input voltage	V_{IHGAIN}	ENRX=1			0.7	V
Low gain input voltage	V_{ILGAIN}	ENRX=1	1.5			V
Opamp Characteristics						
Opamp input offset voltage	V_{offs}		-35		35	mV
Opamp input offset current	I_{offs}	$I_{OAP} - I_{OAN}$	-50		50	nA
Opamp input bias current	I_{bias}	$0.5 * (I_{OAP} + I_{OAN})$	-150		150	nA
RSSI Characteristics						
RSSI voltage at low input level	$V_{RSSI, low}$	P_i = -65 dBm, GAIN_LNA=1	0.5	1.0	1.5	V
RSSI voltage at high input level	$V_{RSSI, high}$	P_i = -35 dBm, GAIN_LNA=1	1.2	1.9	2.5	V

3.5 AC System Characteristics

all parameters under normal operating conditions, unless otherwise stated;
typical values at T_A = 23 °C and V_{CC} = 3 V,
RF at 868.3 MHz; SAW frond-end filter loss and IF at 10.7 MHz;
all parameters based on test circuits for FSK (Fig. 2) and ASK (Fig. 4), respectively;

Parameter	Symbol	Condition	Min	Typ	Max	Unit
Receive Characteristics						
Input sensitivity – FSK (narrow band)	$P_{min, n}$	B_{IF} = 40kHz $\Delta f = \pm 15$kHz (FSK/FM) BER ≤ $3 \cdot 10^{-3}$, 1)		-109		dBm
Input sensitivity – FSK (wide band)	$P_{min, w}$	B_{IF} = 150kHz $\Delta f = \pm 50$kHz (FSK/FM) BER ≤ $3 \cdot 10^{-3}$, 1)		-102		dBm
Input sensitivity – ASK (narrow band)	$P_{minA, n}$	B_{IF} = 40kHz BER ≤ $3 \cdot 10^{-3}$, 1)		-108		dBm
Input sensitivity – ASK (wide band)	$P_{minA, w}$	B_{IF} = 150kHz BER ≤ $3 \cdot 10^{-3}$, 1)		-104		dBm
Maximum input signal – FSK/FM	$P_{max, FSK}$	BER ≤ $3 \cdot 10^{-3}$ GAIN_LNA=1		0		dBm
Maximum input signal – ASK	$P_{max, ASK}$	BER ≤ $3 \cdot 10^{-3}$ GAIN_LNA=1		-10		dBm
Spurious emission	P_{spur}				-70	dBm
Image rejection	ΔP_{imag}			55		dB
Blocking immunity	ΔP_{block}	$\Delta f_{block} > \pm 2$MHz, 2)		57		dB
Start-up Parameters						
Start-up time – FSK/FM	T_{FSK}	ENRX from 0 to 1, valid data at output			0.9	ms
Start-up time – ASK	T_{ASK}	depends on ASK detector time constant, valid data at output			R3•C12 + T_{FSK}	ms
PLL Parameters						
VCO gain	K_{VCO}			350		MHz/V
Charge pump current	I_{CP}			60		µA

1) inclusive 3 dB loss of front-end SAW filter
2) desired signal with FSK/FM or ASK modulation, CW blocking signal

4 Test Circuits

4.1 FSK Reception

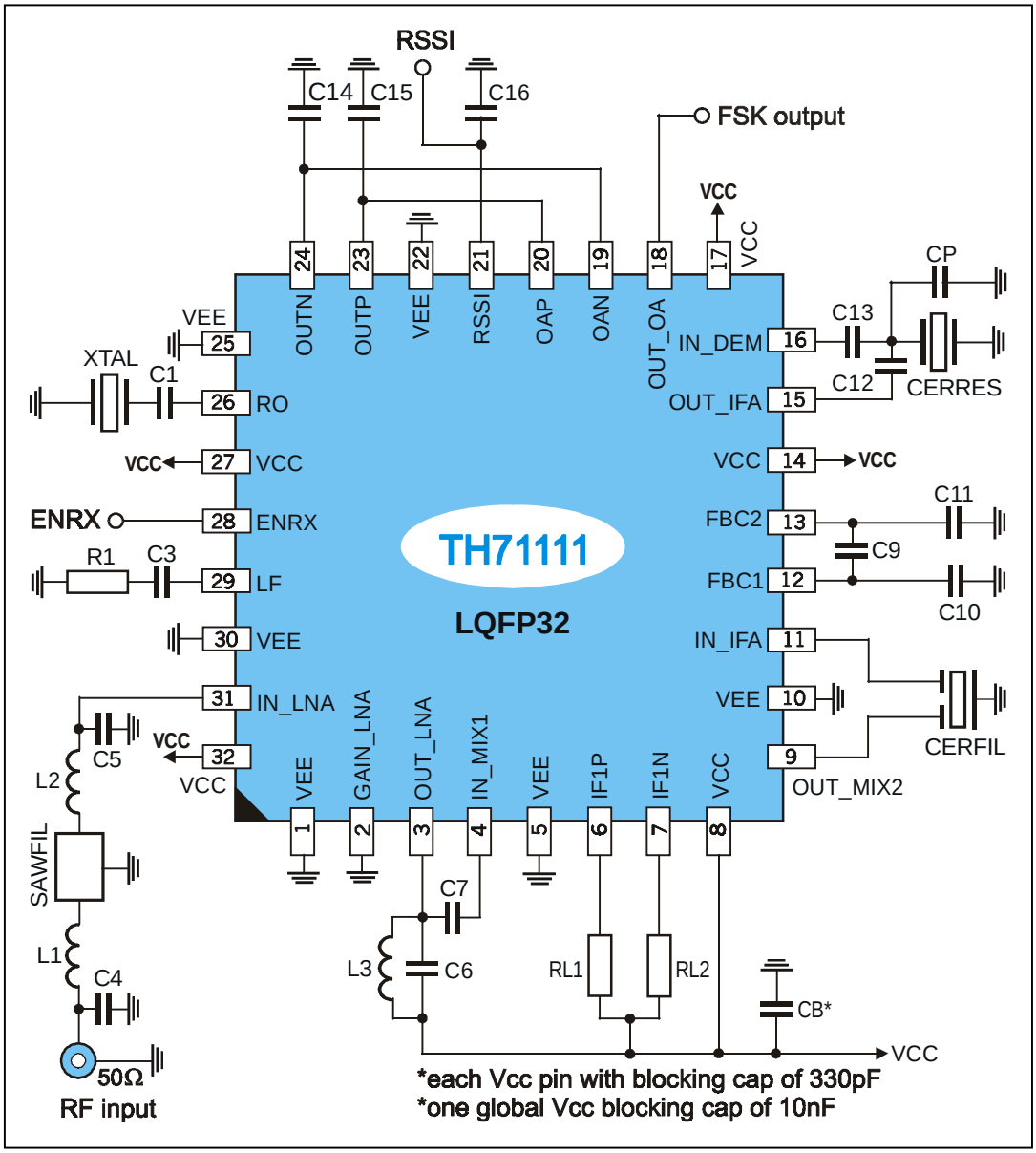


Fig. 2: Test circuit for FSK reception

4.2 FSK test circuit component list (Fig. 2)

Part	Size	Value / Type	Tolerance	Description
C1	0805	15 pF	±10%	crystal series capacitor
C3	0805	1 nF	±10%	loop filter capacitor
C4	0603	4.7 pF	±5%	capacitor to match to SAW filter input
C5	0603	2.7 pF	±5%	capacitor to match to SAW filter output
C6	0603	NIP	±5%	LNA output tank capacitor
C7	0603	1.2 pF	±5%	MIX1 input matching capacitor
C9	0805	33 nF	±10%	IFA feedback capacitor
C10	0603	1 nF	±10%	IFA feedback capacitor
C11	0603	1 nF	±10%	IFA feedback capacitor
C12	0603	1.5 pF	±5%	DEMOD phase-shift capacitor
C13	0603	680 pF	±10%	DEMOD coupling capacitor
CP	0805	10 – 12 pF	±5%	CERRES parallel capacitor
C14	0805	10 – 47 pF	±5%	demodulator output low-pass capacitor, depending on data rate
C15	0805	10 – 47 pF	±5%	demodulator output low-pass capacitor, depending on data rate
C16	0603	1.5 nF	±10%	RSSI output low-pass capacitor
R1	0805	10 kΩ	±10%	loop filter resistor
RL1	0805	470 Ω	±5%	MIX1 bias resistor
RL2	0805	470 Ω	±5%	MIX1 bias resistor
L1	0603	12 nH	±5%	inductor to match SAW filter
L2	0603	12 nH	±5%	inductor to match SAW filter
L3	0603	6.8 nH	±5%	LNA output tank inductor
XTAL	HC49 SMD	26.80000 MHz @ RF = 868.3 MHz	±25ppm calibration ±30ppm temp.	fundamental-mode crystal, C_{load} = 10 pF to 15pF, $C_{0,\,max}$ = 7 pF, $R_{m,\,max}$ = 50 Ω
SAWFIL	QCC8C	B3570 @ RF = 868.3 MHz	B_{3dB} = 1.7MHz	low-loss SAW filter from EPCOS
CERFIL	Leaded type	SFE10.7MFP @ B_{IF2} = 40 kHz	TBD	ceramic filter from Murata
	SMD type	SFECV10.7MJS-A @ B_{IF2} = 150 kHz	±40 kHz	
CERRES	SMD type	CDACV10.7MG18-A		ceramic demodulator tank from Murata

4.3 FSK/FM Circuit with AFC and Ceramic Resonator Compensation

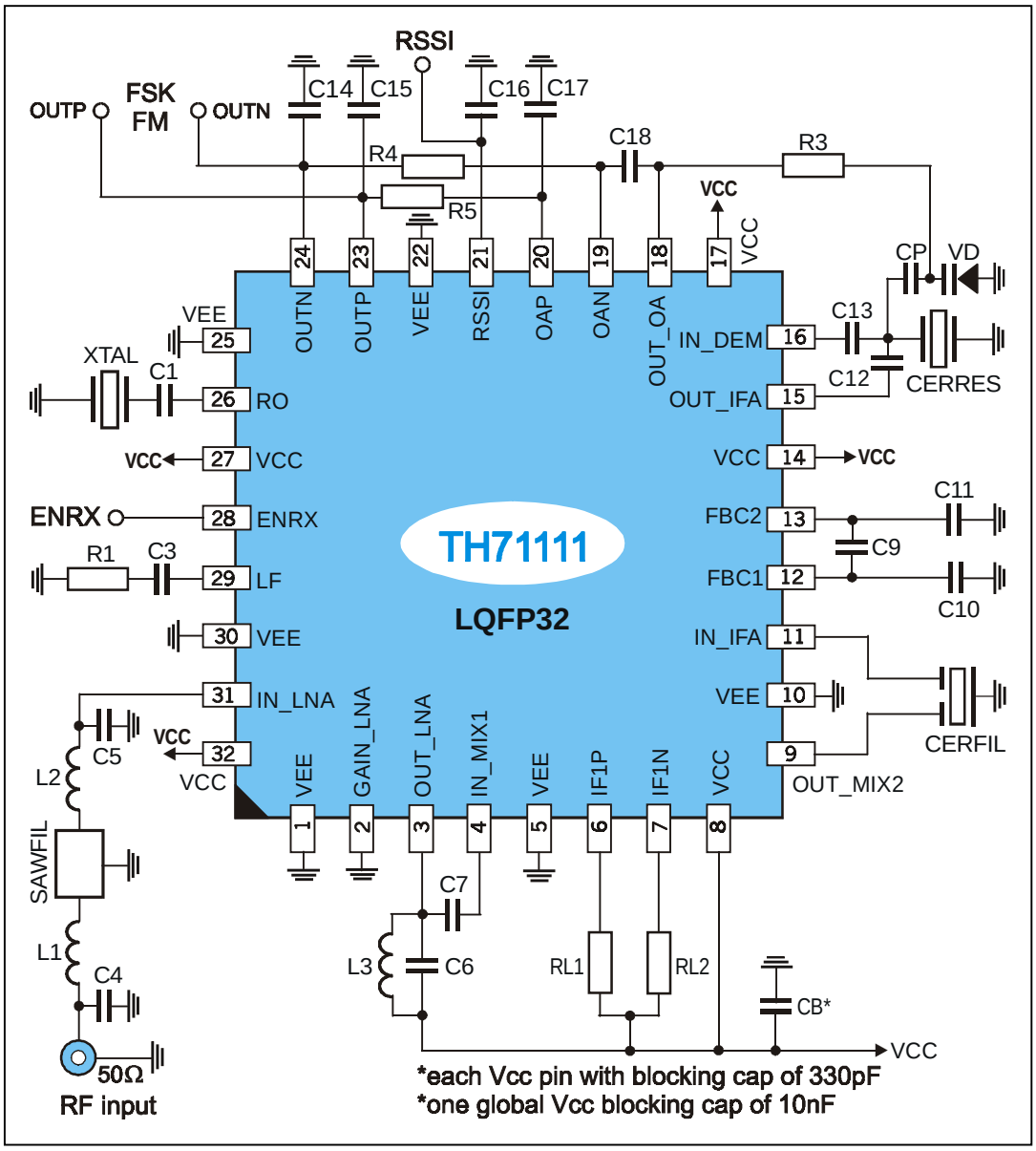


Fig. 3: Test circuit for FSK/FM with AFC and resonator compensation

Circuit Features

- ❑ Improves input frequency acceptance range up to RF_{nom} ±50 kHz
- ❑ Eliminates calibration tolerances of ceramic resonator
- ❑ Eliminates temperature tolerances of ceramic resonator
- ❑ Non-inverted and inverted CMOS-compatible outputs
- ❑ Recommended FM receiver configuration

4.4 FSK/FM (with AFC) test circuit component list (Fig.3)

Part	Size	Value / Type	Tolerance	Description
C1	0805	15 pF	±10%	crystal series capacitor
C3	0805	1 nF	±10%	loop filter capacitor
C4	0603	4.7 pF	±5%	capacitor to match to SAW filter input
C5	0603	2.7 pF	±5%	capacitor to match to SAW filter output
C6	0603	NIP	±5%	LNA output tank capacitor
C7	0603	1.2 pF	±5%	MIX1 input matching capacitor
C9	0805	33 nF	±10%	IFA feedback capacitor
C10	0603	1 nF	±10%	IFA feedback capacitor
C11	0603	1 nF	±10%	IFA feedback capacitor
C12	0603	1.5 pF	±5%	DEMOD phase-shift capacitor
C13	0603	680 pF	±10%	DEMOD coupling capacitor
CP	0805	10 – 12 pF	±5%	ceramic resonator loading capacitor
C14	0805	10 – 47 pF	±5%	demodulator output low-pass capacitor, depending on data rate
C15	0805	10 – 47 pF	±5%	demodulator output low-pass capacitor, depending on data rate
C16	0603	1.5 nF	±10%	RSSI output low-pass capacitor
C17		33 nF	±10%	integrator capacitor, fixed
C18	0805	33 nF	±10%	integrator capacitor, @ 0.5 to 2 kbit/s NRZ
		10 nF		integrator capacitor, @ 2 to 20 kbit/s NRZ
		1 nF		integrator capacitor, @ 20 to 40 kbit/s NRZ
R1	0805	10 kΩ	±10%	loop filter resistor
R3	0805	100 kΩ	±10%	varactor diode biasing resistor
R4	0805	680 kΩ	±10%	integrator resistor
R5	0805	680 kΩ	±10%	integrator resistor
RL1	0805	470 Ω	±5%	MIX1 bias resistor
RL2	0805	470 Ω	±5%	MIX1 bias resistor
L1	0603	12 nH	±5%	inductor to match SAW filter
L2	0603	12 nH	±5%	inductor to match SAW filter
L3	0603	6.8 nH	±5%	LNA output tank inductor
VD	SOD-323	BB535		varactor diode from Infineon
XTAL	HC49 SMD	26.80000 MHz @ RF = 868.3 MHz	±25ppm calibration ±30ppm temp.	fundamental-mode crystal, C_{load} = 10 pF to 15pF, $C_{0,\,max}$ = 7 pF, $R_{m,\,max}$ = 50 Ω
SAWFIL	QCC8C	B3570 @ RF = 868.3 MHz	B_{3dB} = 1.7MHz	low-loss SAW filter from EPCOS
CERFIL	Leaded type	SFE10.7MFP @ B_{IF2} = 40 kHz	TBD	ceramic filter from Murata
	SMD type	SFECV10.7MJS-A @ B_{IF2} = 150 kHz	±40 kHz	
CERRES	SMD type	CDACV10.7MG18-A		ceramic demodulator tank from Murata

4.5 ASK Reception

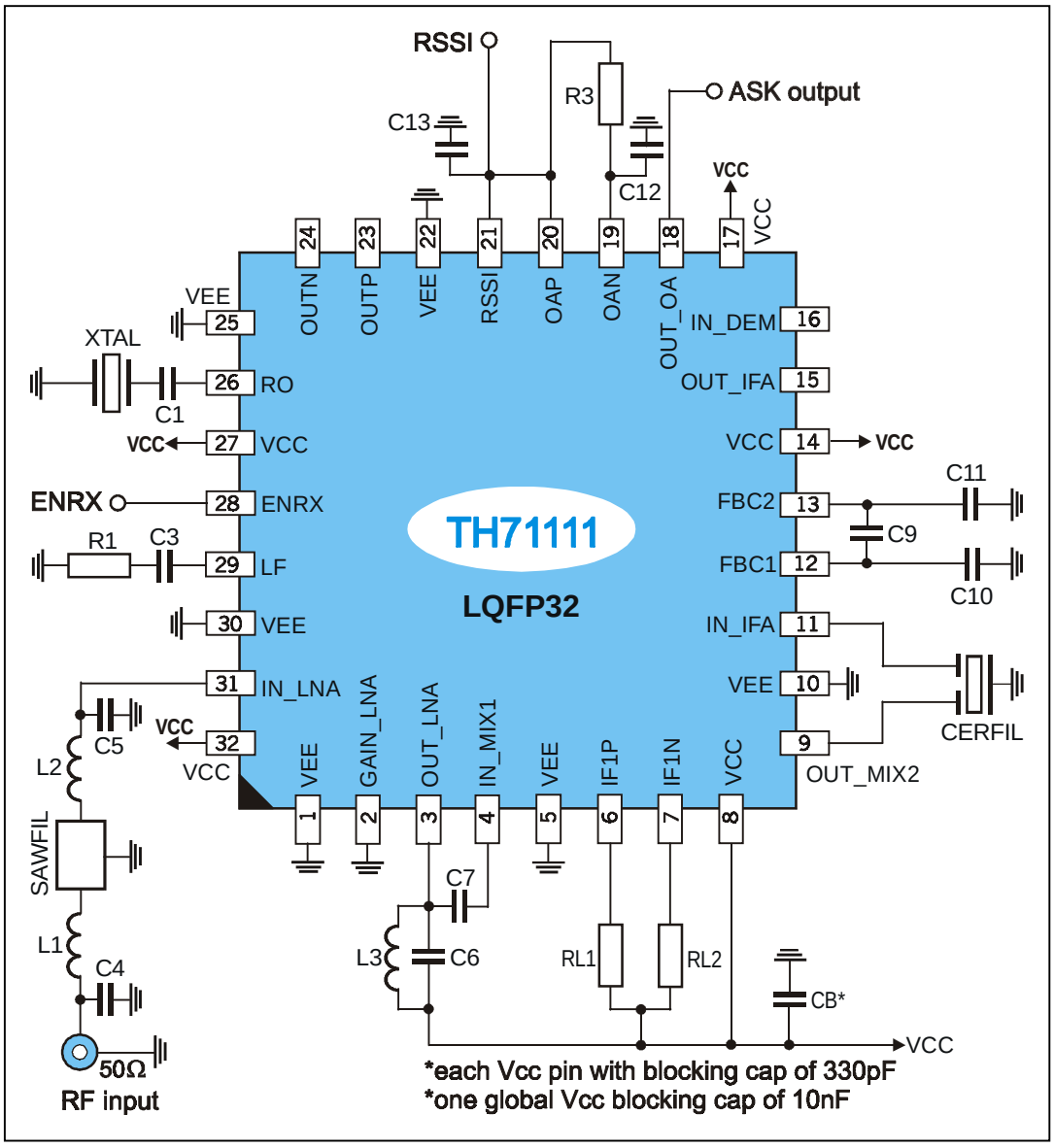


Fig. 4: Test circuit for ASK reception

4.6 ASK Test Circuit Component List (Fig. 4)

Part	Size	Value / Type	Tolerance	Description
C1	0805	15 pF	±10%	crystal series capacitor
C3	0805	1 nF	±10%	loop filter capacitor
C4	0603	4.7 pF	±5%	capacitor to match to SAW filter input
C5	0603	2.7 pF	±5%	capacitor to match to SAW filter output
C6	0603	NIP	±5%	LNA output tank capacitor
C7	0603	1.2 pF	±5%	MIX1 input matching capacitor
C9	0805	33 nF	±10%	IFA feedback capacitor
C10	0603	1 nF	±10%	IFA feedback capacitor
C11	0603	1 nF	±10%	IFA feedback capacitor
C12	0805	1 nF to 100 nF	±10%	ASK data slicer capacitor, depending on data rate
C13	0603	1.5 nF	±10%	RSSI output low-pass capacitor
R1	0805	10 kΩ	±10%	loop filter resistor
R3	0603	100 kΩ	±5%	ASK data slicer resistor, depending on data rate
RL1	0805	470 Ω	±5%	MIX1 bias resistor
RL2	0805	470 Ω	±5%	MIX1 bias resistor
L1	0603	12 nH	±5%	inductor to match SAW filter
L2	0603	12 nH	±5%	inductor to match SAW filter
L3	0603	6.8 nH	±5%	LNA output tank inductor
XTAL	HC49 SMD	26.80000 MHz @ RF = 868.3 MHz	±25ppm calibration ±30ppm temp.	fundamental-mode crystal, C_{load} = 10 pF to 15pF, $C_{0,\,max}$ = 7 pF, $R_{m,\,max}$ = 50 Ω
SAWFIL	QCC8C	B3570 @ RF = 868.3 MHz	B_{3dB} = 1.7MHz	low-loss SAW filter from EPCOS
CERFIL	leaded type	SFE10.7MFP @ B_{IF2} = 40 kHz	TBD	ceramic filter from Murata
	SMD type	SFECV10.7MJS-A @ B_{IF2} = 150 kHz	±40 kHz	

5 Package Dimensions

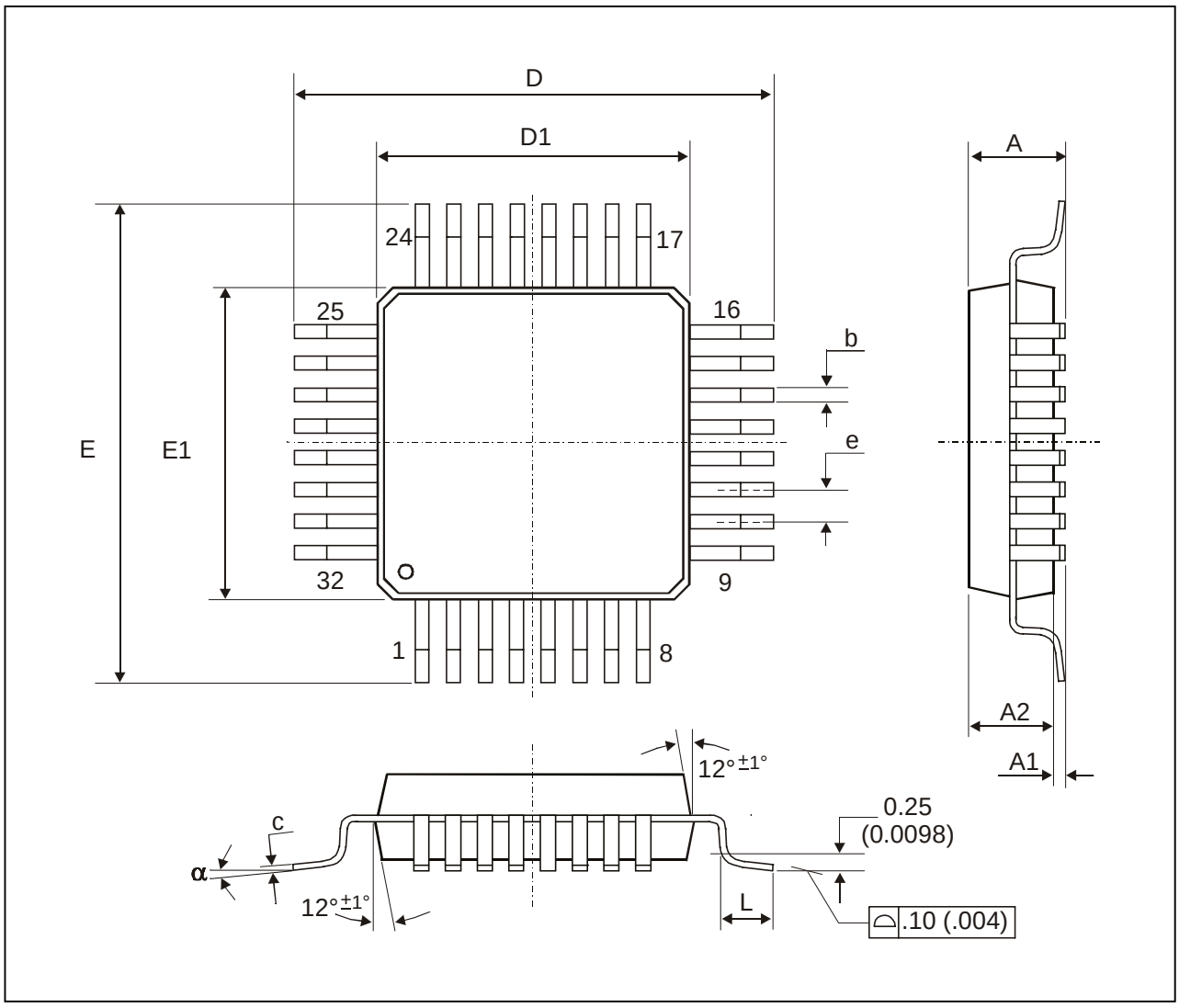


Fig. 5: LQFP32 (Low profile Quad Flat Package)

All Dimension in mm, coplanarity < 0.1mm										
	E1, D1	**E, D**	**A**	**A1**	**A2**	**e**	**b**	**c**	**L**	**α**
min max	7.00	9.00	1.40 1.60	0.05 0.15	1.35 1.45	0.8	0.30 0.45	0.09 0.20	0.45 0.75	0° 7°
All Dimension in inch, coplanarity < 0.004"										
min max	0.276	0.354	0.055 0.063	0.002 0.006	0.053 0.057	0.031	0.012 0.018	0.0035 0.0079	0.018 0.030	0° 7°

6 Reliability Information

Melexis devices are classified and qualified regarding suitability for infrared, vapor phase and wave soldering with usual (63/37 SnPb-) solder (melting point at 183degC).
The following test methods are applied:

- IPC/JEDEC J-STD-020A (issue April 1999)
  Moisture/Reflow Sensitivity Classification For Nonhermetic Solid State Surface Mount Devices
- CECC00802 (issue 1994)
  Standard Method For The Specification of Surface Mounting Components (SMDs) of Assessed Quality
- MIL 883 Method 2003 / JEDEC-STD-22 Test Method B102
  Solderability

For all soldering technologies deviating from above mentioned standard conditions (regarding peak temperature, temperature gradient, temperature profile etc) additional classification and qualification tests have to be agreed upon with Melexis.

The application of Wave Soldering for SMD's is allowed only after consulting Melexis regarding assurance of adhesive strength between device and board.

For more information on manufacturability/solderability see quality page at our website:
http://www.melexis.com/

7 ESD Precautions

Electronic semiconductor products are sensitive to Electro Static Discharge (ESD).
Always observe Electro Static Discharge control procedures whenever handling semiconductor products.

8 Disclaimer

Devices sold by Melexis are covered by the warranty and patent indemnification provisions appearing in its Term of Sale. Melexis makes no warranty, express, statutory, implied, or by description regarding the information set forth herein or regarding the freedom of the described devices from patent infringement. Melexis reserves the right to change specifications and prices at any time and without notice. Therefore, prior to designing this product into a system, it is necessary to check with Melexis for current information. This product is intended for use in normal commercial applications. Applications requiring extended temperature range, unusual environmental requirements, or high reliability applications, such as military, medical life-support or life-sustaining equipment are specifically not recommended without additional processing by Melexis for each application.
The information furnished by Melexis is believed to be correct and accurate. However, Melexis shall not be liable to recipient or any third party for any damages, including but not limited to personal injury, property damage, loss of profits, loss of use, interrupt of business or indirect, special incidental or consequential damages, of any kind, in connection with or arising out of the furnishing, performance or use of the technical data herein. No obligation or liability to recipient or any third party shall arise or flow out of Melexis' rendering of technical or other services.

For the latest version of this document. Go to our website at
www.melexis.com

Or for additional information contact Melexis Direct:

Europe and Japan:
Phone: +32 1367 0495
E-mail: sales_europe@melexis.com

All other locations:
Phone: +1 603 223 2362
E-mail: sales_usa@melexis.com