



October 2006

# FSHDMI04 Wide-Bandwidth Differential Signaling HDMI Switch

## Features

- 1.65 Gbps throughput
- 8kV ESD protection
- -26dB non-adjacent channel crosstalk at 825MHz
- Isolation ground between channels
- Low skew
  - Inter-pair skew <150ps
  - Intra-pair skew <90ps
- Fast turn on/off time
- Low power consumption (1µA maximum)
- Control input: TTL compatible

## Applications

- UXGA and 1080p DVI and HDMI video source selection

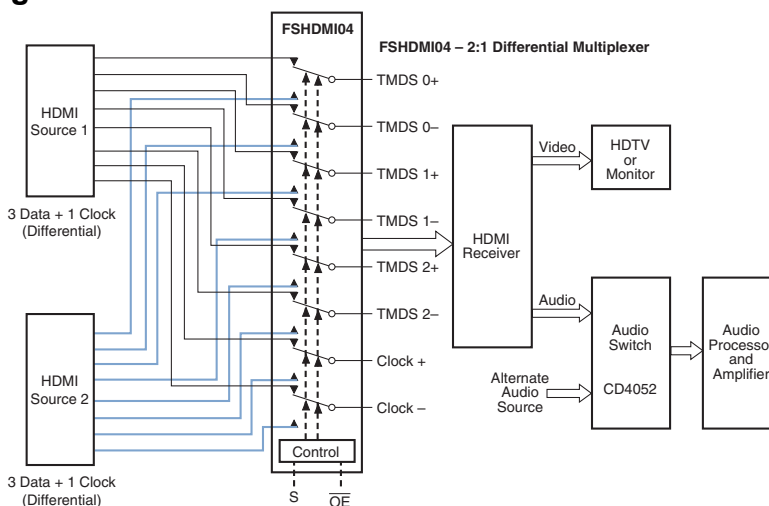
## General Description

The FSHDMI04 is a wide bandwidth switch for routing HDMI Link Data and Clock signals. This device supports data rates up to 1.65Gbps per channel for UXGA resolution. It can also be used to switch TMDS-based DVI digital video streams. Possible applications include LCD TV, DVD, Set-Top Box, notebook computers and other designs with multiple digital video interfaces. The FSHDMI04 switch allows the passage of HDMI link signals with low non-adjacent channel crosstalk and superior OFF-Isolation. This performance is critical to minimize ghost images between active video sources in video applications. The wide bandwidth of this switch allows the high speed differential signal to pass through the switch with minimal additive skew and phase jitter.

## Ordering Information

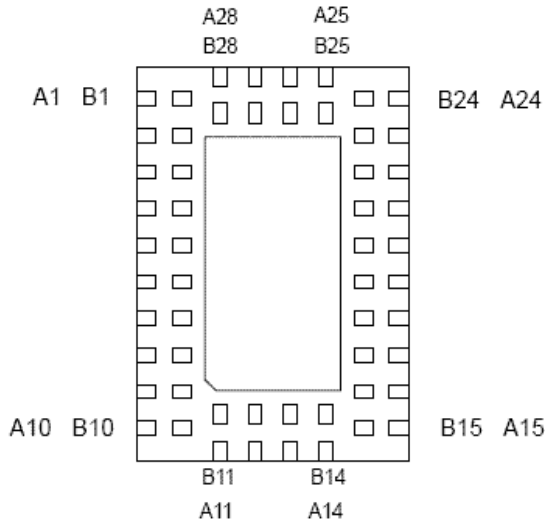
Order Number	Package Number	Package Description
FSHDMI04QSPX	MQA48A	48-Lead Quarter Size Very Small Outline Package (QVSOP), JEDEC MO-154, 0.150inches Wide
FSHDMI04MTDX	MTD48	48-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 6.1mm Wide
FSHDMI04BQX (Preliminary)	MLP56	56-Lead Molded Leadless Package (MLP), 5x7mm Wide

## Applications Diagram



FSHDMI04 Wide-Bandwidth Differential Signaling HDMI Switch

### Pin Assignments



Pin	Function	Pin	Function	Pin	Function
A1	NC	A21	C1-	B13	NC
A2	2C0-	A22	C1+	B14	C3-
A3	1C1+	A23	VCC	B15	GND
A4	1C1-	A24	NC	B16	C3+
A5	2C1-	A25	GND	B17	VCC
A6	GND	A26	VCC	B18	GND
A7	1C2+	A27	Vcc	B19	NC
A8	1C2-	A28	GND	B20	NC
A9	GND	B1	2C0+	B21	GND
A10	NC	B2	1C0-	B22	GND
A11	2C3-	B3	GND	B23	C0-
A12	GND	B4	2C1+	B24	GND
A13	VCC	B5	NC	B25	C0+
A14	GND	B6	NC	B26	NC
A15	NC	B7	2C2+	B27	NC
A16	GND	B8	2C2-	B28	1C0+
A17	C2-	B9	1C3+		
A18	C2+	B10	2C3+		
A19	OE	B11	1C3-		
A20	S	B12	NC		

Figure 1. MLP Pin Assignments

### Pin Assignments

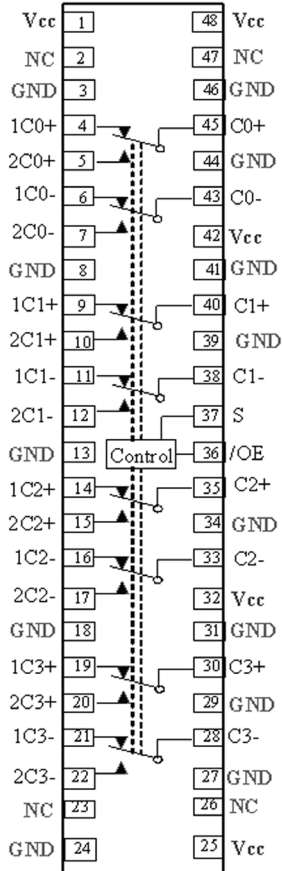


Figure 2. QVSOP and TSSOP Pin Assignments

### Truth Table

S	$\overline{OE}$	Function
X	H	Disconnected
L	L	$1C_n = C_n$
H	L	$2C_n = C_n$

### Pin Descriptions

Pin Name	Description
$\overline{OE}$	Bus Switch Enable
S	Select Input
$1C_n, 2C_n, C0_n, C1_n, C2_n, C3_n$	Data Ports

## Absolute Maximum Ratings

The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the Electrical Characteristics tables are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table defines the conditions for actual device operation.

Symbol	Parameter	Rating
$V_{CC}$	Supply Voltage	-0.5V to +4.6V
$V_S$	DC Switch Voltage	-0.5V to $V_{CC} + 0.05$
$V_{IN}$	DC Input Voltage <sup>(1)</sup>	-0.5V to +4.6V
$I_{IK}$	DC Input Diode Current	-50 mA
$I_{OUT}$	DC Output Sink Current	128 mA
$T_{STG}$	Storage Temperature Range	-65°C to +150°C
	ESD, Human Body Model	8,000V

## Recommended Operating Conditions<sup>(2)</sup>

Symbol	Parameter	Rating
$V_{CC}$	Power Supply Operating	3.0V to 3.6V
$V_{IN}$	Control Input Voltage	0V to $V_{CC}$
	Switch Input Voltage	0V to $V_{CC}$
$T_A$	Operating Temperature	-40°C to 85°C

## DC Electrical Characteristics

All typical values are for  $V_{CC} = 3.3V$  @ 25°C unless otherwise specified.

Symbol	Parameter	Conditions	$V_{CC}$ (V)	$T_A = -40^\circ\text{C to } +85^\circ\text{C}$			Units
				Min.	Typ.	Max.	
$V_{IK}$	Clamp Diode Voltage	$I_{IN} = -18\text{mA}$	3.0			-1.2	V
$V_{IH}$	Input Voltage HIGH		3.0–3.6	2.0			V
$V_{IL}$	Input Voltage LOW		3.0–3.6			0.8	V
$I_{IN}$	Control Input Leakage	$V_{IN} = 0$ to $V_{CC}$	3.6			$\pm 1.0$	$\mu\text{A}$
$I_{OZ}$	OFF-STATE Leakage	$0 \leq nC_n, C_n \leq V_{CC}$	3.6			$\pm 1.0$	$\mu\text{A}$
$R_{ON}$	Switch On Resistance <sup>(3)</sup>	$V_{IN} = V_{CC} - 0.6$ to $V_{CC}$ , $I_{ON} = 10\text{mA}$	3.0		12.0	19.0	$\Omega$
$R_{ON(FLAT)}$	Switch On Resistance Flatness <sup>(4)</sup>	$V_{IN} = V_{CC} - 0.6$ to $V_{CC}$ , $I_{ON} = 10\text{mA}$	3.0		1.0		$\Omega$
$I_{CC}$	Quiescent Supply Current	$V_{IN} = 0$ or $V_{CC}$ , $I_{OUT} = 0$	3.6			1.0	$\mu\text{A}$

### Notes:

1. The input and output negative voltage ratings may be exceeded if the input and output diode current ratings are observed.
2. Unused control inputs must be held HIGH or LOW. They may not float.
3. Measured by the voltage drop between A and B pins at the indicated current through the switch. On resistance is determined by the lower of the voltages on the two (A or B) pins.
4. Flatness is defined as the difference between the maximum and minimum value on resistance over the specified range of conditions.

## AC Electrical Characteristics

All typical values are for  $V_{CC} = 3.3V$  @  $25^{\circ}C$  unless otherwise specified.

Symbol	Parameter	Conditions	$V_{CC}$ (V)	$T_A = -40^{\circ}C$ to $+85^{\circ}C$			Units	Figure Number
				Min.	Typ.	Max.		
$t_{ON}$	Turn ON Time S, $\overline{OE}$ -to-Output	$V_{IN} = V_{CC} - 0.5$ , $R_{PU} = 50\Omega$ , $C_L = 5pF$	3.0 to 3.6		4.0	6.0	ns	Figure 7 Figure 8
$t_{OFF}$	Turn OFF Time S, $\overline{OE}$ -to-Output	$V_{IN} = V_{CC} - 0.5$ , $R_{PU} = 50\Omega$ , $C_L = 5pF$	3.0 to 3.6		2.0	4.0	ns	Figure 7 Figure 8
$t_{BBM}$	Break-Before-Make Time	$V_{IN} = V_{CC} - 0.5$ , $R_{PU} = 20\Omega$ , $C_L = 5pF$	3.0 to 3.6		3.0			Figure 14
$t_{PD}$ ( $t_{PLH}$ , $t_{PHL}$ )	Switch Propagation Delay	$R_{PU} = 50\Omega$ , $C_L = 5pF$	3.0 to 3.6			250	ps	Figure 7 Figure 13
$T_{JITTER}$	Total Jitter (DJ + RJ)	$f = 165MHz$ Clock with 50% Duty Cycle, $R_{PU} = 50\Omega$ , $C_L = 5pF$	3.0 to 3.6		55.0		ps	Figure 7
$T_{RATIO}$	Duty Cycle Ratio				50.0		%	
$T_{SK1}$	Intra-Pair Skew $C_{n+}$ to $C_{n-}$ <sup>(5)</sup>	$f = 1.65Gbps$ , $2^{23}-1$ PRBS $R_{PU} = 50\Omega$ , $C_L = 5pF$	3.0 to 3.6		55.0	90.0	ps	Figure 7 Figure 13
$T_{SK2}$	Inter-Pair Skew <sup>(5)</sup> (Between any two switch paths)	$f = 1.65Gbps$ , $2^{23}-1$ PRBS $R_{PU} = 50\Omega$ , $C_L = 5pF$	3.0 to 3.6		90.0	150.0	ps	Figure 7 Figure 13
$O_{IRR}$	OFF-Isolation	$R_T = 50\Omega$ , $f = 370MHz$	3.0 to 3.6		-35.0		dB	Figure 9
		$R_T = 50\Omega$ , $f = 825MHz$	3.0 to 3.6		-25.0			
$X_{talk}$	Non-Adjacent Channel Crosstalk	$R_T = 50\Omega$ , $f = 370MHz$	3.0 to 3.6		-30.0		dB	Figure 10
		$R_T = 50\Omega$ , $f = 825MHz$	3.0 to 3.6		-26.0			
$f_{MAX}$	Maximum Throughput		3.3		1.65		Gbps	

### Notes:

5. Guaranteed by characteristics and design.

## Capacitance

Symbol	Parameter	Conditions	$T_A = -40^{\circ}C$ to $+85^{\circ}C$			Units
			Min.	Typ.	Max.	
$C_{IN}$	Control Pin Input Capacitance	$V_{CC} = 0V$		1.1		pF
$C_{ON}$	$nC_n$ ON Capacitance	$V_{CC} = 3.3V$		6.0		pF
$C_{OFF}$	Port $C_n$ OFF Capacitance	$V_{CC} = 3.3V$		2.5		pF

## Typical Characteristics

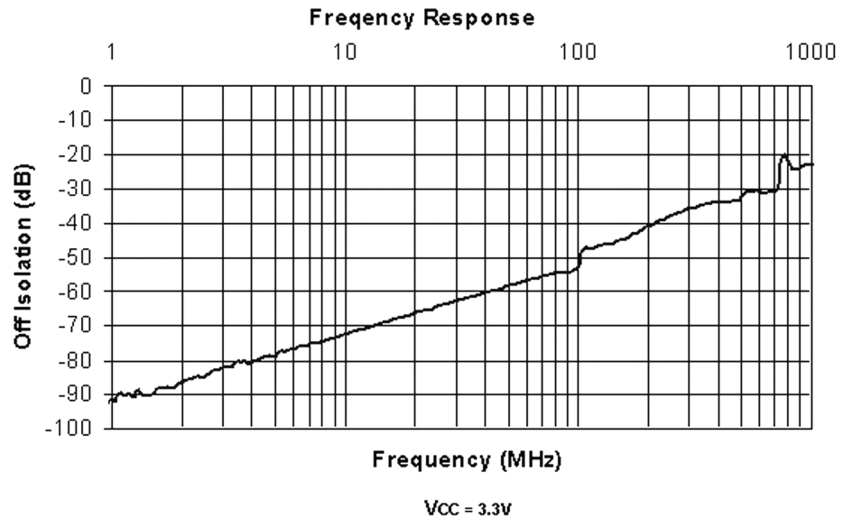


Figure 3. Off- Isolation, V<sub>CC</sub> = 3.3V

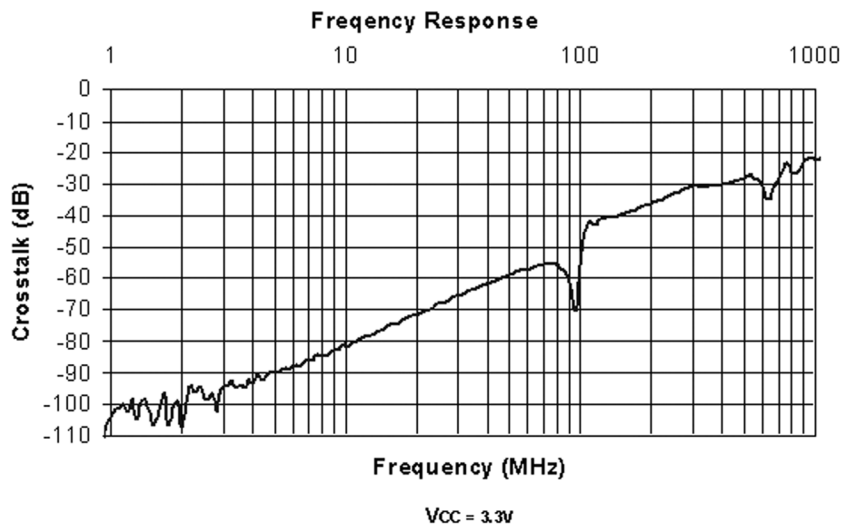
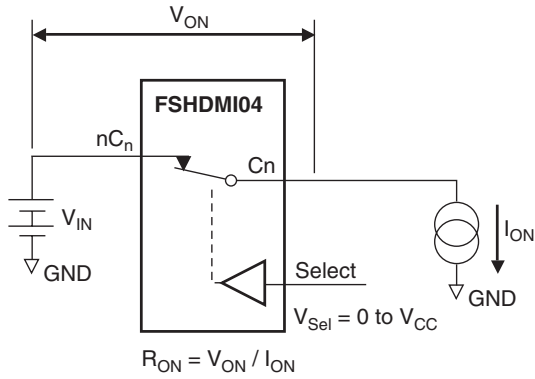
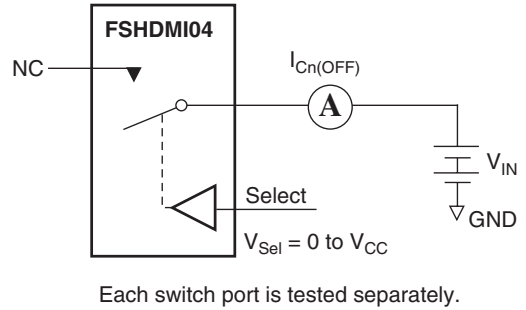


Figure 4. Crosstalk, V<sub>CC</sub> = 3.3CV

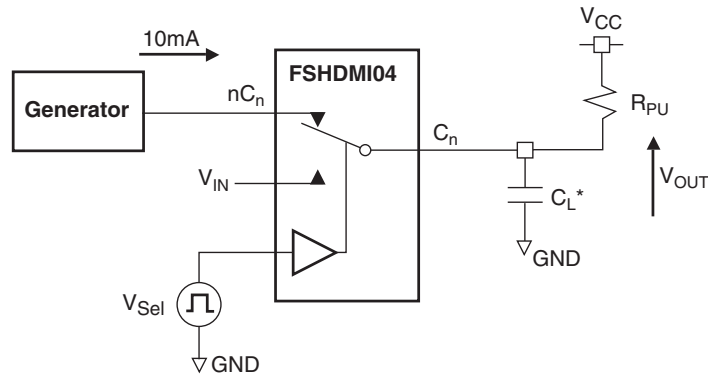
### Test Diagrams



**Figure 5. On Resistance**



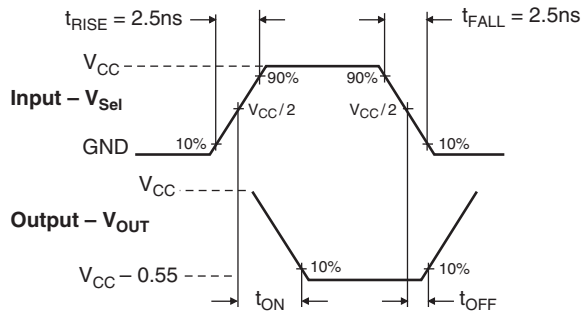
**Figure 6. OFF Leakage**



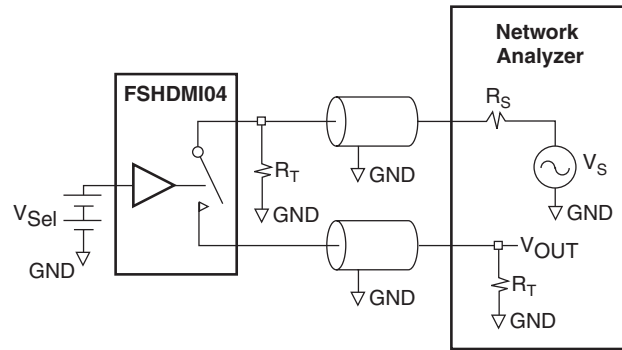
$R_{PU}$  and  $C_L$  are functions of application environment (see AC/DC Tables for values of  $C_L$  and  $R_{PU}$ )  
 \* $C_L$  includes fixture and stray capacitance

**Figure 7. AC Test Circuit Load**

**Test Diagrams (Continued)**

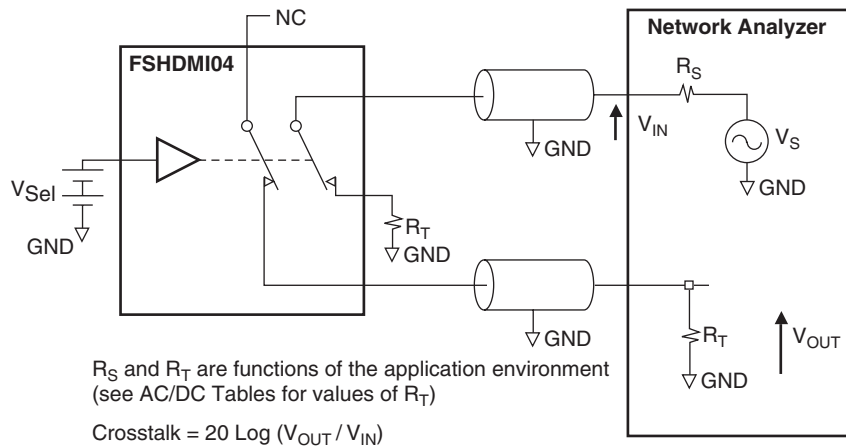


**Figure 8. Turn ON / Turn OFF Waveforms**



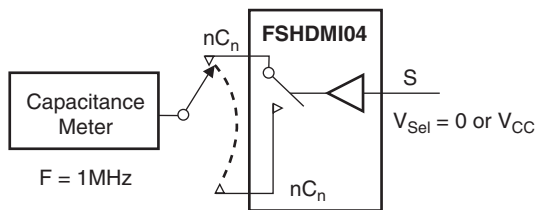
$R_S$  and  $R_T$  are functions of the application environment (see AC/DC Tables for values of  $R_T$ )  
 OFF-Isolation =  $20 \text{ Log } (V_{OUT} / V_{IN})$

**Figure 9. Channel OFF-Isolation**

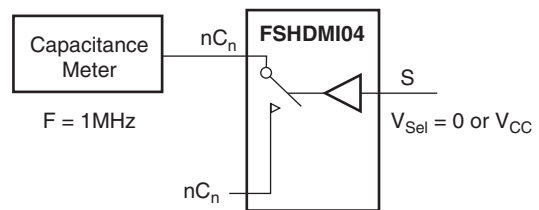


$R_S$  and  $R_T$  are functions of the application environment (see AC/DC Tables for values of  $R_T$ )  
 Crosstalk =  $20 \text{ Log } (V_{OUT} / V_{IN})$

**Figure 10. Non-adjacent Channel-to-Channel Crosstalk**

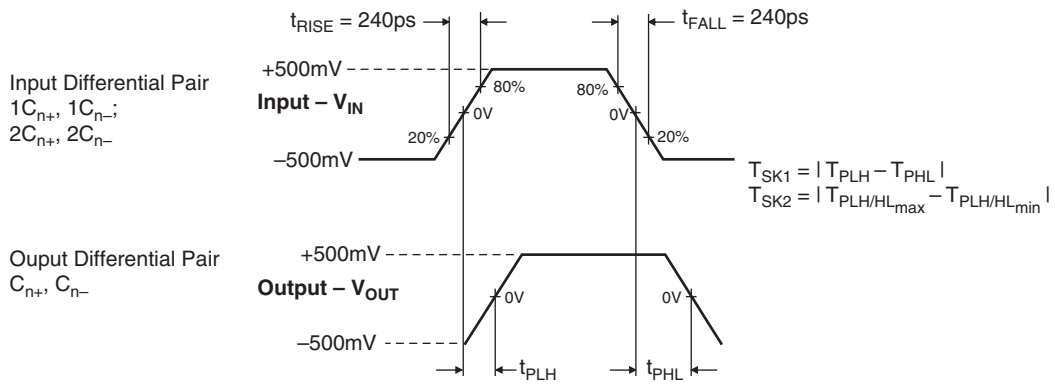


**Figure 11. Channel OFF-Capacitance**

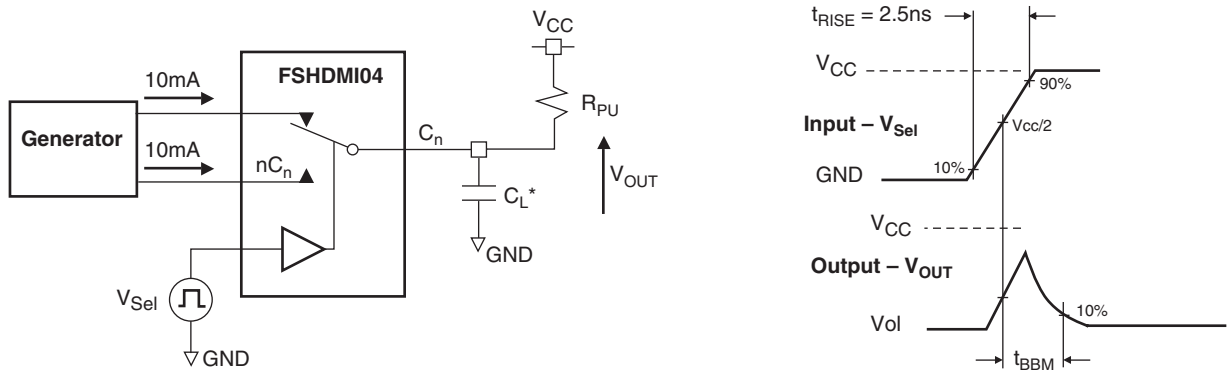


**Figure 12. Channel ON-Capacitance**

**Test Diagrams (Continued)**



**Figure 13. Intra- and Inter-Pair Skew,  $t_{PD}$**



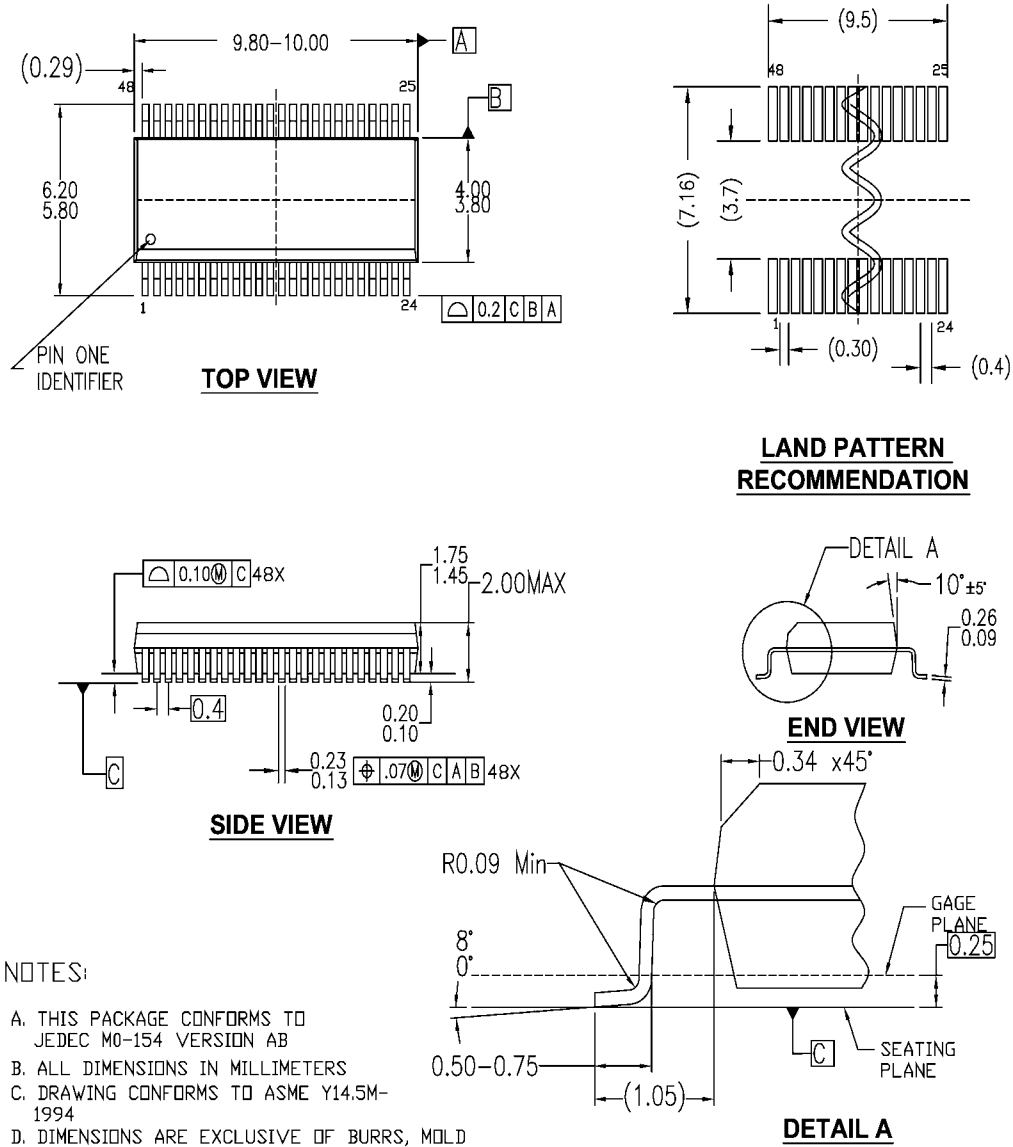
$R_{PU}$  and  $C_L$  are functions of application environment (see AC/DC Tables for values of  $C_L$  and  $R_{PU}$ )  
 $*C_L$  includes fixture and stray capacitance

**Figure 14. Break-Before-Make**



## Physical Dimensions

Dimensions are in millimeters unless otherwise noted.

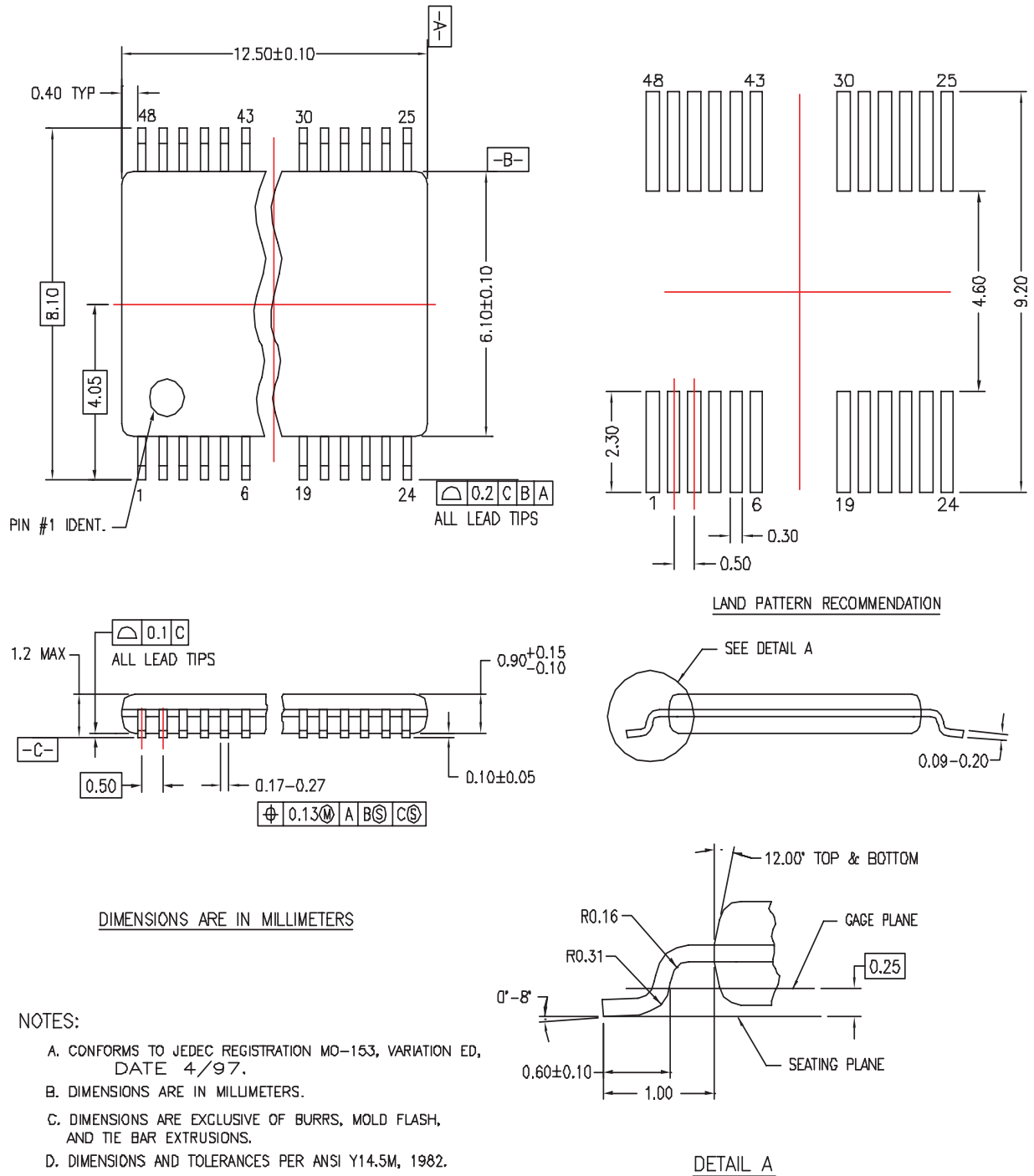


MQA48AREVA

Figure 15. 48-Lead Quarter Size Very Small Outline Package (QVSOP), JEDEC MO-154, 0.150inches Wide

### Physical Dimensions (Continued)

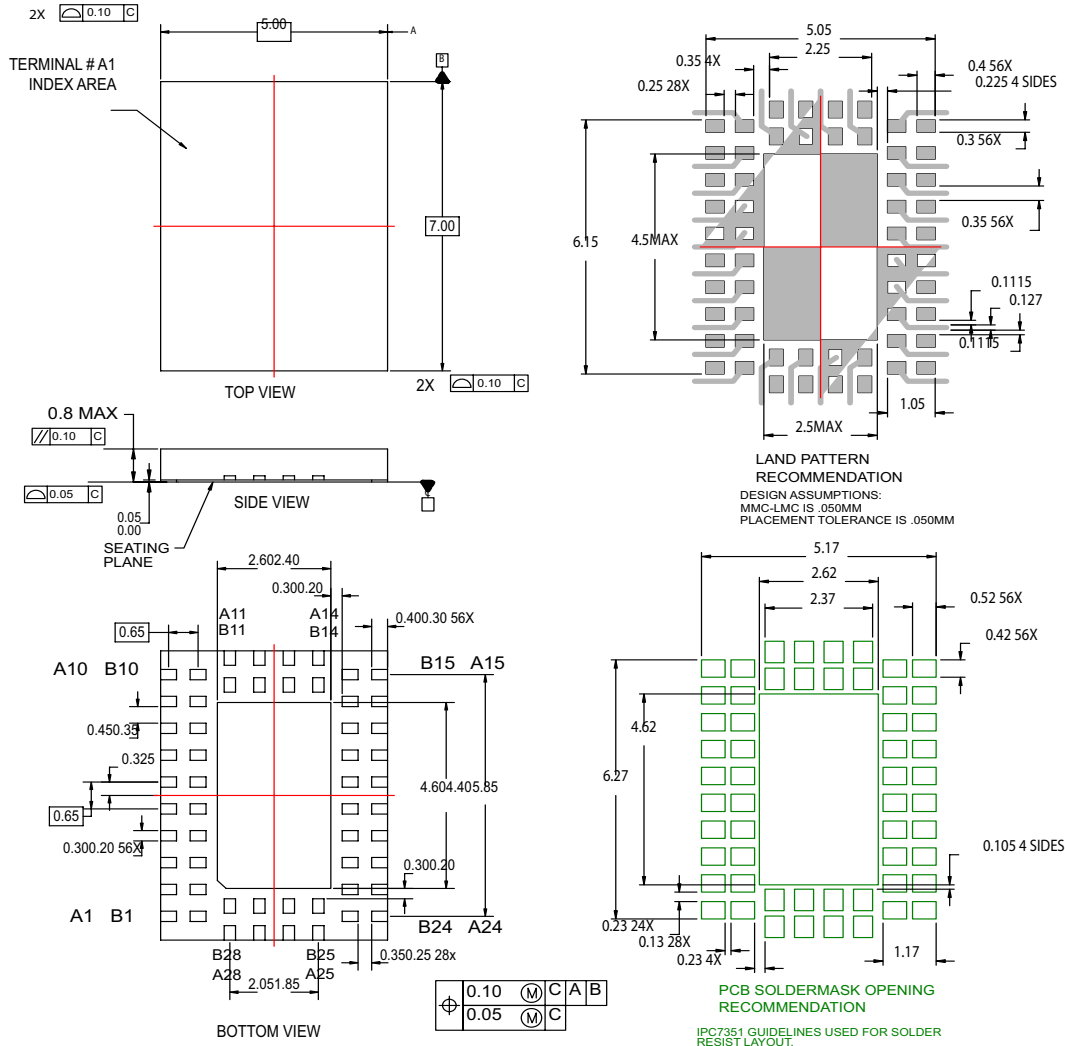
Dimensions are in millimeters unless otherwise noted.



**Figure 16. 48-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 6.1mm Wide**

### Physical Dimensions (Continued)

Dimensions are in millimeters unless otherwise noted.



**NOTES:**

- A. NOT CURRENTLY REGISTERED WITH ANY STANDARDS BODY.
- B. DIMENSIONS ARE IN MILLIMETERS.
- C. DIMENSIONS AND TOLERANCES PER ASME Y14.5M, 1994
- D. PRELIMINARY DRAWING SUBJECT TO REVISION.

MLP56Arev2

**Figure 17. 56-Lead Molded Leadless Package (MLP) 5x7mm**

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Datasheet Identification	Product Status	Definition
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