19-3741; Rev 1; 8/10

MAX1434/MAX1436/MAX1437/MAX1438 Evaluation Kits

General Description

The MAX1434/MAX1436/MAX1437/MAX1438 evaluation kits (EV kits) are fully assembled and tested circuit boards that contain all the components necessary to evaluate the performance of this family of octal 10-/12-bit analog-to-digital converters (ADCs). These ADCs accept differential analog input signals. The EV kits generate these signals from user-provided single-ended input sources. The EV kits' digital outputs can be easily sampled with a user-provided high-speed logic analyzer or data-acquisition system. The EV kits also feature an on-board deserializer to simplify integration with standard logic analysis systems. The EV kits operate from 1.8V and 3.3V (plus 1.5V if the FPGA is used) power supplies and include circuitry that generates a clock signal from an AC signal provided by the user.

Features

- **Low-Voltage and Low-Power Operation**
- **Optional On-Board Clock-Shaping Circuitry**
- **Serial Scalable Low-Voltage Signaling (SLVS)/Low-Voltage Differential Signaling (LVDS) Outputs**
- **On-Board LVPECL Differential Output Drivers**
- **On-Board Deserializer**
- **LVDS Test Mode**
- **Fully Assembled and Tested**

Part Selection Table

PART NUMBER	BITS	SPEED (Msps)
MAX1434ECQ+D	10	50
MAX1436ECQ+D	12	40
MAX1437ECQ+D	12	50
MAX1438ECQ+D	12	65

+Denotes lead(Pb)-free and RoHS compliant.
D = Dry Pack.

Ordering Information

PART	TYPE
MAX1434EVKIT	EV Kit
MAX1436EVKIT	EV Kit
MAX1437EVKIT	EV Kit
MAX1438EVKIT	EV Kit

Component List

DESIGNATION	QTY	DESCRIPTION
C1–C8, C10, C11, C12, C57–C64, C81–C85, C139, C140, C147–C156	36	0.1µF ±10%, 10V X5R ceramic capacitors (0402) TDK C1005X5R1A104K
C9, C29–C44, C56, C77, C78, C80, C92, C93, C134–C137, C146	28	1.0µF ±10%, 6.3V X5R ceramic capacitors (0402) TDK C1005X5R0J105K
C13–C20, C65–C72	0	Not installed, ceramic capacitors (0603)
C21–C28, C126–C133	16	39pF ±5%, 50V C0G ceramic capacitors (0402) TDK C1005C0G1H390J
C45, C46, C47, C86–C89, C143	8	220µF ±20%, 6.3V tantalum capacitors (C-case) AVX TPSC227M006R0250
C48, C49, C50, C144	0	Not installed, capacitors (C-case)
C51, C52, C53, C90, C91, C145	6	10µF ±10%, 10V X5R ceramic capacitors (1210) TDK C3225X5R1A106K
C54	1	2.2µF ±20%, 6.3V X5R ceramic capacitor (0603) TDK C1608X5R0J225M
C55, C157–C176	21	0.01µF ±10%, 25V X7R ceramic capacitors (0402) TDK C1005X7R1E103K
C73–C76, C122–C125	0	Not installed, ceramic capacitors (0402)

Component List (continued)

DESIGNATION	QTY	DESCRIPTION
C79, C138, C142	3	10µF ±10%, 4V X5R ceramic capacitors (0603) TDK C1608X5R0G106K
C94–C121	28	0.1µF ±20%, 6.3V X5R ceramic capacitors (0201) TDK C0603X5R0J104M
C141	1	100µF ±20%, 6.3V X5R ceramic capacitor (1210) TDK C3225X5R0J107M
D1	1	Dual Schottky diode (SOT23) Central Semi CMPD6263S or Diodes Inc. BAS70-04
D2, D3	2	Green surface-mount LEDs (0603)
IN0–IN7, CLOCK	9	SMA PC-mount vertical connectors
J1–J8, JU14	9	2-pin headers
J9–J13, J15	6	Dual-row, 40-pin (2 x 20) headers
J14	1	9-pin header
JU1–JU11, JU13	12	3-pin headers
JU12	1	Dual-row, 8-pin (2 x 4) header
N1	1	Digital logic n-channel MOSFET (SOT23) Central Semi 2N7002
R1–R8, R22–R25, R62–R73	0	Not installed, resistors (0603)
R9–R16, R26–R35, R77–R81, R87–R93, R98	0	Not installed, resistors (0402)
R17–R21, R58–R61	9	49.9Ω ±1% resistors (0603)
R36, R105–R133	30	49.9Ω ±1% resistors (0402)
R37–R44, R74, R75, R76, R82–R86	16	10Ω ±1% resistors (0805)
R45–R50, R100–R103	10	100Ω ±1% resistors (0603)
R51	1	100kΩ potentiometer, 19-turn, 3/8in
R52, R53, R56	3	4.02kΩ ±1% resistors (0603)
R54	1	5kΩ potentiometer, 19-turn, 3/8in
R55	1	2kΩ ±1% resistor (0603)
R57	1	13.0kΩ ±1% resistor (0603)
R94, R95	2	4.7kΩ ±5% resistors (0603)
R96, R97	2	330Ω ±5% resistors (1206)
R99	1	162Ω ±1% resistor (0603)
R104	1	10kΩ ±5% resistor (0603)
SW1	1	Momentary contact switch
T1–T8	8	1:1 800MHz RF transformers Mini-Circuits ADT1-1WT
TP1–TP8, TP13, TP14, TP15	0	Test points, not installed
TP9–TP12	4	PC test points (red)
TP16	1	PC test point (black)
U1	1	See EV kit specific component list
U2	1	Single LVDS line receivers (8 SO) Maxim MAX9111ESA
U3	1	Low-noise, low-distortion op amp (5 SOT23) Maxim MAX4250EUK
U4	1	TinyLogic UHS dual inverter (6 SC70) Fairchild NC7WZ04P6X
U5	1	Virtex II platform FPGA (256 FGBGA) Xilinx XC2V80-5FG256C or Xilinx XC2V80-5FG256I
U6	1	PROM (SO-20) Xilinx XC18V01SO20C
U7–U16	10	LVDS/anything-to-LVPECL translators (8 µMAX®) Maxim MAX9375EUA
None	14	Shunts (JU1–JU14)
None	1	PCB: MAX1434/6/7/8 EVALUATION KIT

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EV Kit Component List

EV KIT PART NUMBER	DESIGNATION	DESCRIPTION
MAX1434EVKIT	U1	MAX1434ECQ+D (100 TQFP-EP 14mm x 14mm x 1mm)
MAX1436EVKIT		MAX1436ECQ+D (100 TQFP-EP 14mm x 14mm x 1mm)
MAX1437EVKIT		MAX1437ECQ+D (100 TQFP-EP 14mm x 14mm x 1mm)
MAX1438EVKIT		MAX1438ECQ+D (100 TQFP-EP 14mm x 14mm x 1mm)

Component Suppliers

SUPPLIER	PHONE	WEBSITE
AVX Corporation	843-946-0238	www.avxcorp.com
Central Semiconductor Corp.	631-435-1110	www.centralsemi.com
Diodes Incorporated	805-446-4800	www.diodes.com
Fairchild Semiconductor Corp.	888-522-5372	www.fairchildsemi..com
Mini-Circuits	718-934-4500	www.minicircuits.com
TDK Corp.	847-803-6100	www.component.tdk.com

Note: *Indicate that you are using the MAX1434, MAX1436, MAX1437, or MAX1438 when contacting these component suppliers.*

Quick Start

Recommended Equipment

- DC power supplies:
  - Clock (CVDD) 3.3V, 100mA
  - Analog (AVDD) 1.8V, 500mA
  - Digital (OVDD) 1.8V, 150mA

  Optional

  - Buffers (VPECL) 3.3V, 400mA
  - Deserializer Core (VD1.5) 1.5V, 200mA
  - Deserializer I/O (VD3.3) 3.3V, 200mA
- Signal generator with low phase noise and low jitter for clock input signal (e.g., HP 8662A, HP 8644B)
- Signal generator for analog signal inputs (e.g., HP 8662A, HP 8644B)
- Logic analyzer or data-acquisition system (e.g., HP 16500C, TLA715)
- Analog bandpass filters (e.g., Allen Avionics, K&L Microwave) for input signal and clock signal
- Digital voltmeter

Procedure

The EV kit is a fully assembled and tested surface-mount board. Follow the steps below to verify board operation. **Do not turn on power supplies or enable signal generators until all connections are completed.**

1) Verify that shunts are installed in the following locations:
   - JU1 (pins 2-3) → single termination
   - JU2 (pins 2-3) → LVDS outputs
   - JU3 (pins 2-3) → normal operation
   - JU4 (pins 2-3) → ADC enabled
   - JU7 (pins 2-3) → two's-complement output
   - JU8 (pins 2-3) → FPGA enabled
   - JU9, JU10, JU11 (pins 2-3) → channels 0–3 output from FPGA
   - JU12 (pins 3-4) → internal reference enabled
   - JU14 (not installed) → disconnect external reference buffer
2) Verify that shunts are installed in the following locations for configuring the specific EV kit:
   a) JU5 (pins 1-2), JU6 (pins 2-3), JU13 (pins 2-3) → 39MHz to 50MHz clock frequency range for the MAX1434 EV kit.

b) JU5 (pins 1-2), JU6 (pins 2-3), JU13 (pins 2-3) → 32.5MHz to 40MHz clock frequency range for the MAX1436 EV kit.

c) JU5, JU6, JU13 (pins 2-3) → 45MHz to 50MHz clock frequency range for the MAX1437 EV kit.

d) JU5, JU6, JU13 (pins 2-3) → 45MHz to 65MHz clock frequency range for the MAX1438 EV kit.

3) Connect the clock signal generator to the input of the clock bandpass filter.

4) Connect the output of the clock bandpass filter to the clock SMA connector.

5) Connect the analog input signal generator to the input of the analog bandpass filter.

6) Connect the output of the analog bandpass filter to either one of the SMA connectors labeled IN0–IN7. The analog input signals can also be monitored at the 2-pin headers J1–J8.

Note: All eight channels can be operated independently or simultaneously.

7) Connect the logic analyzer to either header J9 (SLVS- or LVDS-compatible signals) or J10–J13 (deserialized 3.3V CMOS-compatible signals). See the *Output Bit Locations* section in this document for header connections.

8) Connect the 1.8V, 500mA power supply to AVDD. Connect the ground terminal of this supply to GND.

9) Connect the 1.8V, 150mA power supply to OVDD. Connect the ground terminal of this supply to GND.

10) Connect the 3.3V, 100mA power supply to CVDD. Connect the ground terminal of this supply to GND.

11) Connect the 3.3V, 400mA power supply to VPECL. Connect the ground terminal of this supply to GND.

12) Connect the 1.5V, 200mA power supply to VD1_5. Connect the ground terminal of this supply to GND.

13) Connect the 3.3V, 200mA power supply to VD3_3. Connect the ground terminal of this supply to GND.

14) Turn on the VD3_3 power supply.

15) Turn on the VD1_5 power supply.

16) Verify that the PROGRAMMING LED (D2) and the LOCKED LED (D3) are off.

17) Turn on the remaining power supplies.

18) Enable the signal generators. Set the clock signal generator to output **as specified to configuration** signal, with a $2.6V_{P-P}$ amplitude or higher. Set the analog input signal generators to output the desired frequency with an amplitude $\leq 1.4V_{P-P}$. All signal generators should be phase-locked.

19) Verify that the PROGRAMMING LED (D2) is off.

20) Momentarily press switch SW1 and verify that the LOCKED LED (D3) is on.

21) Enable the logic analyzer.

22) Collect data using the logic analyzer.

_Detailed Description of Hardware

The EV kit is a fully assembled and tested circuit board that contains all the components necessary to evaluate the performance of the MAX1438, MAX1437, MAX1436, or MAX1434.

The ADCs accept differential input signals; however, on-board transformers (T1–T8) convert the single-ended signals applied to the IN0–IN7 SMA connectors, to the required differential signal. The input signals of the ADC can be measured using a differential oscilloscope probe at headers J1–J8.

Output level translators (U7–U16) buffer and convert the SLVS or LVDS output signals of the ADC to higher voltage LVPECL signals, which can be captured by a wide variety of logic analyzers. The SLVS/LVDS output signals are accessible at header J9 and the LVPECL output signals are accessible at header J15.

The EV kit PC board is designed as a six-layer board to optimize performance of the ADC. Separate analog, digital, clock, and buffer power planes minimize noise coupling between analog and digital signals. 50Ω coplanar transmission lines are used for analog and clock inputs. 100Ω differential coplanar transmission lines are used for all digital LVDS outputs. All differential outputs are terminated with 100Ω termination resistors between the true and complementary digital outputs. The trace lengths of the 100Ω differential SLVS/LVDS lines are matched to within a few thousands of an inch to minimize layout-dependent data skew.

Power Supplies

For best performance, the EV kit requires separate analog, digital, clock, and buffer power supplies. Two 1.8V power supplies are used to power the analog (AVDD) and digital (OVDD) portion of the ADC. The clock circuitry (CVDD) is powered by a 3.3V power supply. A separate 3.3V power supply (VPECL) is used to power the output buffers (U7–U16) of the EV kit. 1.5V (VD1_5) and 3.3V (VD3_3) power supplies are required to power the deserializer circuit.

Power-Down

Jumper JU4 controls the power-management feature of data converter U1. See Table 1 for jumper JU4 shunt positions.

Table 1. Power-Down Jumper Settings (JU4)

SHUNT POSITION	POWER-DOWN CONNECTIONS	EV KIT FUNCTION
1-2	AVDD	ADC disabled
2-3*	GND	ADC enabled

**Default configuration: JU4 (2-3).*

Clock

By default, the user-provided AC-coupled clock signal applied to the EV kit CLOCK SMA connector is buffered on board with two inverters (U4). In this mode, diode D1 limits the amplitude of the clock signal. Overdriving the clock input can increase the slew rate of the differential signal, thereby reducing clock jitter. The frequency of the signal should not exceed the maximum sampling rate of the ADC. The sinusoidal input signal frequency (f_{CLK}) determines the sampling rate of the ADC. The clock signal applied to the ADC can be observed at test point TP10.

Optional Clock-Shaping Circuit

The EV kit also features an optional on-board clock-shaping circuit that generates a clock signal with variable duty cycle from the AC-coupled sine-wave signal applied to the CLOCK SMA connector. The MAX9111 differential line receiver (U2) processes the clock input signal and generates the required CMOS clock signal. To use this circuitry, cut the trace on the printed circuit (PC) board at R78 and install 0Ω resistors at R35 and R77. The signal's duty cycle can be adjusted with potentiometer R54. With a 3.3V clock supply voltage (CVDD), a clock signal with a 50% duty cycle (recommended) can be achieved by adjusting R54 until a voltage of 1.32V is produced across test points TP12 and TP16.

PLL Frequency Mode Selection

When driving the EV kit with clock signals lower than the maximum specified sampling rate of the ADC, the phased-locked-loop (PLL) circuit of the ADC must be set accordingly. Refer to the PLL Inputs (PLL0–PLL3) section in the ADC data sheet for further details about the operation of the internal PLL. Jumpers JU5, JU6, and JU13 control the PLL mode of the ADC. See Tables 2, 3, 4, or 5 for shunt positions. Configure jumpers JU5, JU6, and JU13 accordingly and ensure that the clock signal frequency falls between the minimum and maximum limits listed in Table 2 through Table 5.

Table 2. MAX1434 PLL Jumper Settings (JU5, JU6, JU13)

SHUNT POSITION	JUMPER			CLOCK INPUT RANGE (MHz)	
	JU13 (PLL1)	JU6 (PLL2)	JU5 (PLL3)	MIN	MAX
	2-3	2-3	2-3	Unused	
	2-3*	2-3*	1-2*	39.0	50.0
	2-3	1-2	2-3	27.0	39.0
	2-3	1-2	1-2	19.5	27.0
	1-2	2-3	2-3	13.5	19.5
	1-2	2-3	1-2	9.8	13.5
	1-2	1-2	2-3	6.8	9.8
	1-2	1-2	1-2	4.8	6.8

**Default configuration: JU5, JU6 (2-3), JU13 (1-2).*

Table 3. MAX1436 PLL Jumper Settings (JU5, JU6, JU13)

SHUNT POSITION	JUMPER			CLOCK INPUT RANGE (MHz)	
	JU13 (PLL1)	JU6 (PLL2)	JU5 (PLL3)	MIN	MAX
	2-3	2-3	2-3	Unused	
	2-3*	2-3*	1-2*	32.5	40.0
	2-3	1-2	2-3	22.5	32.5
	2-3	1-2	1-2	16.3	22.5
	1-2	2-3	2-3	11.3	16.3
	1-2	2-3	1-2	8.1	11.3
	1-2	1-2	2-3	5.6	8.1
	1-2	1-2	1-2	4.0	5.6

**Default configuration: JU5, JU6 (2-3), JU13 (1-2).*

Table 4. MAX1437 PLL Jumper Settings (JU5, JU6, JU13)

SHUNT POSITION	JUMPER			CLOCK INPUT RANGE (MHz)	
	JU13 (PLL1)	JU6 (PLL2)	JU5 (PLL3)	MIN	MAX
	2-3*	2-3*	2-3*	45.0	50.0
	2-3	2-3	1-2	32.5	45.0
	2-3	1-2	2-3	22.5	32.5
	2-3	1-2	1-2	16.3	22.5
	1-2	2-3	2-3	11.3	16.3
	1-2	2-3	1-2	8.1	11.3
	1-2	1-2	2-3	5.6	8.1
	1-2	1-2	1-2	4.0	5.6

**Default configuration: JU5, JU6, JU13 (2-3).*

Table 5. MAX1438 PLL Jumper Settings (JU5, JU6, JU13)

SHUNT POSITION	JUMPER			CLOCK INPUT RANGE (MHz)	
	JU13 (PLL1)	JU6 (PLL2)	JU5 (PLL3)	MIN	MAX
	2-3*	2-3*	2-3*	45.0	65.0
	2-3	2-3	1-2	32.5	45.0
	2-3	1-2	2-3	22.5	32.5
	2-3	1-2	1-2	16.3	22.5
	1-2	2-3	2-3	11.3	16.3
	1-2	2-3	1-2	8.1	11.3
	1-2	1-2	2-3	5.6	8.1
	1-2	1-2	1-2	4.0	5.6

**Default configuration: JU5, JU6, JU13 (2-3).*

Input Signal

Although the ADC accepts differential analog input signals, the EV kit only requires a single-ended analog input signal with an amplitude of less than $1.4V_{P-P}$ provided by the user. On-board transformers (T1–T8) convert the single-ended analog input signal and generate differential analog signals at the ADCs' differential input pins. Connect the single-ended analog input signals to SMA connectors IN0–IN7 for channel 0 to channel 7, respectively.

Reference Voltage

The EV kit can be configured to use the ADC's 1.24V internal reference, or a stable, low-noise, external reference. Use the 2 x 4 header JU12 to configure the desired reference mode. See Table 6 for the appropriate shunt settings.

Table 6. Reference Jumper Settings (JU12)

SHUNT POSITION	REFADJ PIN CONNECTION	EV KIT FUNCTION
1-2	Connected to AVDD	Internal reference disabled. Apply an external reference voltage at the REFIO pad. Verify that a shunt is installed on jumper JU14.
3-4*	Connected to GND	Internal reference enabled. Verify that a shunt is not installed on jumper JU14.
5-6**	Connected to REFIO through R57 and R51	Increase full-scale range by adjusting potentiometer R51.
7-8**	Connected to GND through R57 and R51	Compensate for gain errors by adjusting potentiometer R51.

**Default configuration: JU12 (3-4).*
***Refer to the Full-Scale Range Adjustments using the Internal Reference section in the MAX1434, MAX1436, MAX1437, or MAX1438 IC data sheet.*

Output Signal

The ADC features eight serial LVDS-compatible digital outputs. Each output transmits the converted analog input signals of channels 0 through 7. Two additional outputs (CLKOUT and FRAME) are provided for data synchronization. Refer to the MAX1434, MAX1436, MAX1437, or MAX1438 data sheet for more details.

Output Format

The digital output coding can be chosen to be two's complement or straight offset binary by configuring jumper JU7. See Table 7 for the appropriate jumper configuration.

Table 7. Output Format Jumper Settings (JU7)

SHUNT POSITION	$\overline{T}$/B PIN CONNECTION	DESCRIPTION
1-2	AVDD	**Straight Offset Binary Selected.** Digital output in straight offset binary format.
2-3*	GND	**Two's Complement Selected.** Digital output in two's-complement format.

**Default configuration: JU7 (2-3).*

Double-Termination Settings

The ADC features trimmed, internal 100Ω termination resistors between the positive (true) and negative (complementary) line of each output (D0–D7, CLKOUT, and FRAME). The EV kit circuit also features 100Ω termination resistors located at the far end of each differential output pair. Activating the internal termination helps eliminate unwanted reflections on the signal traces. Use jumper JU1 to activate either single or double-termination. See Table 8 for appropriate shunt positions that select the termination architecture.

Table 8. Double-Termination Jumper Settings (JU1)

SHUNT POSITION	DT PIN CONNECTION	EV KIT FUNCTION
1-2	AVDD	**Double Termination Selected.** Outputs are double-terminated.
2-3*	GND	**Single Termination Selected.** Outputs are single-terminated.

**Default configuration: JU1 (2-3).*

SLVS/LVDS Outputs

The ADC is capable of generating SLVS or LVDS signals at its outputs. Jumper JU2 controls this feature of the ADC. See Table 9 for shunt positions. Regardless of which output signal type is selected, the output buffers (U7–U16) will convert the data to LVPECL logic levels. When operating in SLVS output mode, JU1 must be configured for double-termination (shunt across pins 1 and 2).

Table 9. SLVS/$\overline{\text{LVDS}}$ Jumper Settings (JU7)

SHUNT POSITION	SLVS/$\overline{\text{LVDS}}$ PIN CONNECTION	ADC OUTPUT
1-2	AVDD	SLVS
2-3*	GND	LVDS

**Default configuration: JU7 (2-3).*

LVDS Test Pattern

To debug signal integrity problems, the ADC can generate a factory-set test pattern on all of the output channels. Jumper JU3 controls this feature. See Table 10 for the appropriate shunt positions. The test pattern for the MAX1436, MAX1437, and MAX1438 is 0000 1011 1101. The test pattern for the MAX1434 is 00 0101 1101 (MSB to LSB).

Table 10. LVDS Test Pattern Jumper Settings (JU3)

SHUNT POSITION	LVDSTEST PIN CONNECTION	EV KIT FUNCTION
1-2	AVDD	Test pattern transmitted, LSB first, on all SLVS/LVDS outputs
2-3*	GND	Normal operation

**Default configuration: JU3 (2-3).*

Output Bit Locations

The digital outputs of the ADC are connected to the 40-pin header J9. All PC board trace lengths are matched to minimize data skew and improve the overall dynamic performance of the device. Additionally, 10 drivers (U7–U16) buffer and level-translate the digital outputs to LVPECL-compatible signals. The drivers increase the differential voltage swing, and are capable of driving large capacitive loads, which may be present at the logic analyzer connection. The outputs of the buffers are connected with 40-pin header J15. See Table 11 for bit locations of headers J9 and J15.

Table 11. Output Bit Locations

SIGNAL		UNBUFFERED (LVDS or SLVS)	BUFFERED (LVPECL)	DESCRIPTION
CH0	P	J9-1	J15-1	Channel 0
	N	J9-2	J15-2	
CH1	P	J9-5	J15-5	Channel 1
	N	J9-6	J15-6	
CH2	P	J9-9	J15-9	Channel 2
	N	J9-10	J15-10	
CH3	P	J9-13	J15-13	Channel 3
	N	J9-14	J15-14	
CLKOUT	P	J9-17	J15-17	Clock
	N	J9-18	J15-18	
FRAME	P	J9-21	J15-21	Frame
	N	J9-22	J15-22	
CH4	P	J9-25	J15-25	Channel 4
	N	J9-26	J15-26	
CH5	P	J9-29	J15-29	Channel 5
	N	J9-30	J15-30	
CH6	P	J9-33	J15-33	Channel 6
	N	J9-34	J15-34	
CH7	P	J9-37	J15-37	Channel 7
	N	J9-38	J15-38	

P = True (+).
N = Complementary (-).

On-Board Deserializer

The EV kit features an on-board deserializer that converts the serial outputs of the ADC to a parallel data stream. The deserializer uses a delay-locked loop (DLL) to synchronize itself with the incoming serial data stream. **After every change in ADC clock frequency, reset this DLL by pressing switch SW1.** If the LOCKED LED D3 is not lit, the serial data stream is not synchronized and the outputs of the deserializer are not valid.

Channel 0 through channel 7 data is captured on headers J10–J13. Only four channels can be captured at one time on the EV kit. Configure jumpers JU9, JU10, and JU11 to select the location of the channels. See Table 12 for jumper JU9, JU10, JU11 configuration. See Table 13 for bit locations.

Table 12. Output Channel Locations (JU9, JU10, JU11)

JU9 (S2) SHUNT POSITION	JU10 (S1) SHUNT POSITION	JU11 (S0) SHUNT POSITION	J10	J11	J12	J13
2-3	2-3	2-3	CH0	CH1	CH2	CH3
2-3	2-3	1-2	CH4	CH5	CH6	CH7
2-3	1-2	2-3	CH0	CH4	CH1	CH5
2-3	1-2	1-2	CH0	CH6	CH1	CH7
1-2	2-3	2-3	CH2	CH4	CH3	CH5
1-2	2-3	1-2	CH2	CH6	CH3	CH7

Table 13. Output Bit Locations (J10–J13)

BIT	POSITION			
CLK	J10-38	J11-38	J12-38	J13-38
D11	J10-26	J11-26	J12-26	J13-26
D10	J10-24	J11-24	J12-24	J13-24
D9	J10-22	J11-22	J12-22	J13-22
D8	J10-20	J11-20	J12-20	J13-20
D7	J10-18	J11-18	J12-18	J13-18
D6	J10-16	J11-16	J12-16	J13-16
D5	J10-14	J11-14	J12-14	J13-14
D4	J10-12	J11-12	J12-12	J13-12
D3	J10-10	J11-10	J12-10	J13-10
D2	J10-8	J11-8	J12-8	J13-8
D1	J10-6	J11-6	J12-6	J13-6
D0	J10-4	J11-4	J12-4	J13-4

Note: *Odd numbered pins are connected to ground. Remaining pins are no connects.*

Deserializer Output Enabled

Jumper JU8 controls the output enabled of the deserializer. See Table 14 for jumper JU8 configuration.

Table 14. Deserializer Output Enables (JU8)

SHUNT POSITION	EV KIT FUNCTION
1-2	Deserializer output disabled
2-3*	Deserializer output enabled

**Default configuration: JU8 (2-3).*

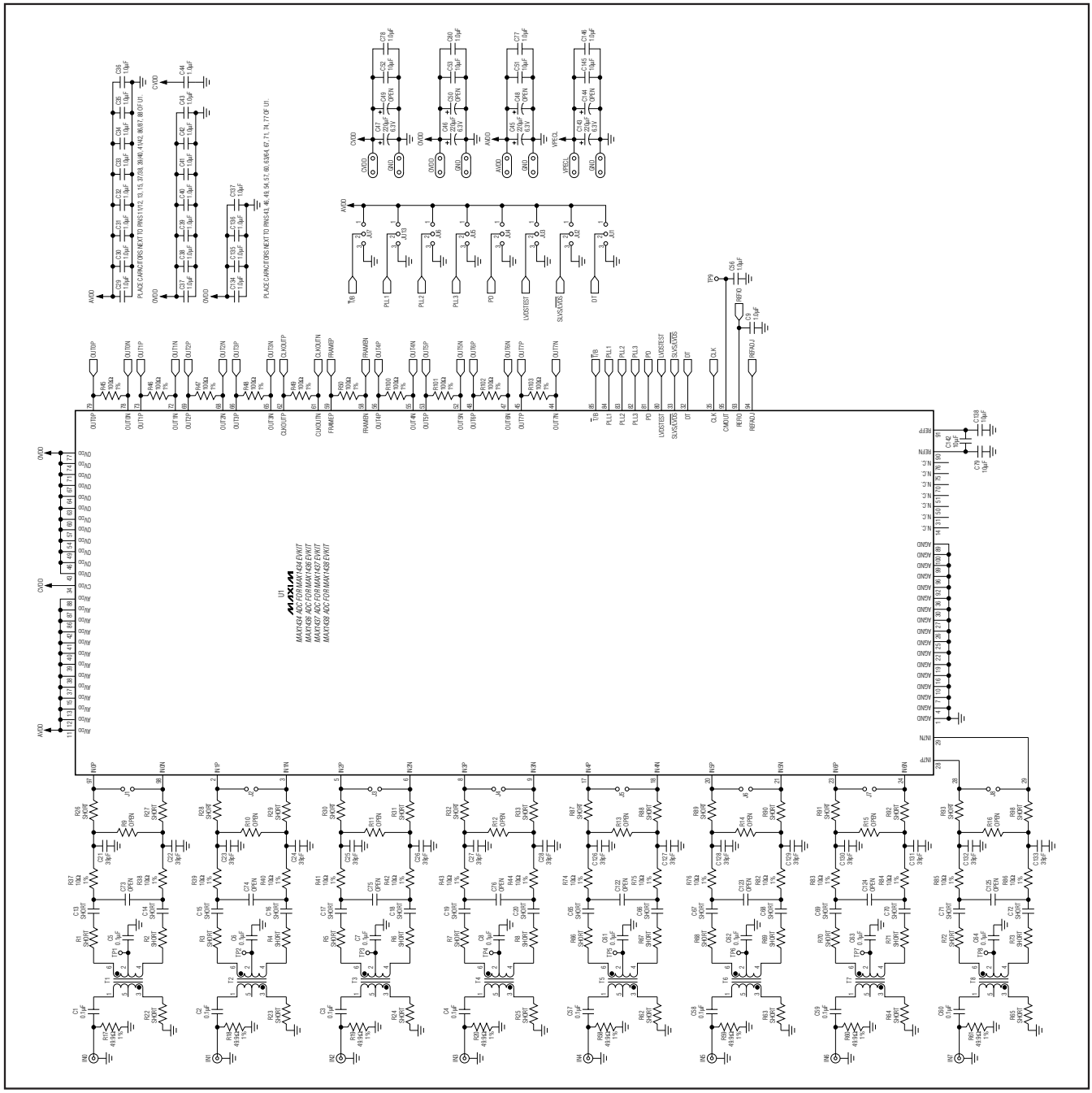

Figure 1. MAX1434/MAX1436/MAX1437/MAX1438 EV Kit Schematic—ADC (Sheet 1 of 6)

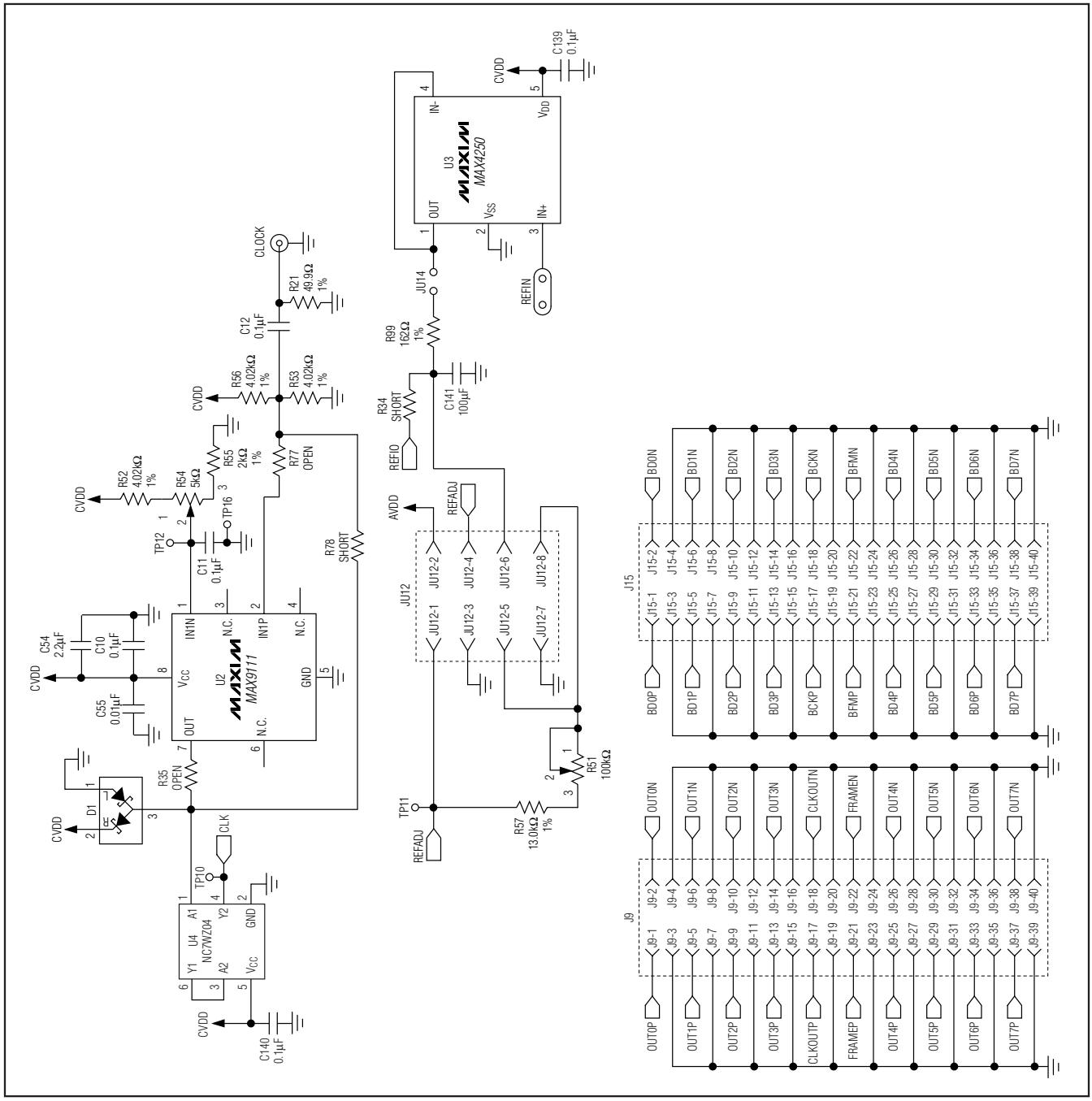

Figure 2. MAX1434/MAX1436/MAX1437/MAX1438 EV Kit Schematic—Clock, Voltage Reference (Sheet 2 of 6)

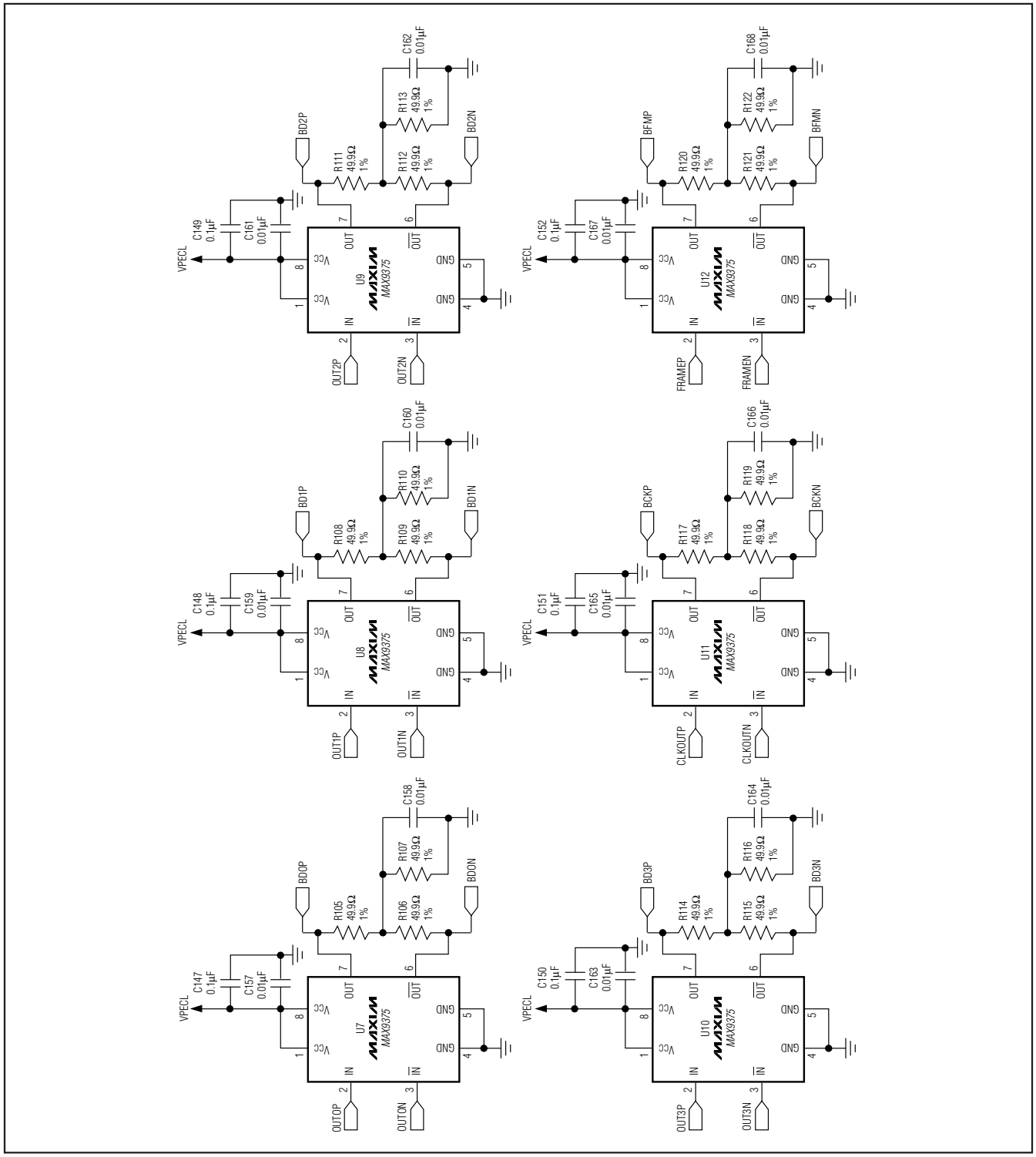

Figure 3. MAX1434/MAX1436/MAX1437/MAX1438 EV Kit Schematic—LVPECL Level Translators (Sheet 3 of 6)

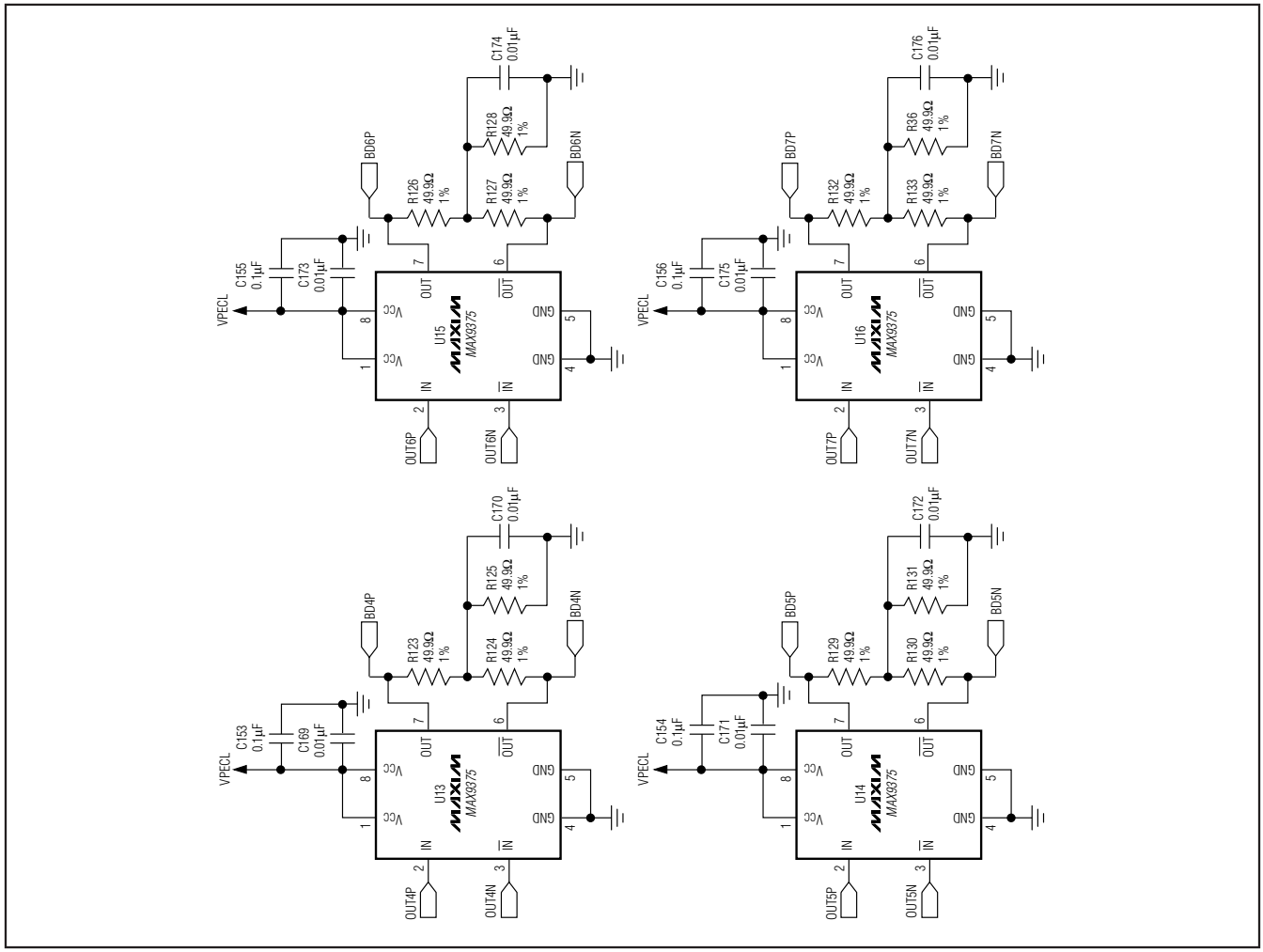

Figure 4. MAX1434/MAX1436/MAX1437/MAX1438 EV Kit Schematic—LVPECL Level Translators (Sheet 4 of 6)

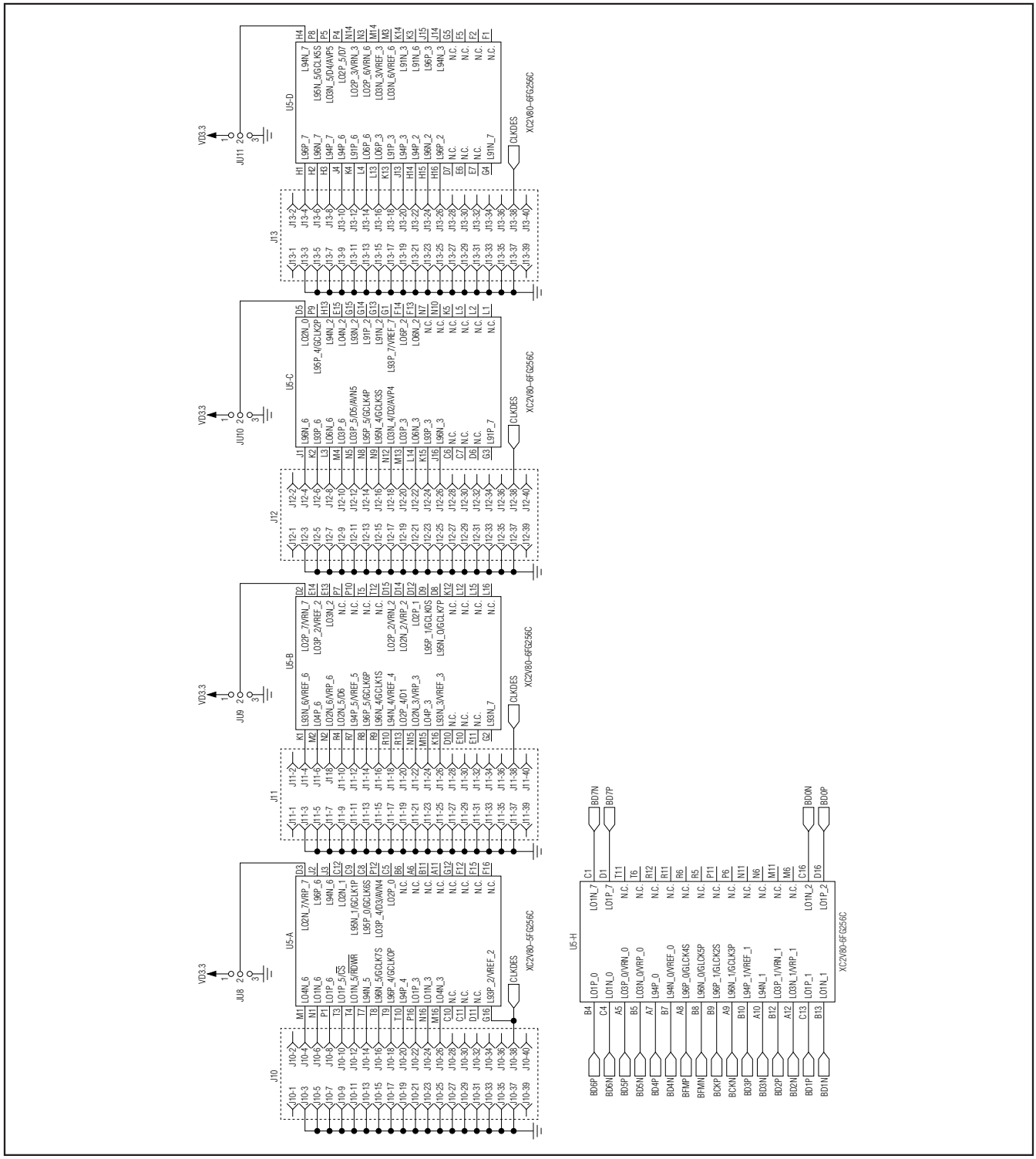

Figure 5. MAX1434/MAX1436/MAX1437/MAX1438 EV Kit Schematic—Deserializer Input and Outputs (Sheet 5 of 6)

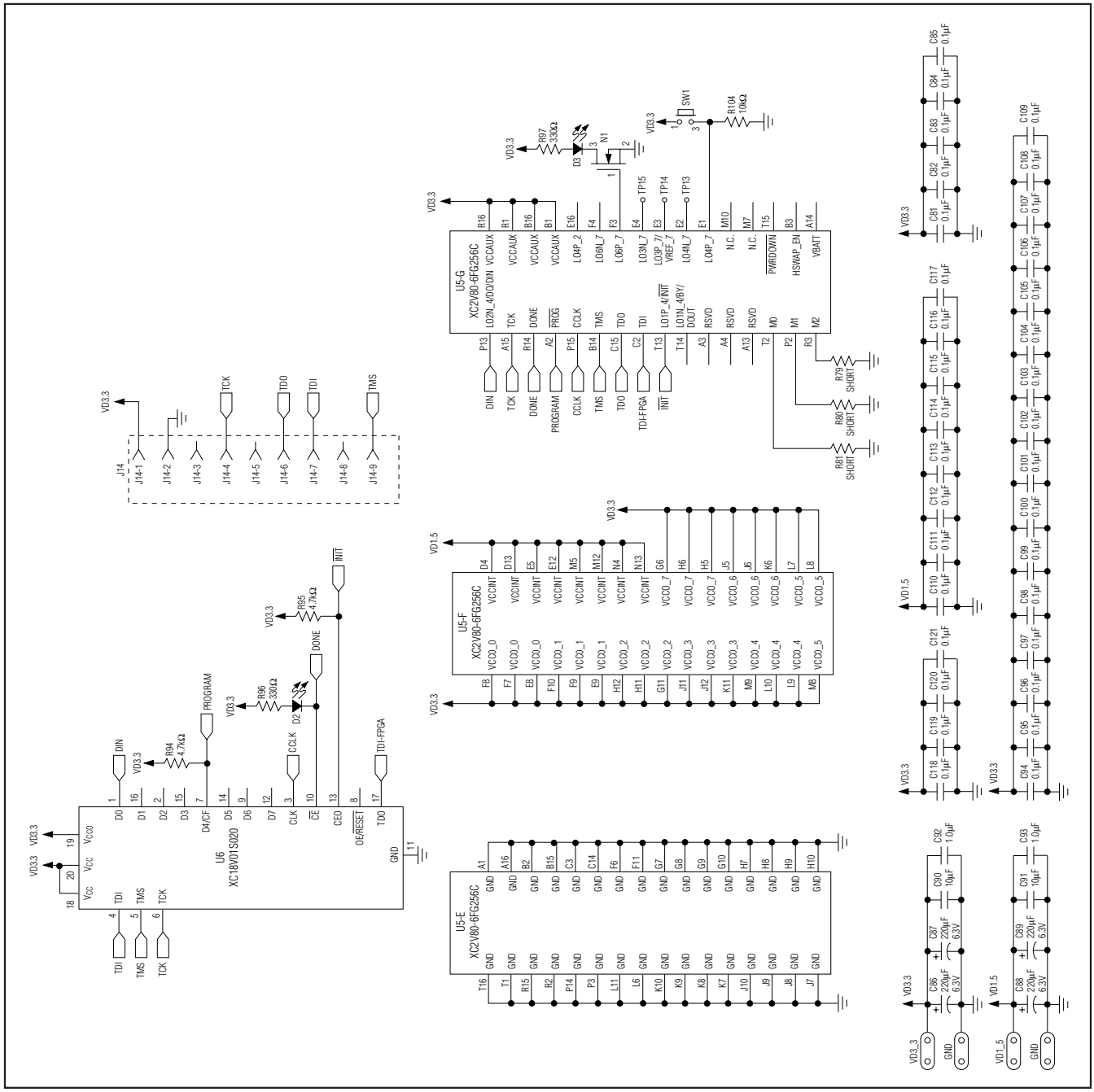

Figure 6. MAX1434/MAX1436/MAX1437/MAX1438 EV Kit Schematic—PROM and FPGA (Sheet 6 of 6)

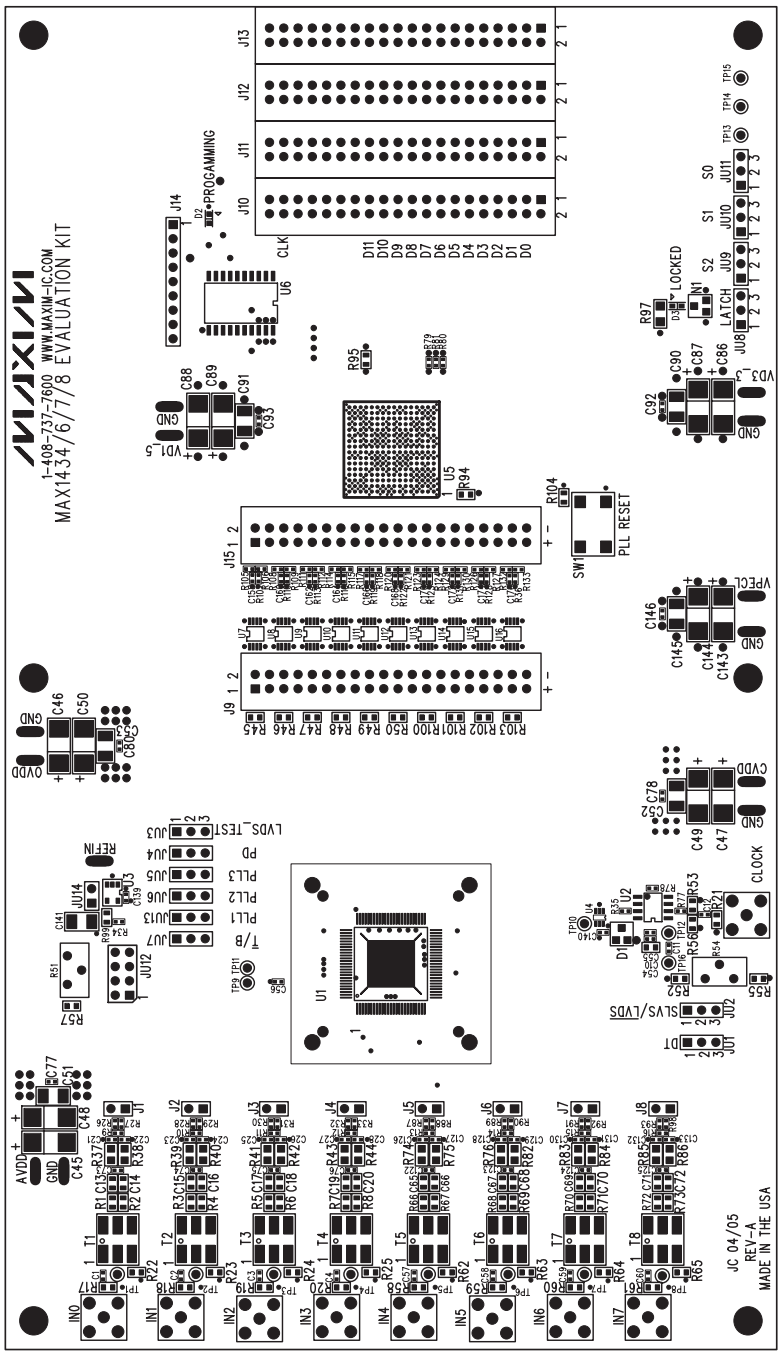

Figure 7. MAX1434/MAX1436/MAX1437/MAX1438 EV Kit Component Placement Guide—Component Side

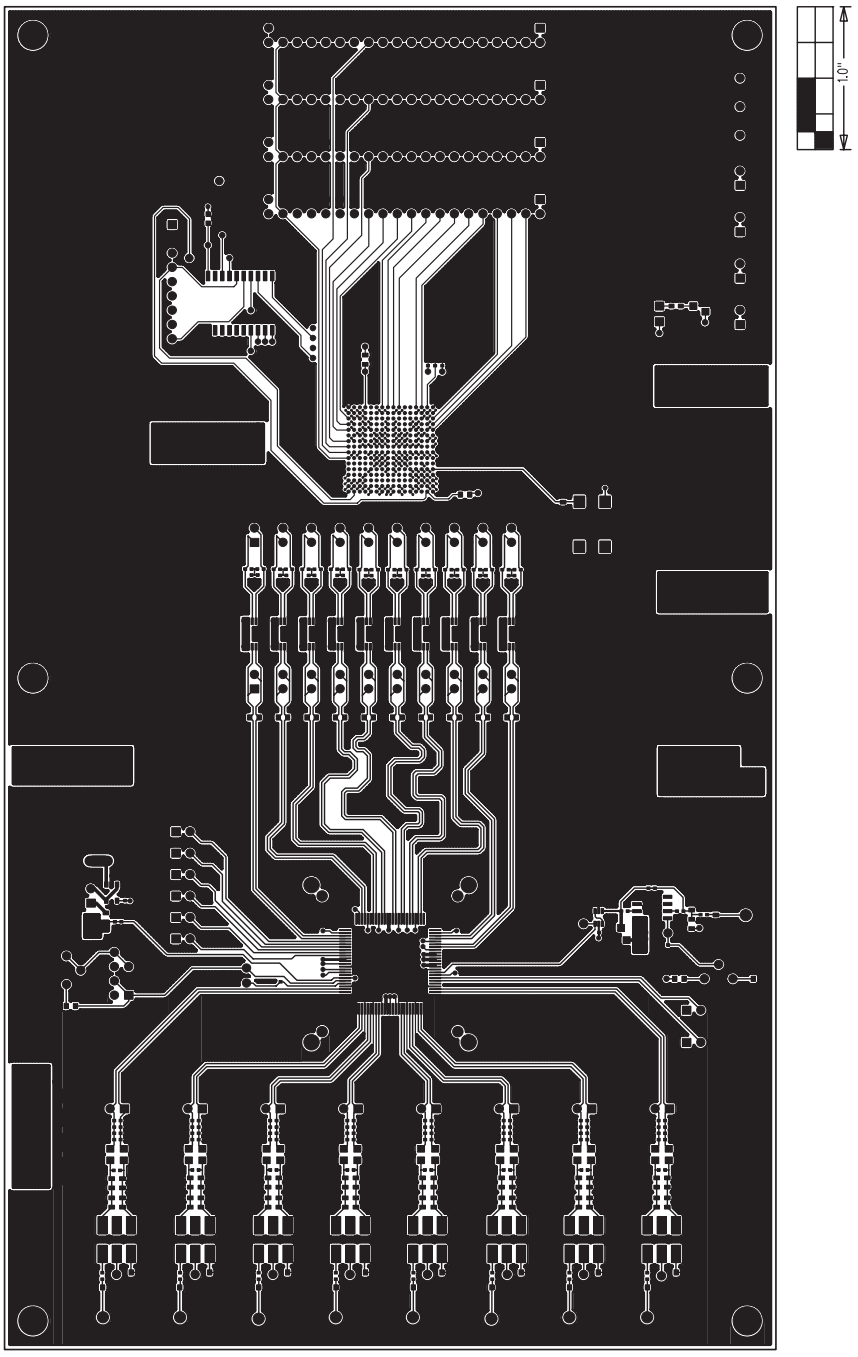

Figure 8. MAX1434/MAX1436/MAX1437/MAX1438 EV Kit PC Board Layout—Component Side

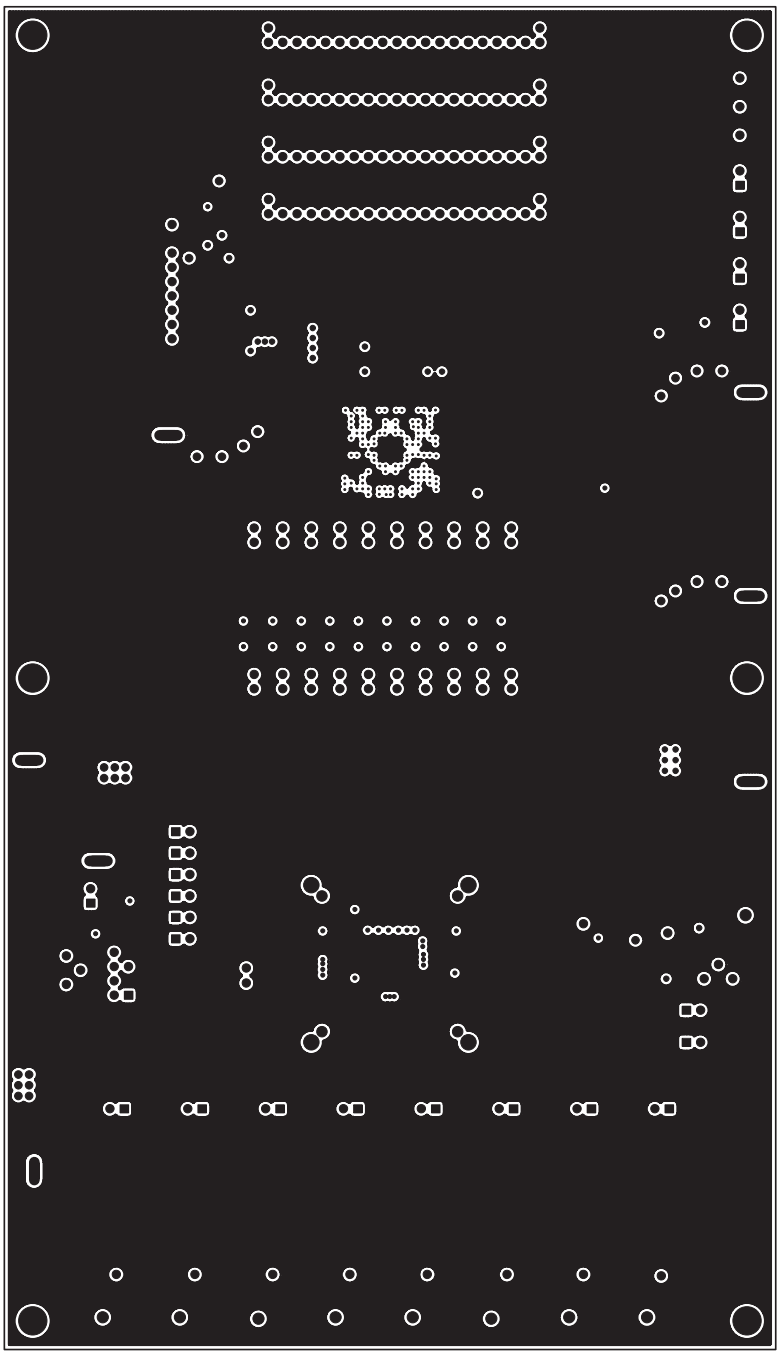

Figure 9. MAX1434/MAX1436/MAX1437/MAX1438 EV Kit PC Board Layout (Inner Layer 2)—Ground Planes

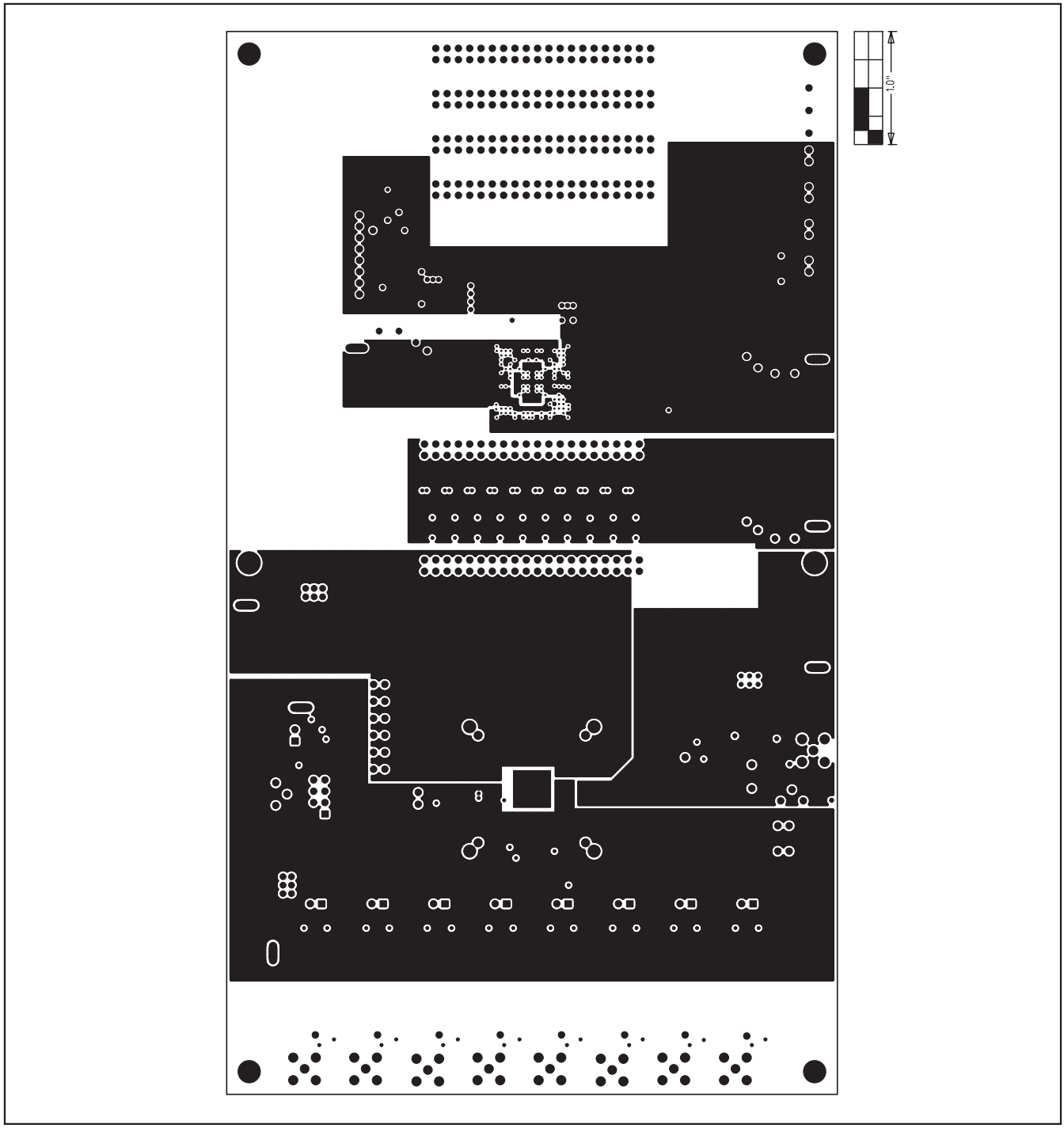

Figure 10. MAX1434/MAX1436/MAX1437/MAX1438 EV Kit PC Board Layout (Inner Layer 3)—Power Planes

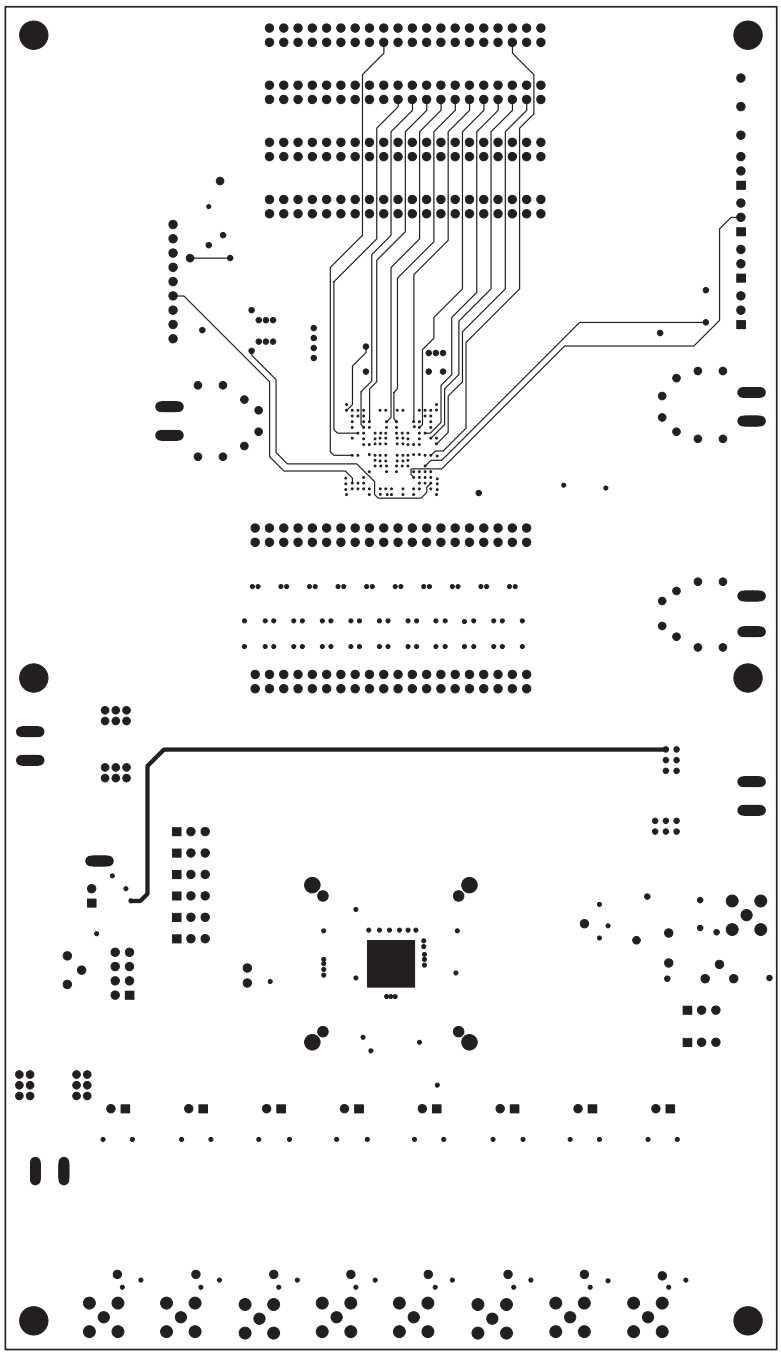

Figure 11. MAX1434/MAX1436/MAX1437/MAX1438 EV Kit PC Board Layout (Inner Layer 4)—Signal Layer

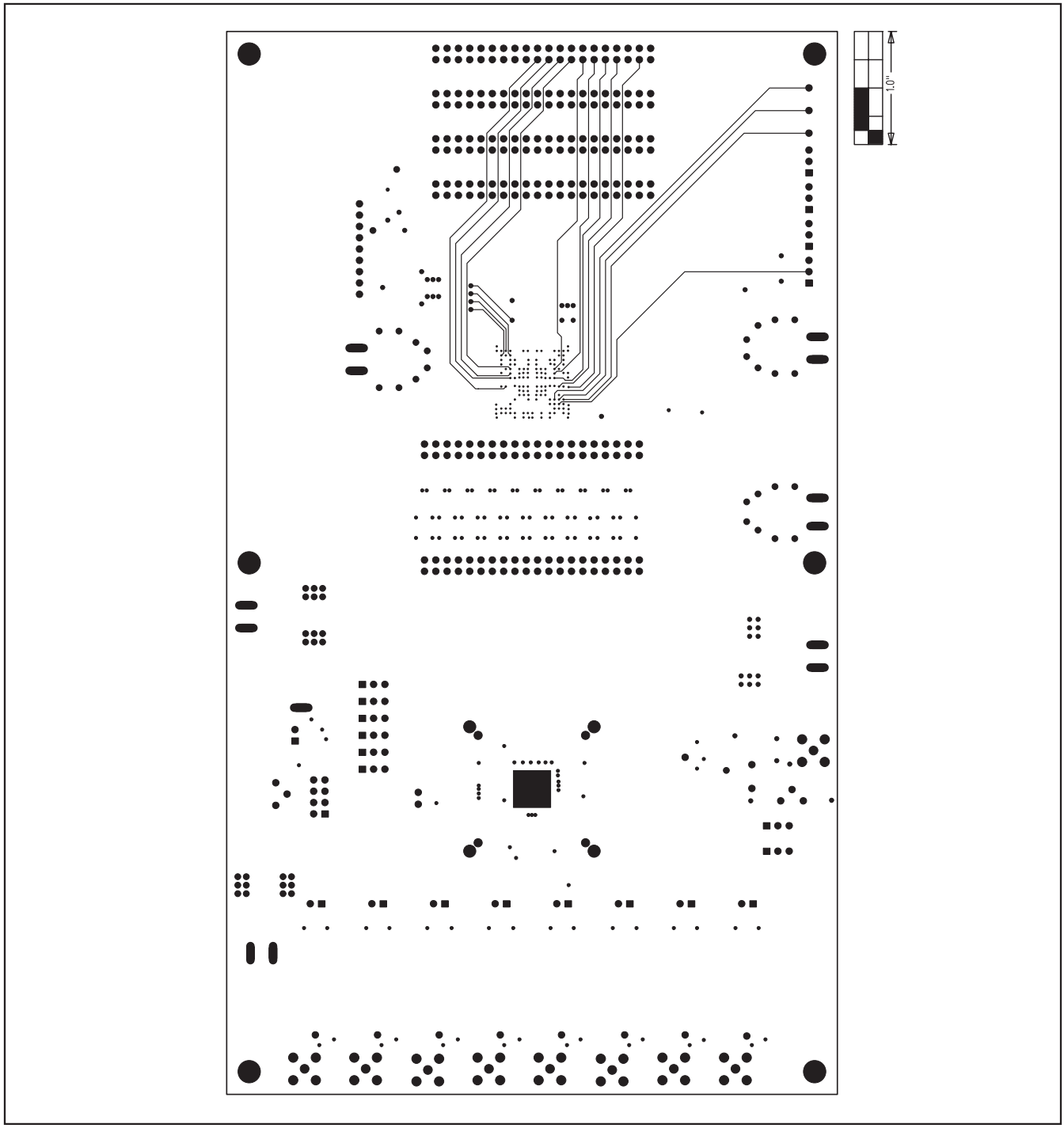

Figure 12. MAX1434/MAX1436/MAX1437/MAX1438 EV Kit PC Board Layout (Inner Layer 5)—Signal Layer

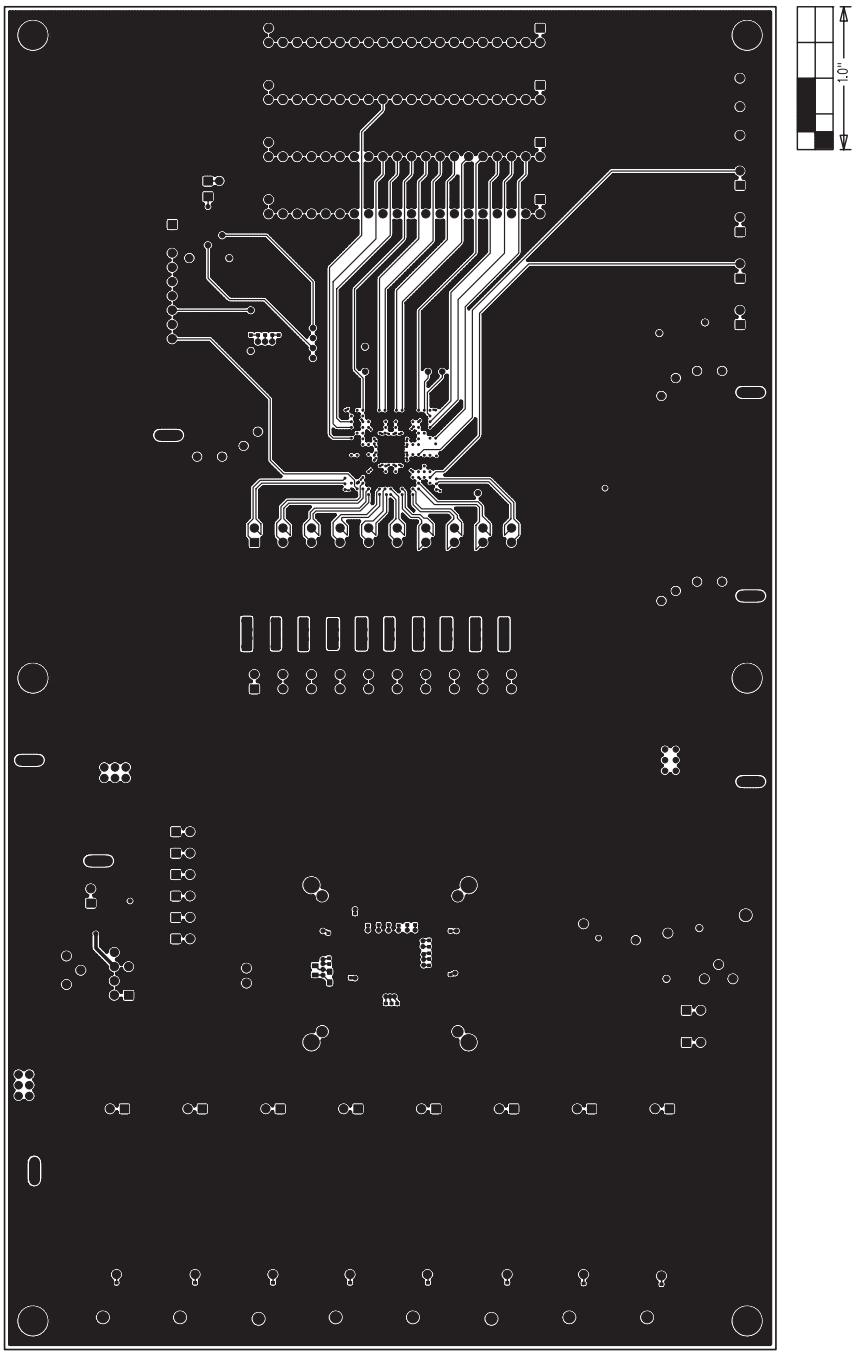

Figure 13. MAX1434/MAX1436/MAX1437/MAX1438 EV Kit PC Board Layout—Solder Side

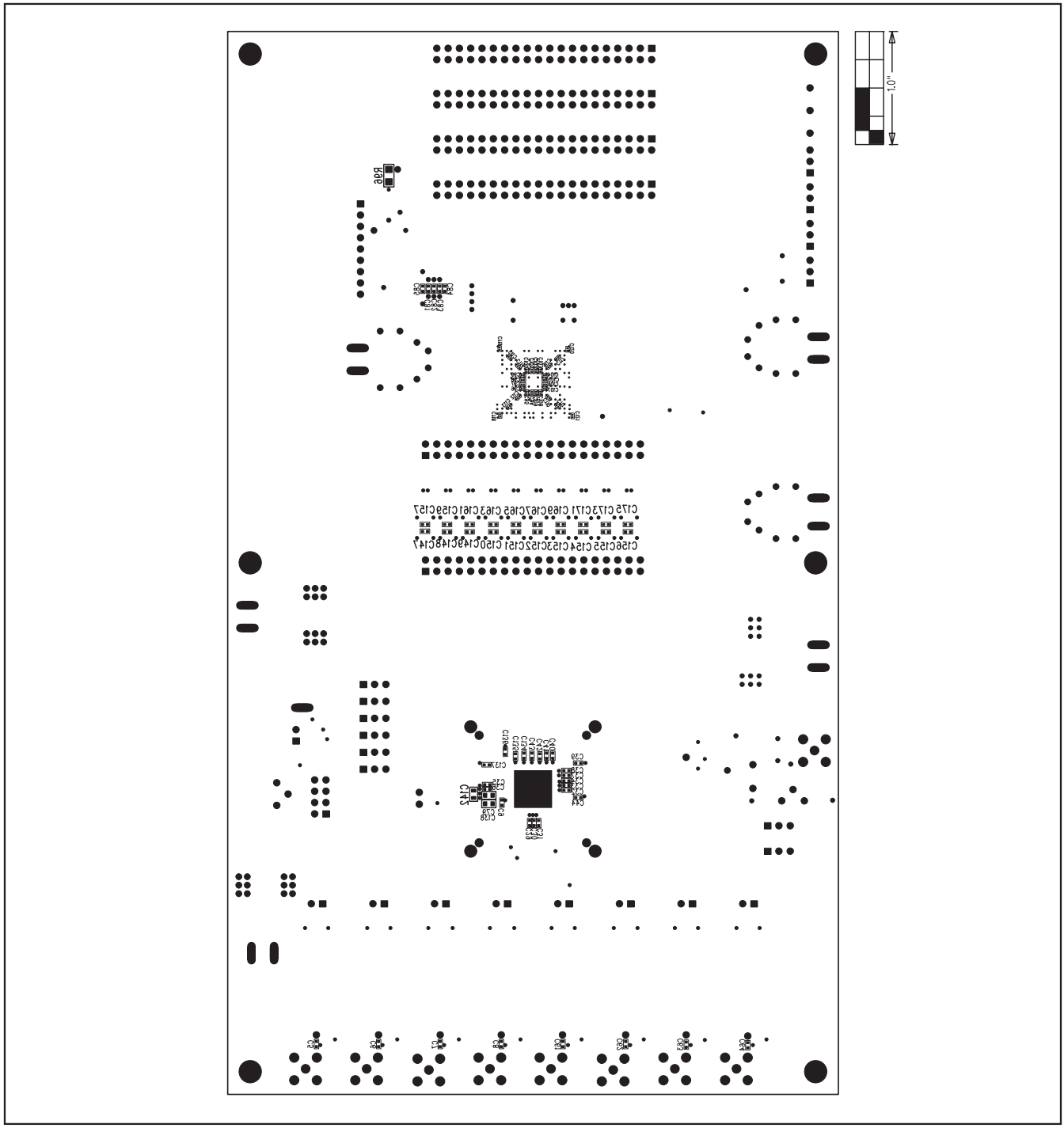

Figure 14. MAX1434/MAX1436/MAX1437/MAX1438 EV Kit Component Placement Guide—Solder Side

Revision History

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
0	6/05	Initial release	—
1	8/10	Added lead-free parts to *Part Selection Table* and *EV Kit Component List* and updated *Component Suppliers*	1, 3