Document Number: KTPF0100UG
Rev. 5.0 8/2015

KITPF0100EPEVBE Evaluation Board

Featuring the MMPF0100 14-Channel Configurable PMIC

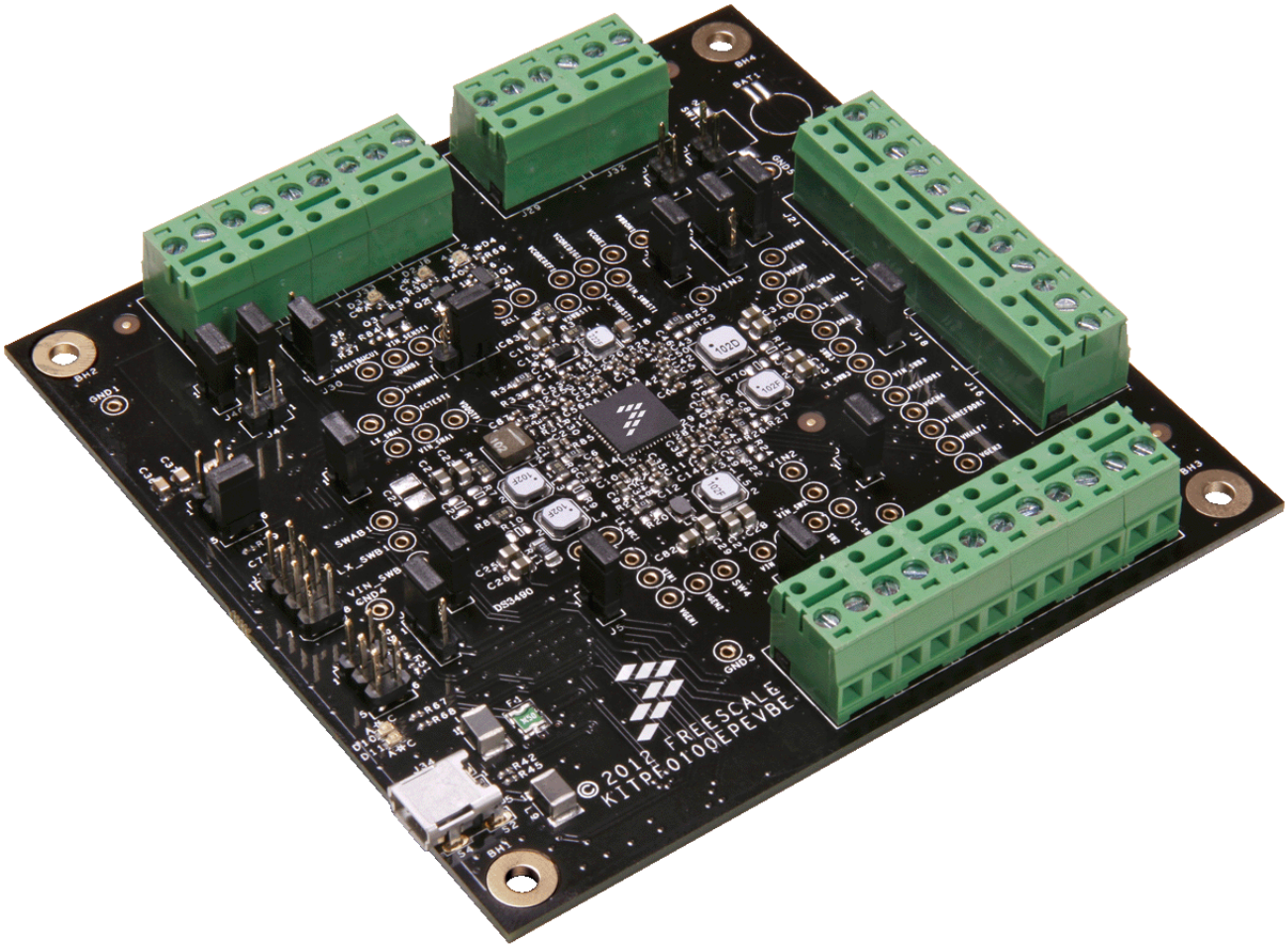

Figure 1. KITPF0100EPEVBE Evaluation Board

Contents

1 Important Notice

Freescale provides the enclosed product(s) under the following conditions:

This evaluation kit is intended for use of ENGINEERING DEVELOPMENT OR EVALUATION PURPOSES ONLY. It is provided as a sample IC pre-soldered to a printed circuit board to make it easier to access inputs, outputs, and supply terminals. This evaluation kit may be used with any development system or other source of I/O signals by simply connecting it to the host MCU or computer board via off-the-shelf cables. Final device in an application will be heavily dependent on proper printed circuit board layout and heat sinking design as well as attention to supply filtering, transient suppression, and I/O signal quality.

The goods provided may not be complete in terms of required design, marketing, and or manufacturing related protective considerations, including product safety measures typically found in the end product incorporating the goods. Due to the open construction of the product, it is the user's responsibility to take any and all appropriate precautions with regard to electrostatic discharge. In order to minimize risks associated with the customers applications, adequate design and operating safeguards must be provided by the customer to minimize inherent or procedural hazards. For any safety concerns, contact Freescale sales and technical support services.

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2 Getting Started

2.1 Kit Contents/Packing List

- Customer evaluation board KITPF0100EPEVBE
- Warranty card and technical support brochure

3 Introduction

The KITPF0100EPEVBE evaluation board supports the development and testing of the PF0100 PMIC, a member of Freescale's i.MX6 family of application processors. The board provides access to all output voltage rails as well as control and signal pins through terminal block connectors. A single terminal block connector for the input power supply allows the user to supply the board with an external DC power supply to fully evaluate the performance of the device.

The KITPF0100EPEVBE comes with a non-programmed version of the PF0100 PMIC that is prepared to power up from the default sequence. However, an integrated control/fuse programming interface allows the customer to program the OTP/TBB (One Time Programmable/Try-Before-Buy) memory and also to select it as the default source for the power-up configuration. Likewise, the programming interface allows full control of the PF0100 through the I^2C communication lines.

This document is intended to provide an overview of the KITPF0100EPEVBE evaluation board as well as detailed instruction for programming the PF0100 through its dedicated Graphic User Interface (GUI).

4 KITPF0100EPEVBE Features

- Input voltage operation range from 3.1 V to 4.5 V
- Output voltage supplies accessible through detachable terminal blocks
  - Four to six independent buck converters
  - One 5.0 V boost regulator
  - Six general purpose LDO regulators
  - One DDR memory termination voltage reference
  - One VSRTC supply
- Coin cell support for "Try-Before-Buy" (TBB) mode
- On/off push button support
- Hardware configuration flexibility through various jumper headers and resistors
- Integrated USB to I^2C programming interface for full control/configuration
  - Onboard OTP programming supply and control
  - Onboard PMIC control through the I^2C register map
  - Fully featured programmer through J36 for external device control/programming
- On board connectors for interfacing with future evaluation/debug tools
- Compact form factor (4 x 4 in^2)

5 MMPF0100 Features

The PF0100 Power Management Integrated Circuit (PMIC) provides a highly programmable/ configurable architecture with fully integrated power devices and minimal external components. With up to six buck converters, six linear regulators, RTC supply, and coin-cell charger, the PF0100 can provide power for a complete system, including applications processors, memory, and system peripherals, in a wide range of applications.

- Four to six buck converters, depending on configuration
  - Single/Dual phase/ parallel options
  - DDR termination tracking mode option
- Boost regulator to 5.0 V output
- Six general purpose linear regulators
- Programmable output voltage, sequence, and timing
- OTP (One Time Programmable) memory for device configuration
- Coin cell charger and RTC supply
- DDR termination reference voltage
- Power control logic with processor interface and event detection
- Individually programmable ON, OFF, and Standby modes

Freescale analog ICs are manufactured using the SMARTMOS process, a combinational BiCMOS manufacturing flow which integrates precision analog, power functions, and dense CMOS logic on a single cost-effective die.

5.1 MC9S08JM60 Features

The KITPF0100EPEVBE implements a Freescale MC9S08JM60 low-cost, high-performance 8-bit HCS08 microcontroller to interface via USB to I2C to control the main PMIC.

- 8-bit HCS08 Central Processing Unit (CPU)
  - Up to 24 MHz internal bus (48 MHz HCS08 core) frequency offering 2.7 to 5.5 V across temperature range of -40 to +85 °C
  - Support for up to 32 peripheral interrupt/reset sources
- On-Chip Memory
  - Up to 60 K flash read/program/erase over full operating voltage and temperature
  - Up to 4 K RAM
  - 256 Byte USB RAM

6 Hardware/Software Requirements

6.1 Hardware Requirements

- Power supply:
  - Output voltage range from 3.1 V to 4.5 V
  - Current capability from 3 to 5 A (current requirement is dependent on output loading)
- Supply to board connection cables (capable of withstanding up to 5.0 A current)
- USB (male) to mini USB (male) communication cable.
- USB-enabled computer.

6.2 Software Requirements

- Windows XP or Windows 7 operating system

7 Hardware Configuration

Connect the power supply and the USB communication cables as shown in Figure 2. Voltmeters are optional but it is recommended in order to accurately verify that each one of the output supplies is providing the correct voltage level.

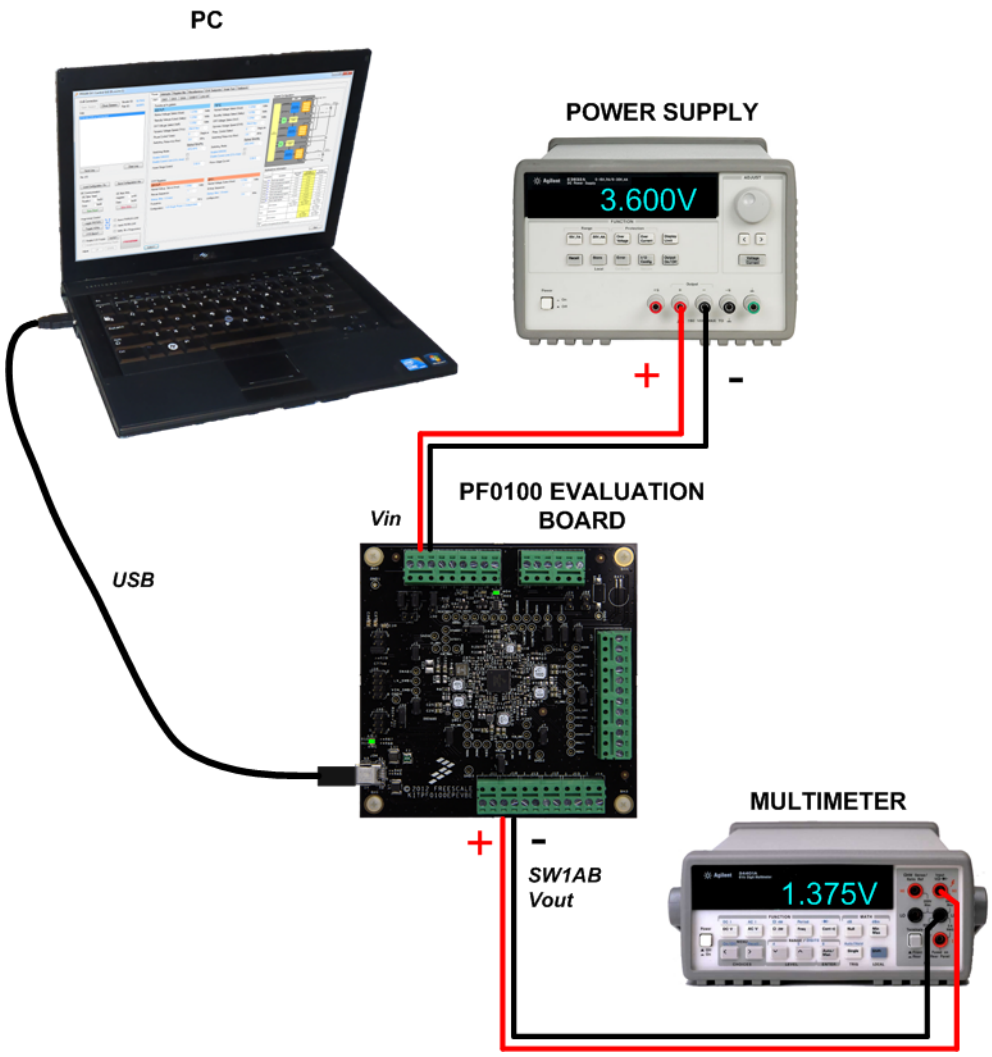


Figure 2. Evaluation Board Setup

Note: The KITPF0100EPEVBE allows the selection of SW2 regulator output or an external 3.3 V LDO output as the VDDIO/I^2C pull-up supply. By default, the SW2 regulator is the source for the VDDIO supply (J46 = 3-4). If the SW2 regulator is to be set below 3.0 V then switch the 3.3 V LDO connection to VDDIO (J46 = 1-2.)

8 Evaluation Board Schematic

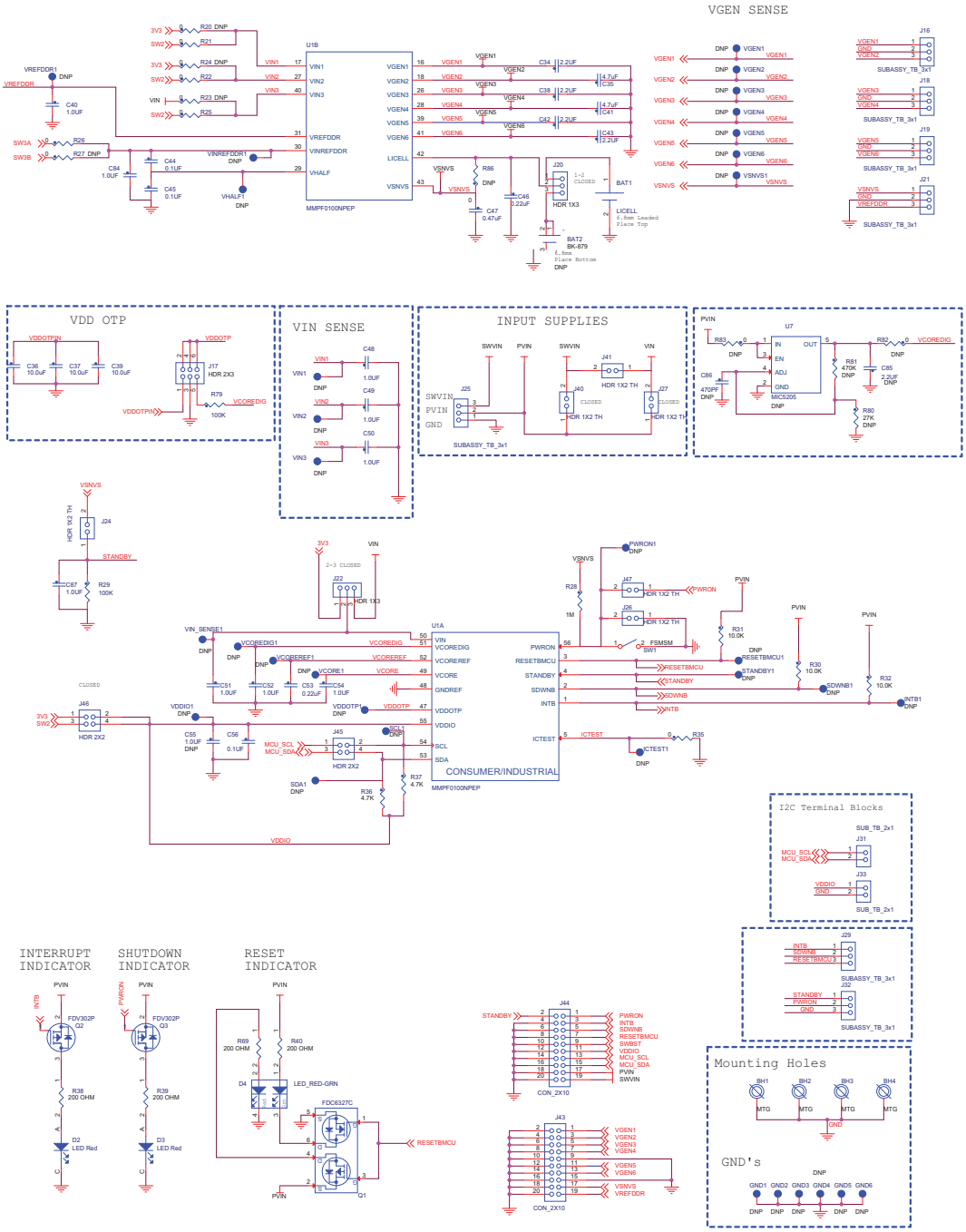


Figure 3. KITPF0100EPEVBE LDO/Control Schematic Part 1

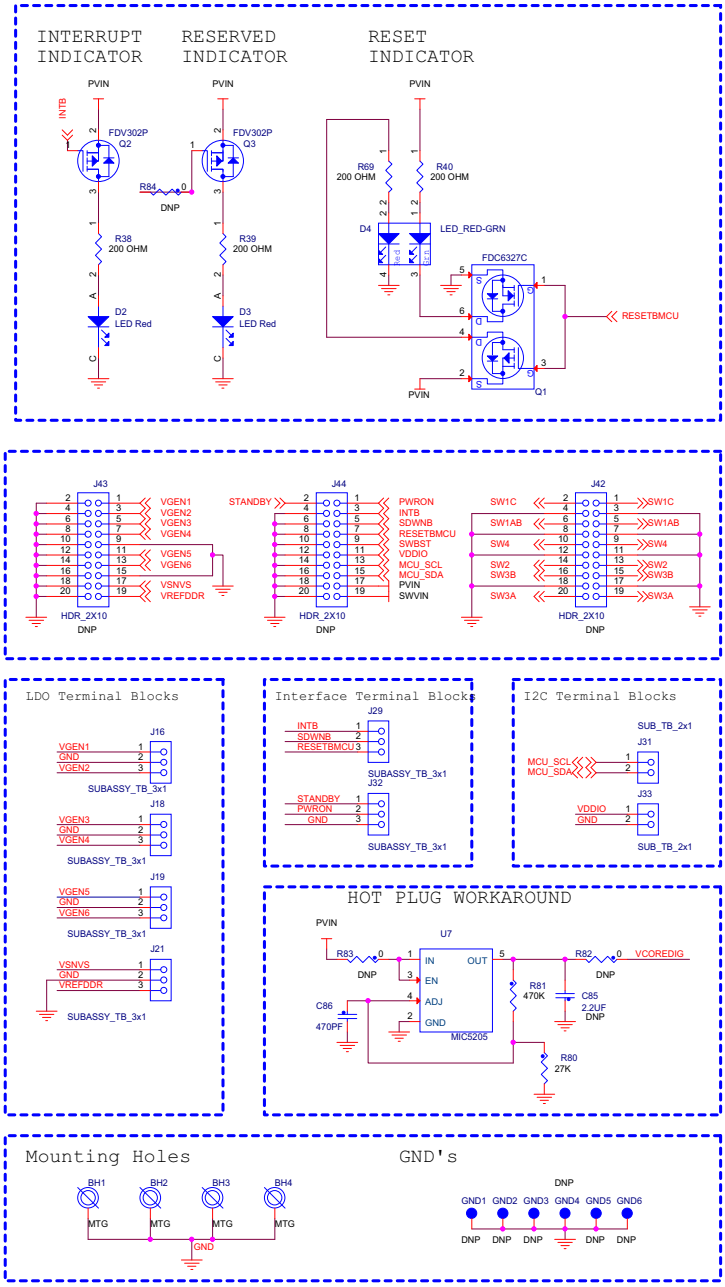


Figure 4. KITPF0100EPEVBE LDO/Control Schematic Part 2

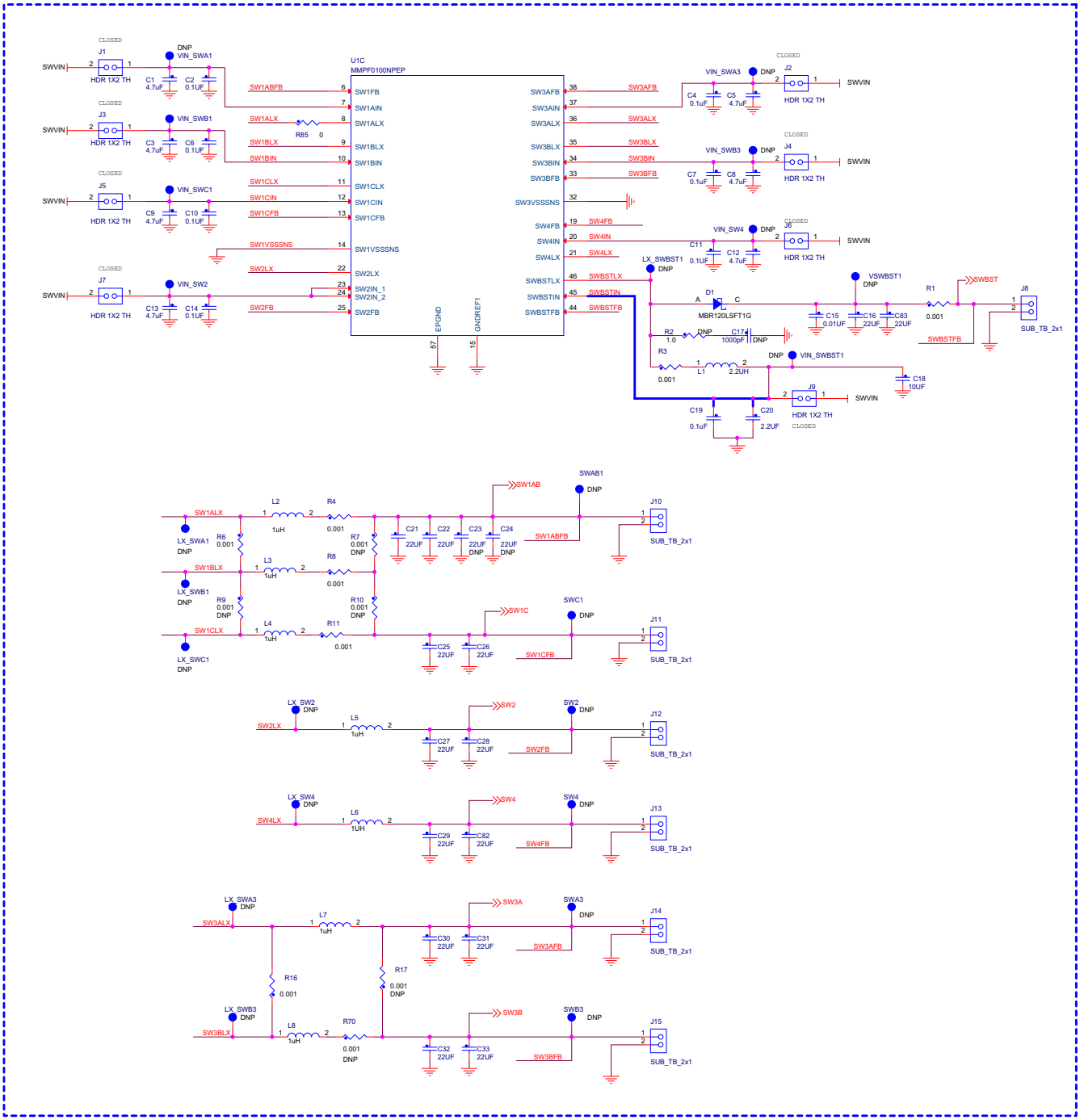


Figure 5. KITPF0100EPEVBE Switching Regulators Schematic

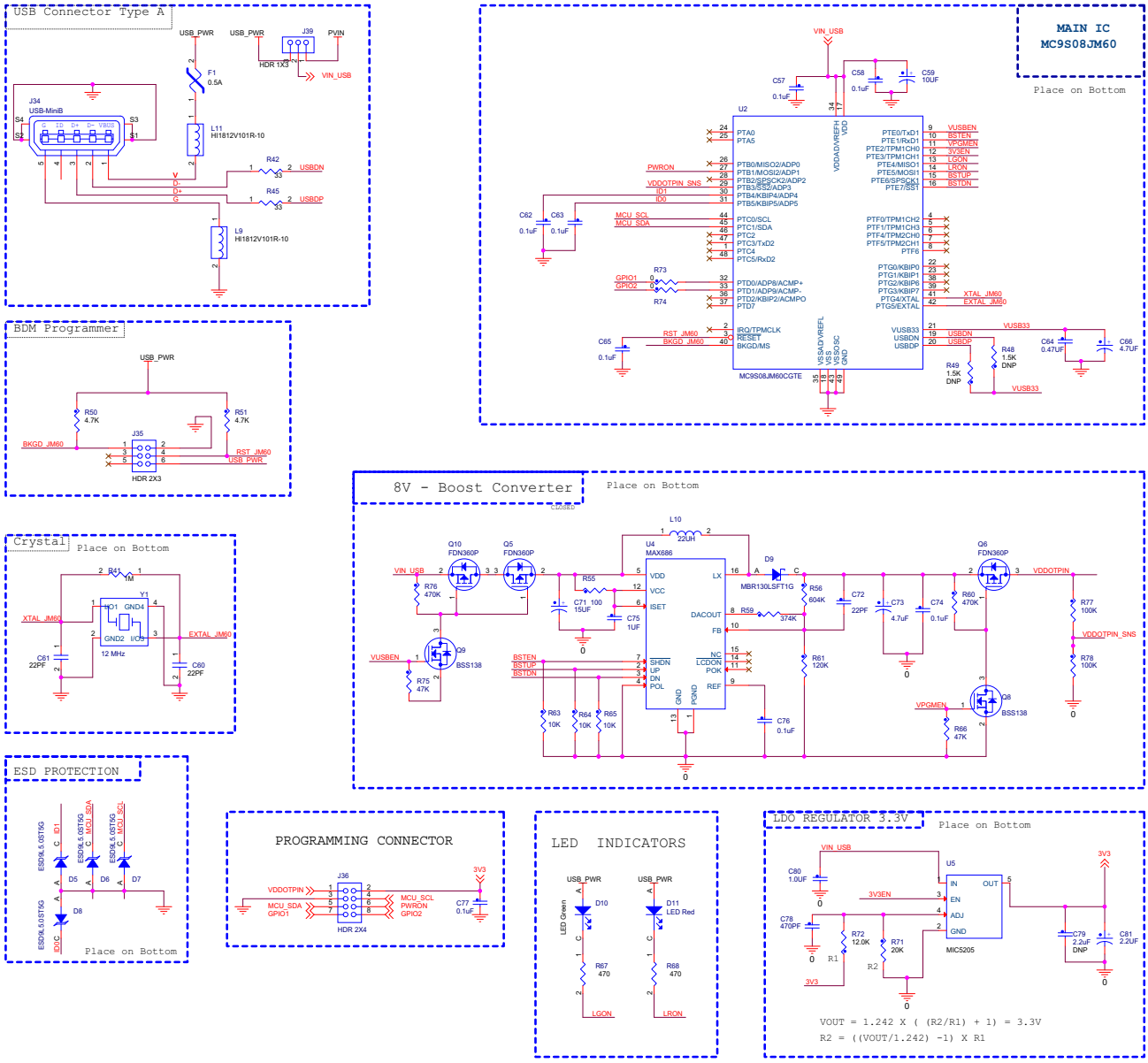


Figure 6. KITPF0100EPEVBE Control/Programming Interface Schematic

9 Hardware Description

The KITPF0100EPEVBE operates with a single power supply from 3.1 V to 4.5 V and is controlled via USB with help of an integrated USB-I^{2}C communication bridge. By applying the input voltage supply, the KITPF0100EPEVBE powers up according to the default power-up sequence described in the MMPF0100 Data Sheet.

Important notice: If power-up sequences and configuration are to be modified, the user must ensure that the register settings are consistent with the hardware configuration. This is most important for the buck regulators, where the quantity, size, and value of the inductors depend on the configuration (single/dual phase or independent mode) and the switching frequency. Additionally, if an LDO is powered by a buck regulator, it is gated by the buck regulator in the start-up sequence. Refer to the MMPF0100 Data Sheet for details on buck regulator setup.

9.1 Jumper Description

By default, the KITPF0100EPEVBE evaluation board is set to power up from the default power-up sequence. Verify that the jumpers are placed in the right position as shown in Figure 7. For a detailed description of the jumper functionality, refer to Table 1.

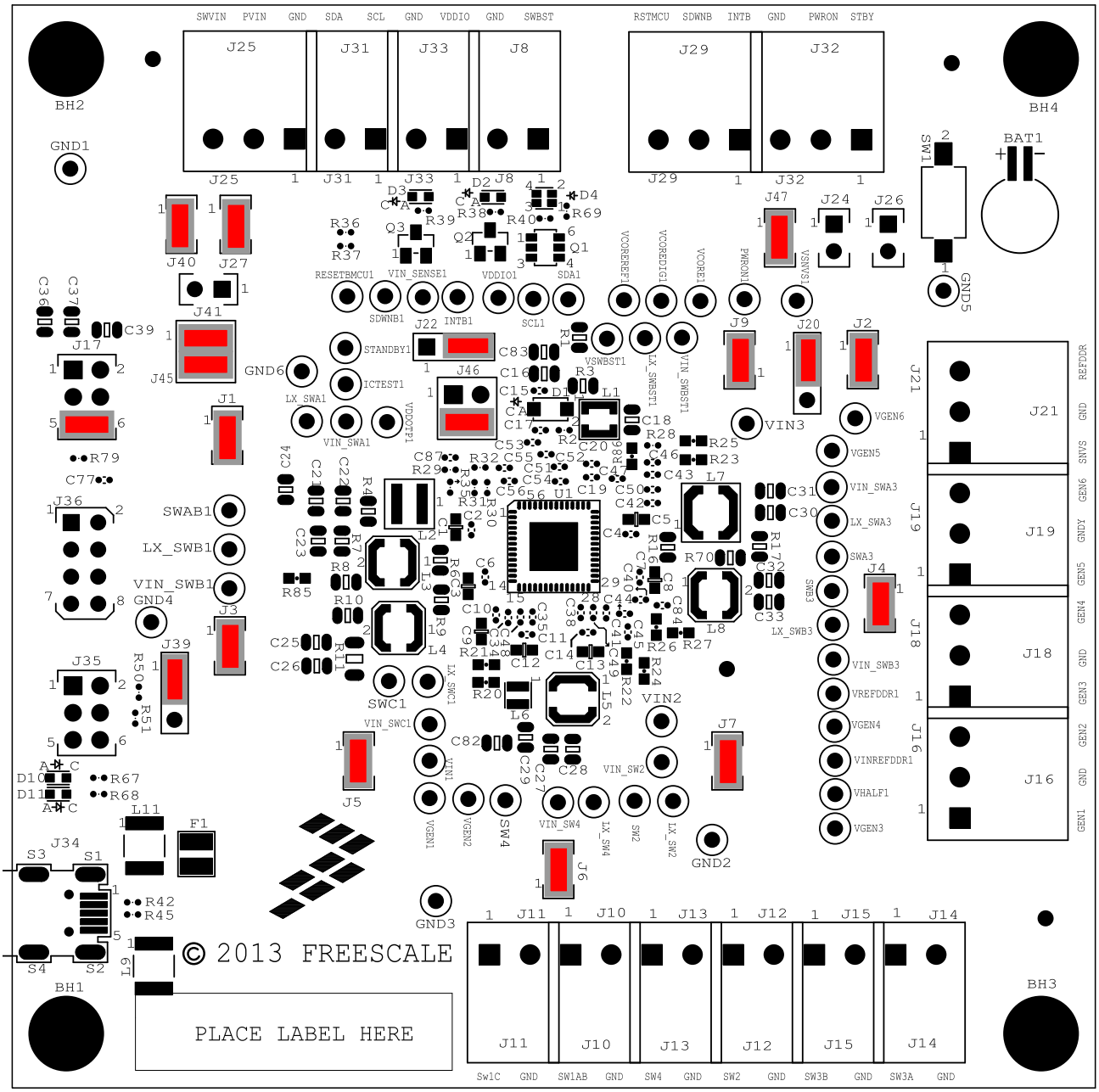


Figure 7. Default Jumper Configuration Diagram

Table 1. KITPF0100EPEVBE Jumper Description

Jumper	Default	Description
J1-J7	Closed	Buck regulators input power path isolation. Short these jumpers to allow SWxIN to be powered from the SWVIN supply.
J9	Closed	SWBST regulator input power path isolation. Short this jumper to allow SWBSTIN to be powered from the SWVIN supply.

Table 1. KITPF0100EPEVBE Jumper Description (continued)

Jumper	Default	Description
J17	5-6	VDDOTP Supply selector • 1-2: Connect VDDOTP to the OTP Boost output (VDDOTPIN) for OTP programming. • 3-4: Connect VDDOTP to GND to power up from OTP/TBB sequence. • 5-6: Connect VDDOTP to VCOREDIG to power up from Default Power up sequence.
J20	1-2	Coin cell selector. • 1-2: Enables BAT1 as the main coin cell supply. • 2-3: Enables BAT2 as the main coin cell supply.
J40	Closed	Shorts PVIN and SWVIN. Allows supply isolation to provide more accurate efficiency readings on the switching supplies.
J41	Open	Shorts SWVIN to VIN. Allows one to isolate or connect the PF0100 logic input supply to SWVIN net. (debugging option)
J27	Closed	Shorts PVIN to VIN. Allows one to isolate or connect the PF0100 logic input supply to PVIN net. (debugging option)
J22	2-3	PF0100 input logic supply selector. • 1-2: Connects PF0100 VIN terminal to the 3.3 V external LDO regulator for debugging purposes. • 2-3: Connects PF0100 VIN terminal to the main input supply. Refer to Figure 3.
J26	Open	Short to hold PWRON pin low.
J24	Open	Short to pull STANDBY to VSNVS voltage supply.
J39	1-2	Control Interface input supply selector • 1-2: Enables PVIN node as the input supply source for the control interface. • 2-3: Enables USB power as the input supply source for the control interface.

9.2 Connectors and Terminal Blocks Description

Table 2. Terminal Blocks descriptions

Connector	Function	Pin definition
J8	SWBST	Pin 1 - SWBST Output Pin 2 - GND
J10	SW1AB	Pin 1 - SW1AB Output Pin 2 - GND
J11	SW1C	Pin 1 - SW1C Output Pin 2 - GND
J12	SW2	Pin 1 - SW2 Output Pin 2 - GND
J13	SW4	Pin 1 - SW4 Output Pin 2 - GND
J14	SW3A	Pin 1 - SW3A Output Pin 2 - GND
J15	SW3B	Pin 1 - SW3B Output Pin 2 - GND
J16	VGEN1/VGEN2	Pin 1 - VGEN1 Output Pin 2 - GND Pin 3 - VGEN2 Output
J18	VGEN3/VGEN4	Pin 1 - VGEN3 Output Pin 2 - GND Pin 3 - VGEN4 Output
J19	VGEN5/VGEN6	Pin 1 - VGEN5 Output Pin 2 - GND Pin 3 - VGEN6 Output

Table 2. Terminal Blocks descriptions (continued)

Connector	Function	Pin definition
J21	VSNVS/VREFDDR	Pin 1 - VSNVS Output Pin 2 - GND Pin 3 - VREFDDR Output
J25	Main Input Supply	Pin 1 - GND Pin 2 - PVIN Pin 3 - SWVIN
J29	Interfacing 1	Pin 1 - INTB Pin 2 - SDWNB Pin 3 - RESETBMCU
J32	Interfacing 2	Pin 1 - STANDBY Pin 2 - PWRON Pin 3 - GND
J31	I^2C Signals	Pin 1 - SCL Pin 2 - SDA
J33	VDDIO	Pin 1 - VDDIO Pin 2 - GND

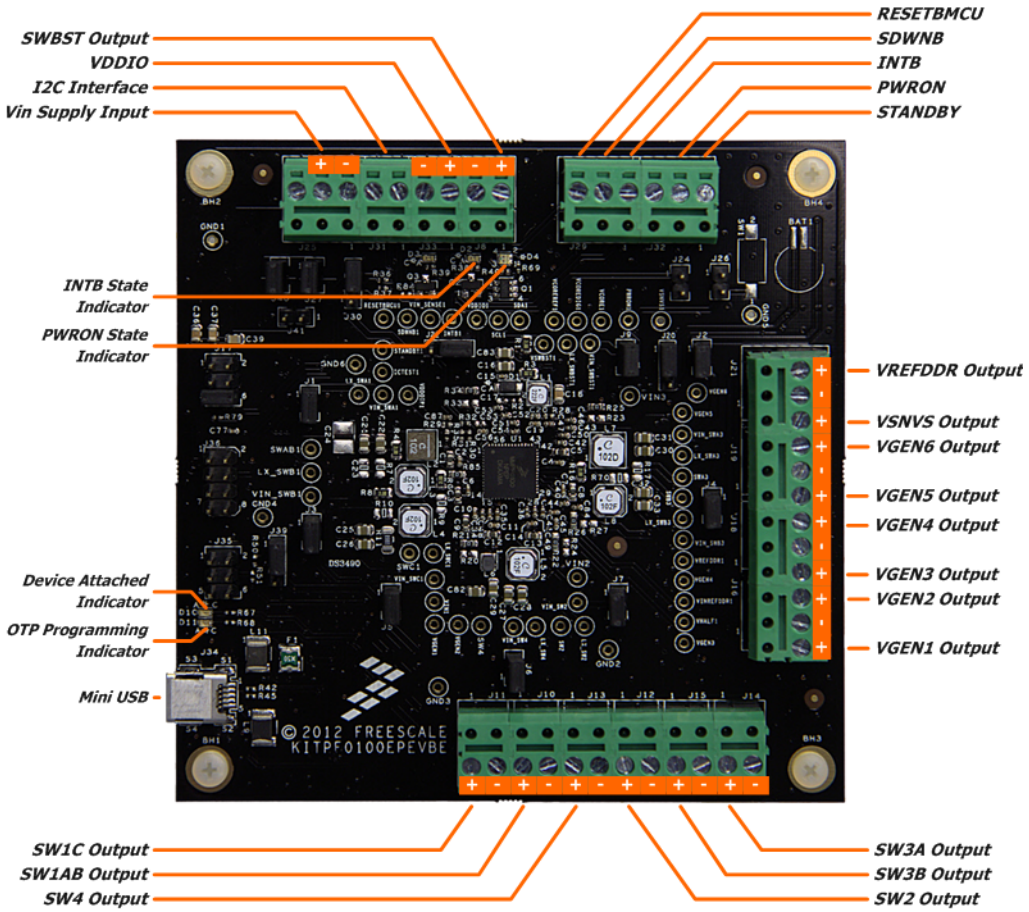
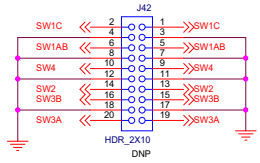
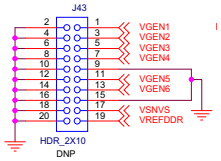
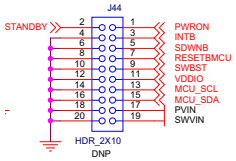


Figure 8. Input/Output Terminal Blocks

Table 3. Connector Description

Connector	Function	Pin definition
J34	Mini USB connector	Pin 1 - VBUS Pin 2 - D- Pin 3 - D+ Pin 4 - NC Pin 5 - GND Chassis - GND
J35	BDM connector	Pin 1 - BKGD_JM60 Pin 2 - GND Pin 3 - NC Pin 4 - RST_JM60 Pin 5 - NC Pin 6 - USB_PWR
J36	Programmer connector	Pin 1 - VDDOTPIN (8.5V boost output) Pin 2 - 3V3 (3.3 V LDO output) Pin 3 - GND Pin 4 - MCU_SCL (I^2C clock signal) Pin 5 - MCU_SDA (I^2C data signal) Pin 6 - PWRON (Controls the PWRON on the target device) Pin 7 - GPIO 1 (General Purpose GPIO) Pin 8 - GPIO 2 (General Purpose GPIO)
J42	Debug Port 1	Debugging connector for future development tools. 
J43	Debug Port 2	Debugging connector for future development tools 
J44	Debug Port 3	Debugging connector for future development tools 

9.3 Debug and Configuration Components

The KITPF0100EPEVBE allows full flexibility to change the default configuration of SW1A/B/C and SW3A/B outputs to one more suitable for a specific application scenario. It also provides several source options for the LDO supplies to test various loading and supplying scenarios.

Test points are provided on key nodes of the KITPF0100EPEVBE to allow full debugging capability during application development.

9.3.1 SW1A/B/C Configuration Components

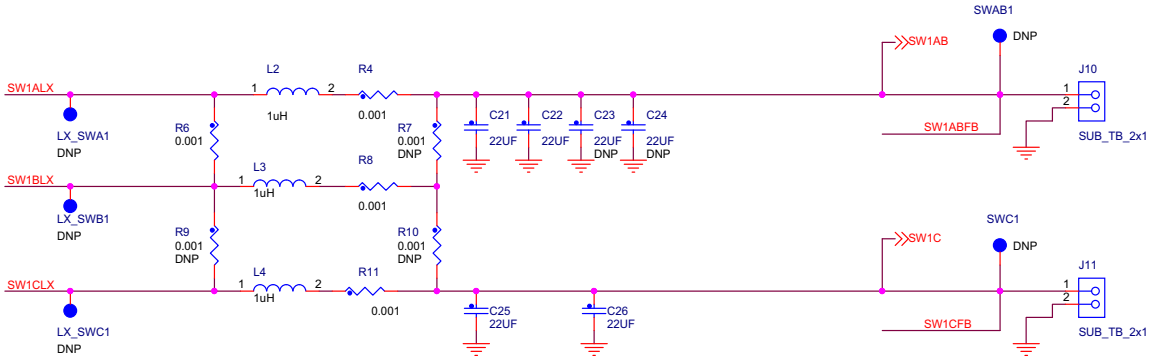


Figure 9. SW1A/B/C Output Configuration

The SW1A/B/C regulator can be configured in various operating modes as described in Table 4.

Table 4. SW1ABC Configuration Chart

Component	SW1A/B/C Single phase	SW1A/B Single phase SW1C independent	SW1A/B Dual phase SW1C independent
R6	Closed	Closed	DNP
R9	Closed	DNP	DNP
R4	Closed	Closed	Closed
R7	Closed	DNP	Closed
R8	DNP	DNP	Closed
R10	Closed	DNP	DNP
R11	DNP	Closed	Closed
L2	1.0 µH ISAT = 6.0 A	1.0 µH ISAT = 4.5 A	1.0 µH ISAT = 2.4 A
L3	N/A	N/A	1.0 µH ISAT = 2.4 A
L4	N/A	1.0 µH ISAT = 2.4 A	1.0 µH ISAT = 2.4 A

9.3.2 SW3A/B Configuration Components

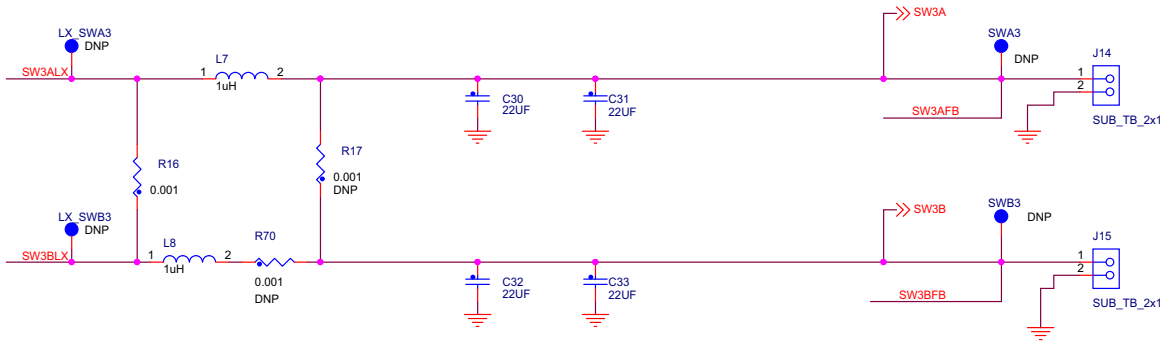


Figure 10. SW3A/B Output Configuration

The SW3A/B regulator can be configured in various operating modes as described in Table 5.

Table 5. SW3ABC Configuration Chart

Component	SW3A/B Single phase	SW3A/B Dual phase	SW3A Independent SW3B Independent
R16	Closed	DNP	DNP
R17	Closed	Closed	DNP
R70	DNP	Closed	Closed
L7	1.0 µH ISAT = 3.9A	1.0 µH ISAT = 3.0A	1.0 µH ISAT = 3.0 A
L8	N/A	1.0 µH ISAT = 3.0 A	1.0 µH ISAT = 3.0 A

9.3.3 LDO Input Supply Source Selection

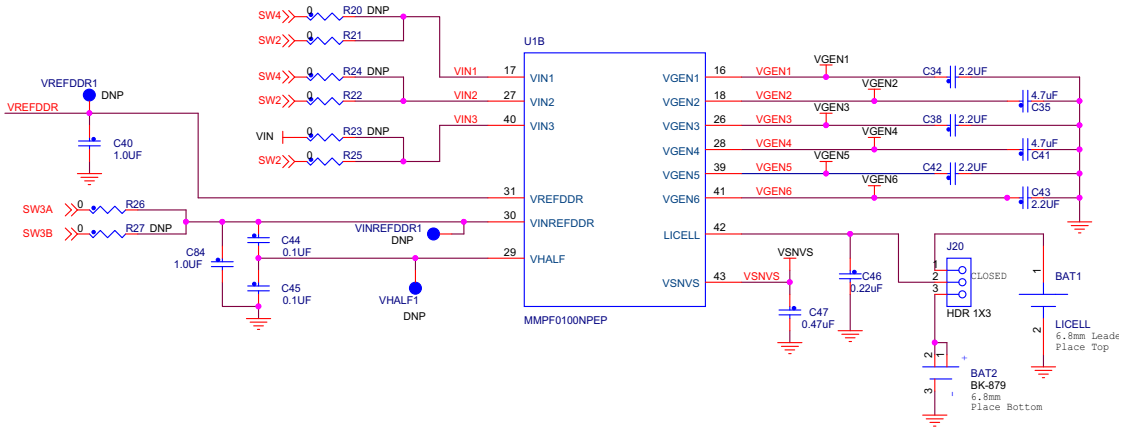


Figure 11. LDO Schematic Configuration

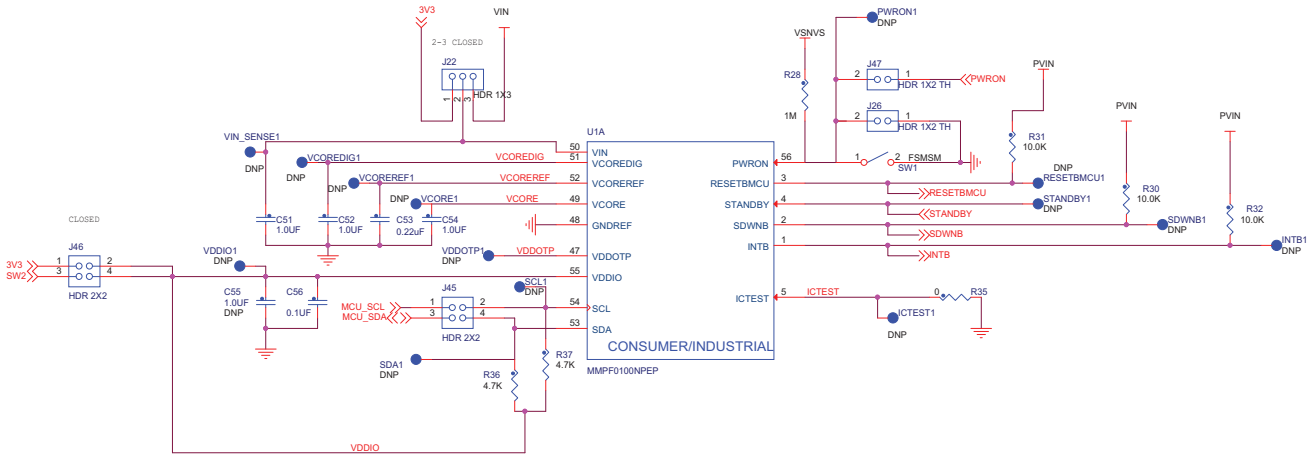


Figure 12. Logic and Core Supplies Schematic

Table 6. LDO Input Supply Configuration Chart

Input Pin	Input options
VIN1	Input supply for VGEN1 and VGEN2 R20 = SW4 R21 = SW2
VIN2	Input supply for VGEN3 and VGEN4 R24 = SW4 R22 = SW2
VIN3	Input supply for VGEN5 and VGEN6 R23 = VIN R25 = SW2
VINREFDDR	VREFDDR input supply R26 = SW3A R27 = SW3B
VDDIO	VDDIO Input supply 3V3 J46 = 1-2 SW2 J46 = 2-3

1. Make sure to populate only one option per input pin to avoid shorts between various sources.

9.3.4 Test point

All test points are clearly marked on the KITPF0100EPEVBE evaluation board. Figure 13 shows the location of various test points of interest during evaluation.

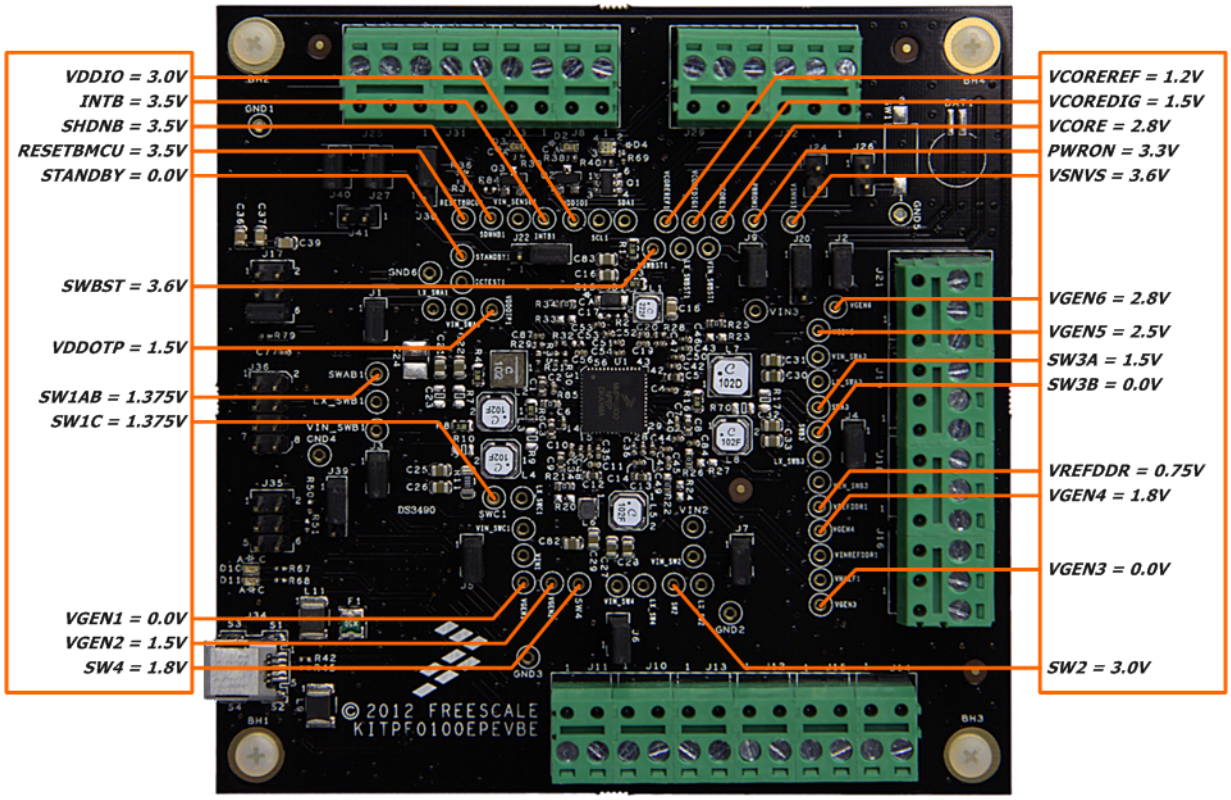


Figure 13. Key Test Point Locations and Default Voltages

9.4 Miscellaneous Components

9.4.1 Power on Push Button

A footprint for a normally open, momentary push-button is provided at the PWRON terminal to allow a momentary low state by pressing the push button. J47 allows isolation of the PWRON terminal from the MCU GPIO controlling this pin.

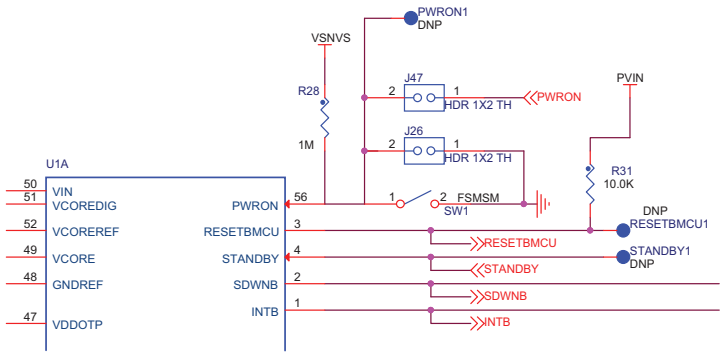


Figure 14. Power on Circuit

9.4.2 PMIC LED Indicators

LED indicators are provided to notify the PMIC status to the user. Figure 15 shows the PMIC status LEDs D2 and D4, and a Reserved LED indicator D3, that allows for an external rework connection to the transistor gate if any given signal debug is required.

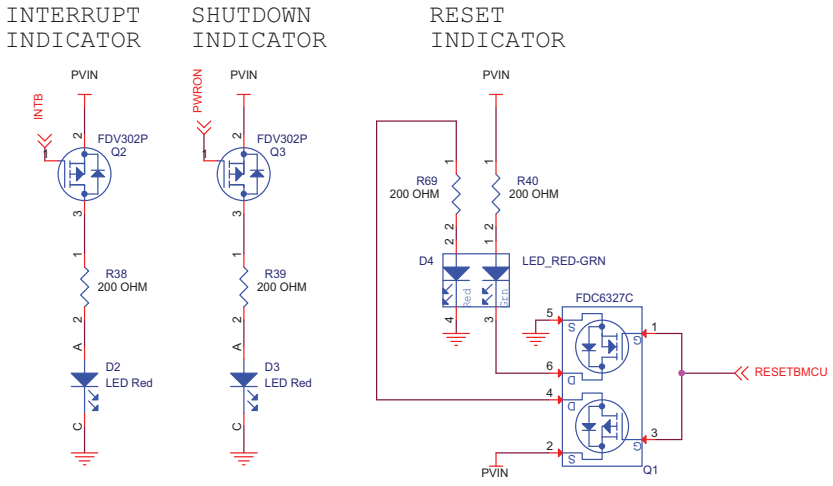


Figure 15. PMIC Status Indicator

Table 7 describes the meaning of the LED states.

Table 7. LED State Description

LED	Description
D2	Interrupt Notification ON = PMIC has detected an unmasked interrupt OFF = No interrupt detected
D4	RESETBMCU Notification Green = PMIC is in regulation and operating properly Red = PMIC is out of regulation
D3	Reserved debug LED ON = Q3 gate (R84 pad) is low OFF = Q3 gate (R84 pad) is high or floating

9.4.3 Control/Programming Interface

This onboard USB-to-I^{2}C interface comprises three basic blocks.

1. Controlling MCU (MC9S08JM60CGTE) for USB-I^{2}C translation.
2. 3.3 V LDO supply for external device controlling.
3. 8.25 V boost converter for OTP programming.

The control/programming interface allows one to program the onboard PF0100 PMIC. Alternatively, the interface can serve as a programmer for external devices though the connector J36.

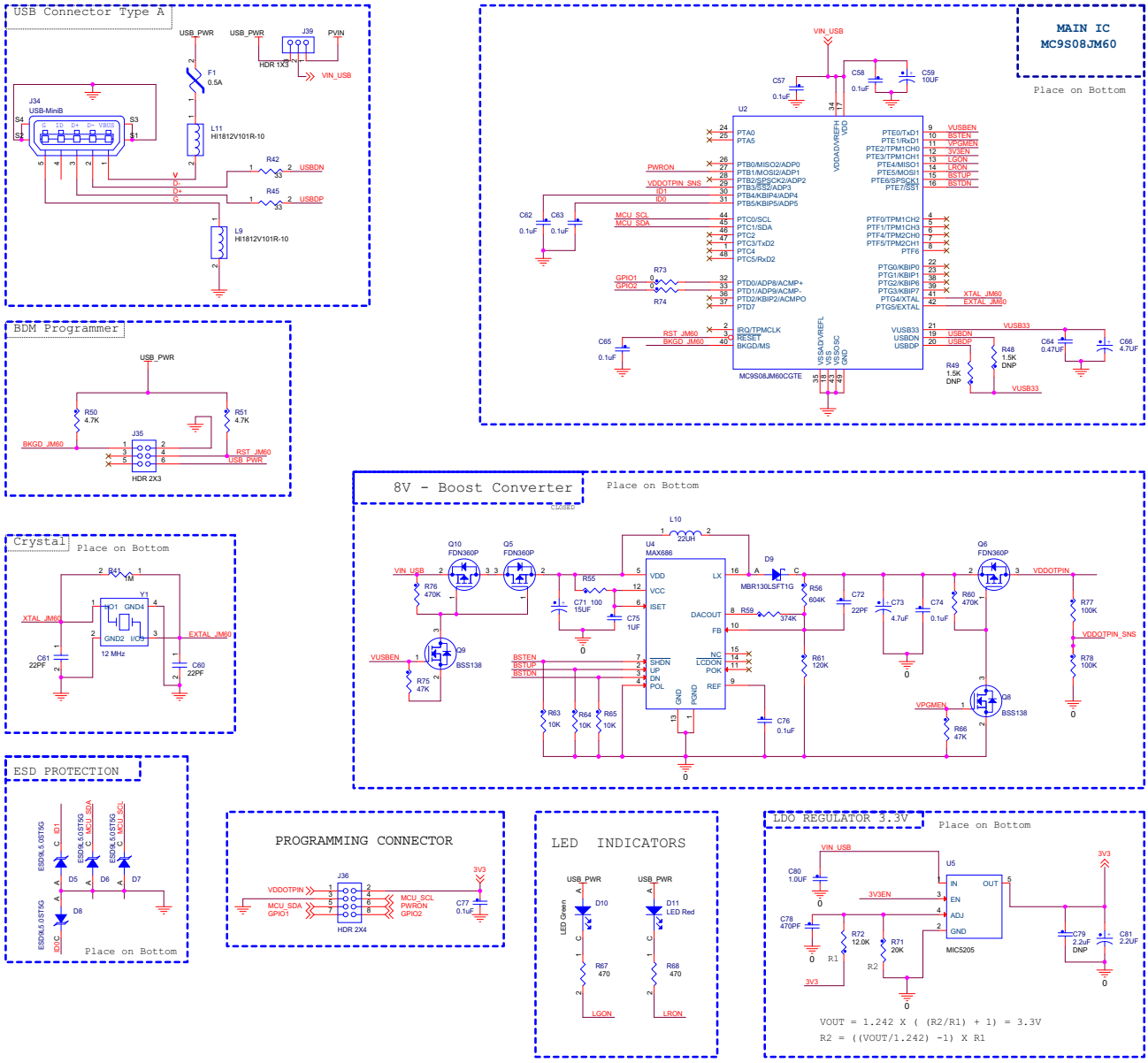


Figure 16. Control/Programming Interface Schematic

10 KITPF0100EPEVBE Board Layout

10.1 Assembly Layer Top

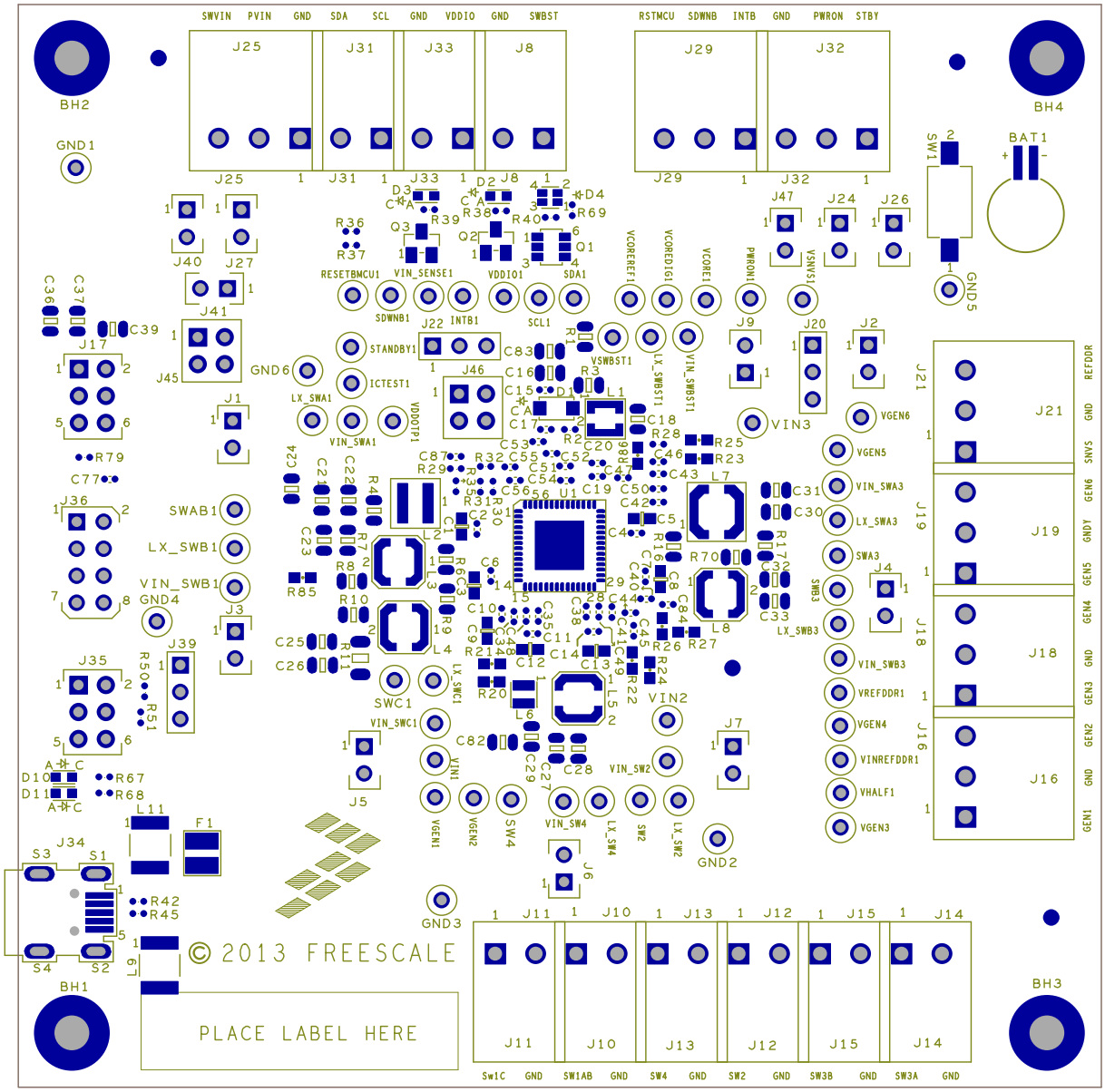


Figure 17. Assembly Top Layer

10.2 Assembly Layer Bottom

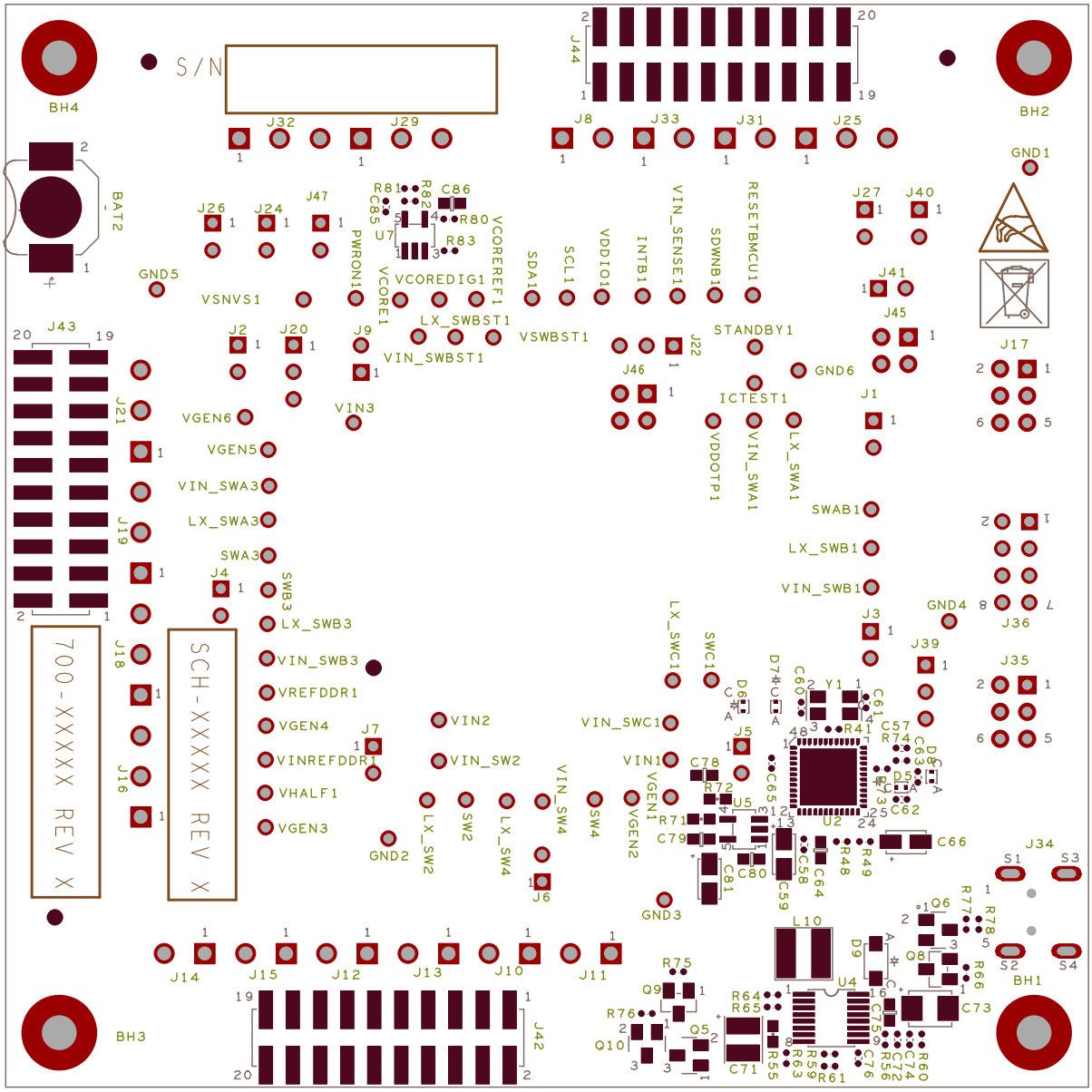


Figure 18. Assembly Layer Bottom

10.3 Top Layer Routing

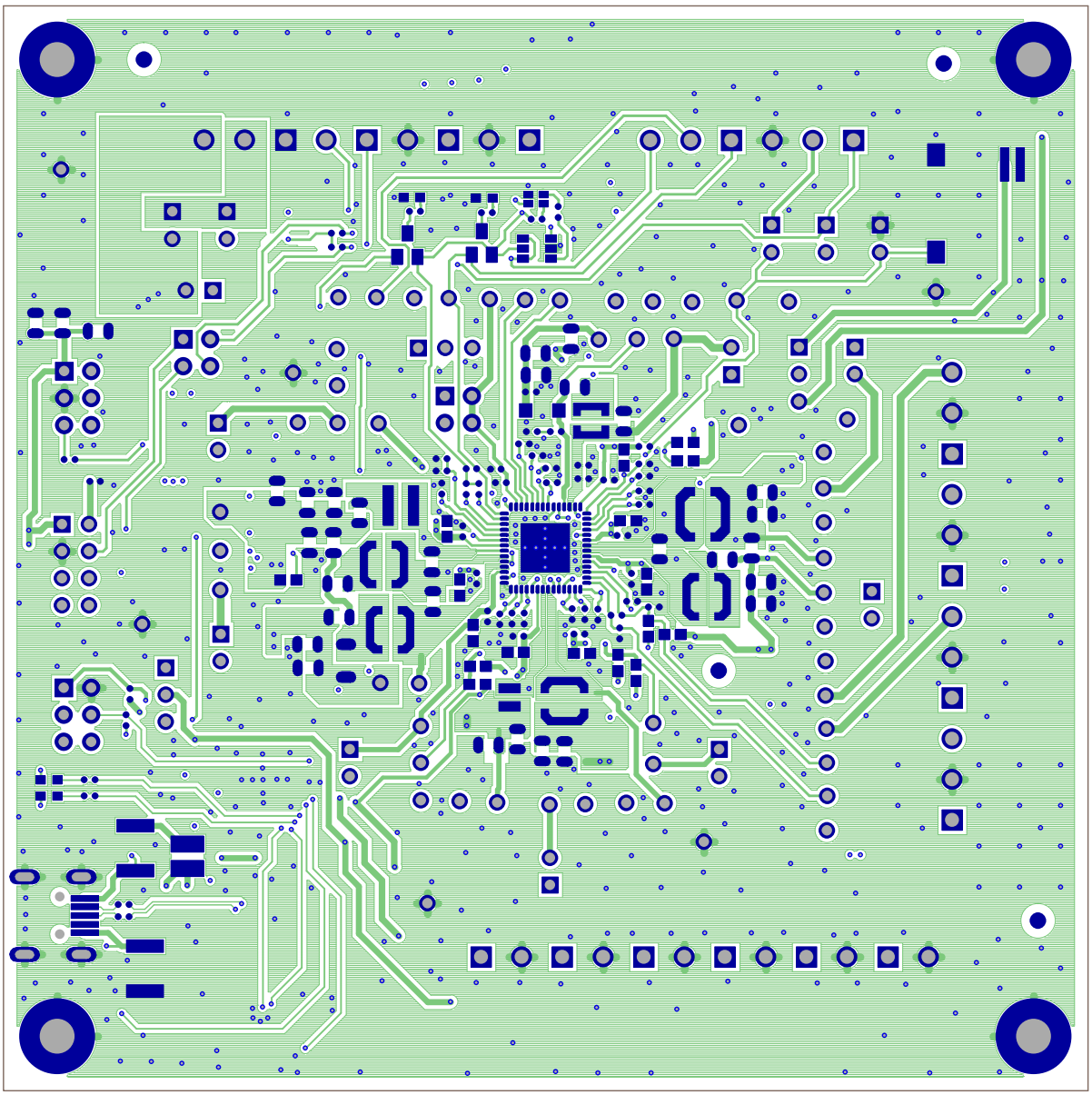


Figure 19. Top Layer Routing

10.4 Inner Layer 1 Routing

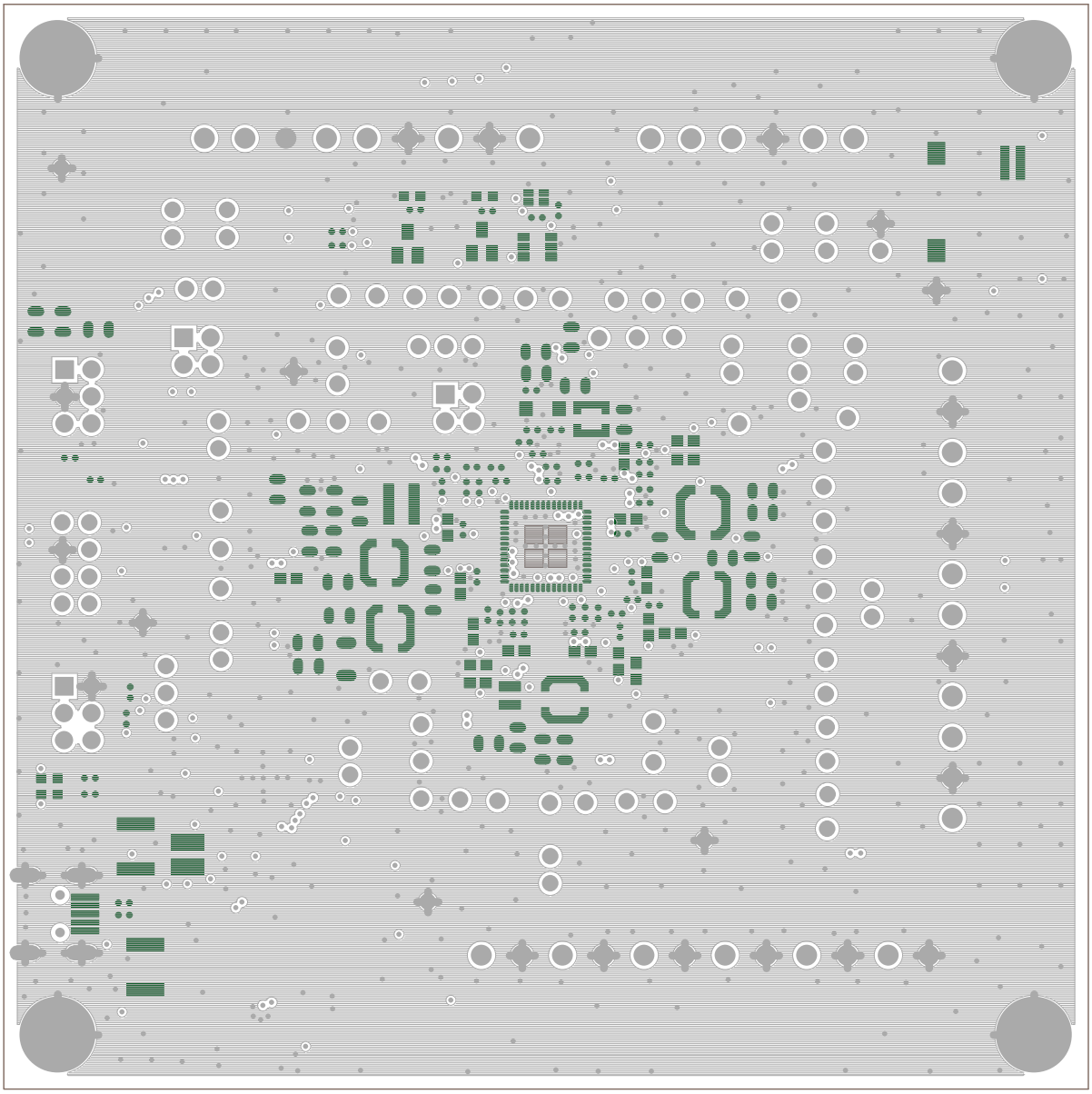


Figure 20. Inner Layer 1 Routing

10.5 Inner Layer 2 Routing

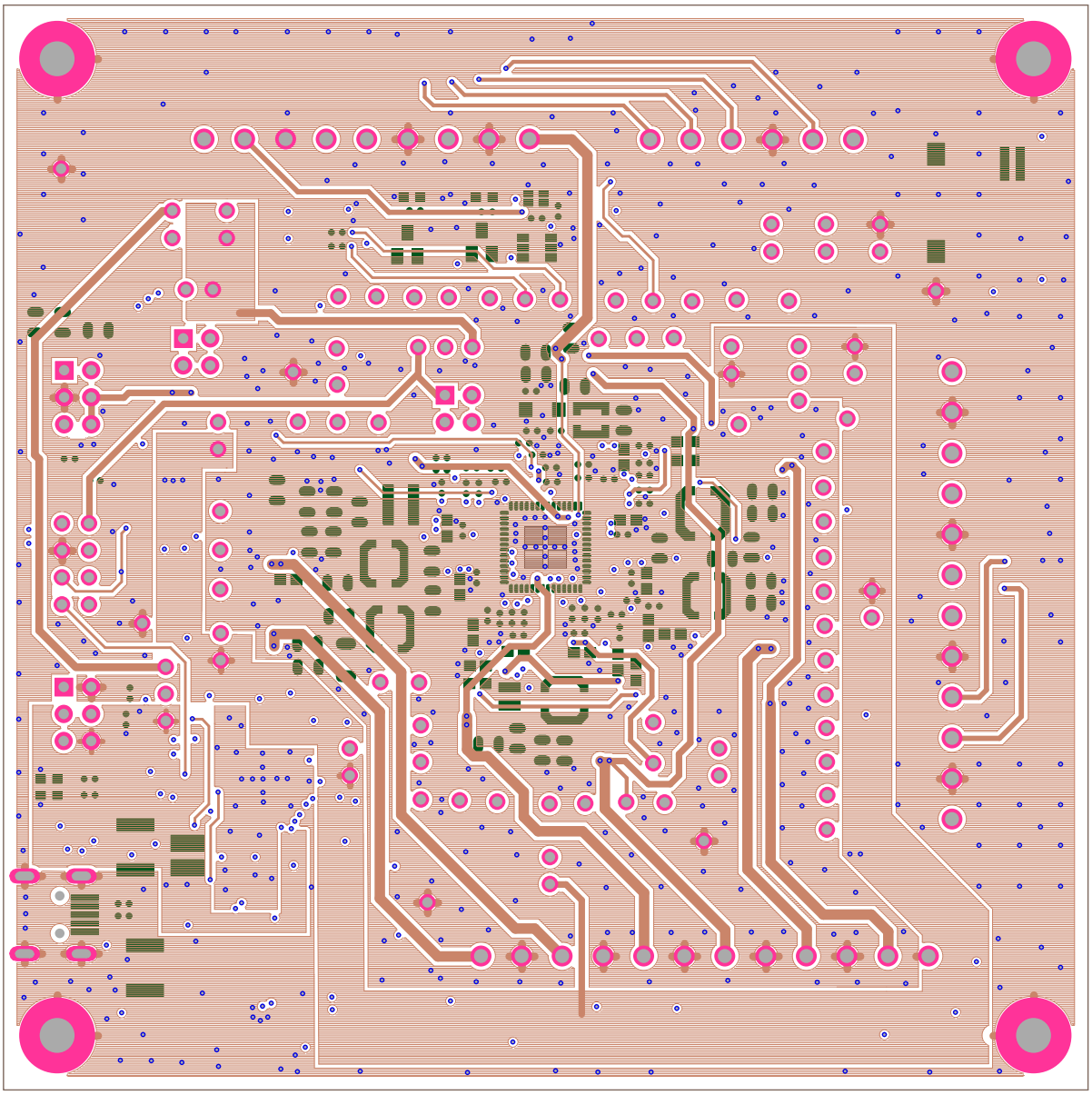


Figure 21. Inner Layer 2 Routing

10.6 Bottom Layer Routing

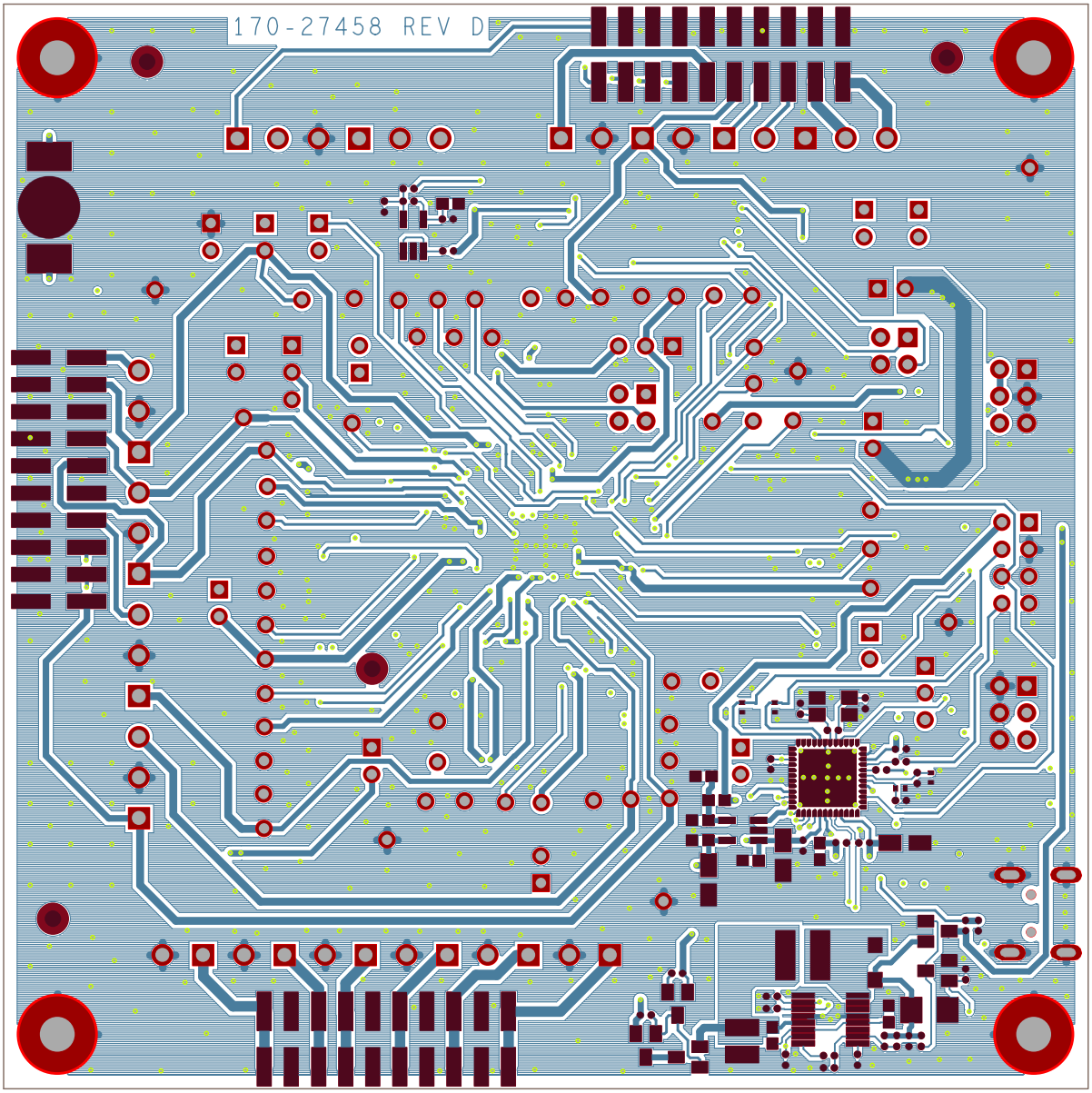


Figure 22. Bottom Layer Routing

11 Bill of Materials

Table 8. Bill of Materials [(2)]

Item	Qty	Schematic Label	Value/Description	Part Number	Assy Opt
Freescale Components					
1	1	U1	IC POWER MANAGEMENT CONSUMER/INDUSTRIAL QFN56	MMPF0100NPEP	
2	1	U2	IC MCU 8BIT 48 MHZ 60 KB FLASH 2.7-5.5 V QFN48	MC9S08JM60CGTE	
Active Components					
3	1	U4	IC DAC CTRL BOOST INV +/-27.5 V -- 2.7-5.5 V QSOP16	MAX686EEE+	
4	1	U5	IC LIN VREG LDO 1.5-15 V 150 MA 2.5-16 V SOT23-5	MIC5205YM5	
5	1	U7	IC LIN VREG LDO 1.5-15 V 150 MA 2.5-16 V SOT23-5	MIC5205YM5	(3)
6	1	Y1	XTAL 12 MHZ SER 9 PF SMT	ECS-120-9-42X-CKM-TR	
Diodes					
7	1	D1	DIODE SCH PWR RECT 1 A 20 V SMT	MBR120LSFT1G	
8	3	D2,D3,D11	LED RED SGL 30 MA 0603	SML-LXFM0603SIC-TR	
9	1	D4	LED DUAL GRN/RED 30 MA SMT	LTST-C195KGJRKT	
10	4	D5,D6,D7,D8	DIODE TVS ESD PROT ULT LOW CAP 5-5.4 V SOD-923	ESD9L5.0ST5G	
11	1	D9	DIODE SCH PWR RECT 1 A 30 V SOD-123	MBR130LSFT1G	
12	1	D10	LED GRN SGL 30 MA SMT 0603	SML-LXFM0603SUGCTR	
Capacitors					
13	7	C1,C3,C5,C8,C9,C12,C13	CAP CER 4.7 mF 10 V 10% X5R 0603	LMK107BJ475KA-T	
14	12	C2,C4,C6,C7,C10,C11,C14,C19,C44,C45,C56,C77	CAP CER 0.1 mF 10 V 10% X5R 0402	C0402C104K8PAC	
15	1	C15	CAP CER 0.01 mF 50 V 10% X7R 0402	GCM155R71H103KA55D	
16	16	C16,C21,C22,C23,C24,C25,C26,C27,C28,C29,C30,C31,C32,C33,C82,C83	CAP CER 22 mF 10 V 20% X5R 0805	LMK212BJ226MG-T	
17	1	C17	CAP CER 1000 pF 50 V X7R 5% 0402	0402X102J500SNT	(3)
18	1	C18	CAP CER 10 mF 10 V 10% X7R 0805	GRM21BR71A106KE51L	
19	5	C20,C34,C38,C42,C43	CAP CER 2.2 mF 6.3 V 20% X5R 0402	C0402C225M9PACTU	
20	2	C35,C41	CAP CER 4.7 mF 6.3 V 20% X5R 0402	C0402X5R6R3-475MNP	
21	3	C36,C37,C39	CAP CER 10 mF 16 V 10% X7R 0805	0805X106K160SNT	
22	9	C40,C48,C49,C50,C51,C52,C54,C84,C87	CAP CER 1.0 mF 10 V 10% X5R 0402	CC0402KRX5R6BB105	
23	2	C46,C53	CAP CER 0.22 mF 16 V 10% X7R 0402	GRM155R71C224KA12D	
24	1	C47	CAP CER 0.47 mF 10 V 10% X7R 0402	GMC04X7R474K10NT-LF	

Table 8. Bill of Materials [(2)]

Item	Qty	Schematic Label	Value/Description	Part Number	Assy Opt
25	1	C55	CAP CER 1.0 mF 10 V 10% X5R 0402	CC0402KRX5R6BB105	(3)
26	5	C57,C58,C62,C63,C65	CAP CER 0.1 mF 16 V 10% X5R 0402	C1005X5R1C104K	
27	1	C59	CAP TANT 10 mF 16 V 10% -- 3216-18	TAJA106K016R	
28	3	C60,C61,C72	CAP CER 22 pF 25 V 5% C0G 0402	C0402C0G250-220JNE	
29	1	C64	CAP CER 0.47 mF 16 V 10% X7R 0603	C0603C474K4RAC	
30	1	C66	CAP TANT 4.7 mF 10 V 10% -- 3216-18	T491A475K010AT	
31	1	C71	CAP TANT ESR 0.600 W 15 mF 25 V 10% -- 3528-21	TR3B156K025C0600	
32	1	C73	CAP TANT 4.7 mF 25 V 10% -- 3528-21	TAJB475K025RNJ	
33	1	C74	CAP CER 0.1 mF 25 V 10% X5R 0402	CC0402KRX5R8BB104	
34	1	C75	CAP CER 1.0 mF 25 V 10% X5R 0603	C0603C105K3PAC	
35	1	C76	CAP CER 0.1 mF 6.3 V 10% X7R 0402	C0402C104K9RACTU	
36	1	C78	CAP CER 470 pF 50 V 5% COG 0603	06035A471JAT2A	
37	1	C79	CAP CER 2.2 mF 16 V 10% X5R 0603	GRM188R61C225KE15D	(3)
38	1	C80	CAP CER 1.0 mF 16 V 10% X5R 0603	C1608X5R1C105K	
39	1	C81	CAP TANT ESR=1.800 W 2.2 mF 10 V 10% 3216-18	TPSA225K010R1800	
40	1	C85	CAP CER 2.2 mF 6.3 V 20% X5R 0402	C0402C225M9PACTU	(3)
41	1	C86	CAP CER 470 pF 50 V 5% COG 0603	06035A471JAT2A	(3)
Inductors					
42	1	L1	IND PWR 2.2 mH@100 kHZ 2.0 A 20% SMT	LPS3015-222ML_	
43	1	L2	IND PWR 1 mH@100 kHz 6 A 20% SMT	XAL4020-102MEC	
44	4	L3,L4,L5,L8	IND PWR 1 mH@100 kHZ 2.4 A 30% SMT	LPS4012-102NLC	
45	1	L6	IND PWR 1 mH@1 MHZ 2 A 30% SMT	VLS252010T-1R0N	
46	1	L7	IND PWR 1 mH@100 kHZ 2.65 A 20% SMT	LPS5015-102MLC	
47	1	L9	IND FER 100 W@100 MHZ 8 A 25% SMD/1812	HI1812V101R-10	
48	1	L10	IND PWR CHK 22 mH@1 kHZ 1 A 20% SMD	744773122	
49	1	L11	IND FER 100 W@100 MHZ 8 A 25% SMD/1812	HI1812V101R-10	
Resistors					
50	6	R1,R3,R4,R6,R8,R16	RES -- 0.001 W 1/4 W 5% 0805	LMI-R001-5.0	
51	1	R2	RES MF 1.0 W 1/16 W 1% 0402	RK73H1ETTP1R00F	(3)
52	5	R7,R9,R10,R17,R70	RES -- 0.001 W 1/4 W 5% 0805	LMI-R001-5.0	(3)
53	1	R11	RES MF 0.001 W 1 W 1% 1206	CSNL1206FT1L00	
54	5	R20,R23,R24,R27,R86	RES MF ZERO W 1/10 W 1% 0603	MC0603SAF0000T5E	(3)
55	5	R21,R22,R25,R26,R85	RES MF ZERO W 1/10 W 1% 0603	MC0603SAF0000T5E	
56	2	R28,R41	RES MF 1.0 MW 1/16 W 1% AEC-Q200 0402	CRCW04021M00FKED	

Table 8. Bill of Materials [(2)]

Item	Qty	Schematic Label	Value/Description	Part Number	Assy Opt
57	2	R29,R79	RES MF 100 KW 1/16 W 5% 0402	RK73B1ETTP104J	
58	3	R30,R31,R32	RES MF 10.0 KW 1/16 W 1% AEC-Q200 0402	CRCW040210K0FKED	
59	3	R35,R73,R74	RES MF 0 W 1/10 W -- 0402	ERJ-2GE0R00X	
60	4	R36,R37,R50,R51	RES MF 4.70 KW 1/16 W 1% 0402	RK73H1ETTP4701F	
61	4	R38,R39,R40,R69	RES MF 200 W 1/10 W 1% 0402	ERJ2RKF2000X	
62	2	R42,R45	RES MF 33.0 W 1/16 W 1% 0402	CR-02FL6---33R	
63	2	R48,R49	RES MF 1.5 KW 1/16 W 5% 0402	CRCW04021K50JNED	(3)
64	1	R55	RES MF 100 W 1/10 W 1% 0603	RK73H1JTTD1000F	
65	1	R56	RES MF 604 KW 1/16 W 1% 0402	ERJ2RKF6043X	
66	1	R59	RES MF 374 KW 1/16 W 1% 0402	RK73H1ETTP3743F	
67	2	R60,R76	RES MF 470 KW 1/16 W 1% 0402	RK73H1ETTP4703F	
68	1	R61	RES MF 120 KW 1/16 W 1% 0402	RK73H1ETTP1203F	
69	3	R63,R64,R65	RES MF 10 KW 1/16 W 5% 0402	CRCW040210K0JNED	
70	2	R66,R75	RES MF 47 KW 1/16 W 1% 0402	RK73H1ETTP4702F	
71	2	R67,R68	RES MF 470 W 1/16 W 1% 0402	CR-02FL6--470R	
72	1	R71	RES MF 20 KW 1/10 W 5% 0603	CR0603-JW-203ELF	
73	1	R72	RES MF 12.0 KW 1/10 W 1% 0603	RK73H1JTTD1202F	
74	2	R77,R78	RES MF 100 KW 1/16 W 1% 0402	RC0402FR-07100KL	
75	1	R80	RES MF 27 KW 1/16 W 5% 0402	CRCW040227K0JNED	(3)
76	1	R81	RES MF 470 KW 1/16 W 5% 0402	CR0402-16W-474JT	(3)
77	2	R82,R83	RES MF 0 W 1/10 W -- 0402	ERJ-2GE0R00X	(3)
Transistors					
78	1	Q1	TRAN MOSFET DUAL N & P CHANNEL 2.5 V S-SOT6	FDC6327C	
79	2	Q2,Q3	TRAN PMOS SW 120 MA 25 V SOT23	FDV302P	
80	3	Q5,Q6,Q10	TRAN PMOS SW 2 A 30 V SSOT3	FDN360P	
81	2	Q8,Q9	TRAN NMOS 50 V 220 MA SOT-23	BSS138	

Table 8. Bill of Materials [(2)]

Item	Qty	Schematic Label	Value/Description	Part Number	Assy Opt
Switches, Connectors, Jumpers and Test Points					
82	56	VSWBST1,VSNVS1,VREFDDR1,VIN_SWC1,VIN_SWBST1,VIN_SWB1,VIN_SWA1,VIN_SENSE1,VINREFDDR1,VIN1,VHALF1,VGEN1,VDDOTP1,VDDIO1,VCOREREF1,VCOREDIG1,VCORE1,SWC1,SWAB1,STANDBY1,SDWNB1,SDA1,SCL1,RESETBMCU1,PWRON1,LX_SWC1,LX_SWBST1,LX_SWB1,LX_SWA1,INTB1,ICTEST1,GND1,VIN_SW2,VIN2,VGEN2,SW2,LX_SW2,GND2,VIN_SWB3,VIN_SWA3,VIN3,VGEN3,SWB3,SWA3,LX_SWB3,LX_SWA3,GND3,VIN_SW4,VGEN4,SW4,LX_SW4,GND4,VGEN5,GND5,VGEN6,GND6	TEST POINT RED 40 MIL DRILL 180 MIL TH 109L	5000	(3)
83	14	J1,J2,J3,J4,J5,J6,J7,J9,J24,J26,J27,J40,J41,J47	HDR 1X2 TH 100 MIL SP 339H AU 118L	210-91-02GB01	
84	9	J8,J10,J11,J12,J13,J14,J15,J31,J33	SUBASSEMBLY CON 1X2 TB TH 3.81 MM SP 201H -- 138L + TERM BLOCK PLUG 3.81MM 2POS	210-80097, 210-80098	
85	7	J16,J18,J19,J21,J25,J29,J32	SUBASSEMBLY CON 1X3 TB TH 3.81 MM SP 201H -- 138L + TERM BLOCK PLUG 3.81MM 3POS	210-80099,211-79220	
86	2	J17,J35	HDR 2X3 TH 100 MIL CTR 335H AU 95L	TSW-103-07-S-D	
87	3	J20,J22,J39	HDR 1X3 TH 100 MIL SP 340H AU 118L	M20-9990345	
88	1	J34	CON 5 USB MINI-B RA SHLD SKT SMT 31 MIL SP AU	675031340	
89	1	J36	HDR 2X4 TH 100 MIL CTR 425H AU 310L	TSW-104-16-G-D	
90	3	J42,J43,J44	CON 2X10 SKT SMT 100 MIL CTR 390H AU	SSW-110-22-F-D-VS-N	
91	2	J45,J46	HDR 2X2 TH 100 MIL CTR 340H SN 105L	5-146258-2	
92	1	SW1	SW SPST PB 12V 50 MA SMT	1437566-4	(3)
Misc					
93	1	BAT1	BATTERY LITHIUM -- 3 V 5.5 MAH	MS621F-FL11E	
94	1	BAT2	HOLDER COIN CELL 6.8 MM SMT	BK-879	(3)
95	4	BH1,BH2,BH3,BH4	MOUNTING HOLE 0.130 INCH, no part to order	not a part to order	

Table 8. Bill of Materials [(2)]

Item	Qty	Schematic Label	Value/Description	Part Number	Assy Opt
96	1	F1	FUSE PLYSW 0.5 A 13.2 V SMT	MICROSMD050F-2	

Notes:

2. Freescale does not assume liability, endorse, or warrant components from external manufacturers that are referenced in circuit drawings or tables. While Freescale offers component recommendations in this configuration, it is the customer's responsibility to validate their application
3. Do Not Populate

12 References

Document Number	Description	URL
MMPF0100	Data Sheet	http://cache.freescale.com/files/analog/doc/data_sheet/MMPF0100.pdf
MMPF0100ER	Errata	http://cache.freescale.com/files/analog/doc/errata/MMPF0100ER.pdf
PFSERIESFS	Fact Sheet	http://cache.freescale.com/files/analog/doc/fact_sheet/PFSeriesFS.pdf
AN4622	Layout Application Note	http://cache.freescale.com/files/analog/doc/app_note/AN4622.pdf
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KITPF0100EPEVBE	Tool Summary Page	www.freescale.com/KITPF0100EPEVBE
	Analog Home Page	www.freescale.com/analog
	Power Management Home Page	www.freescale.com/PMIC

12.1 Support

Visit Freescale.com/support for a list of phone numbers within your region.

12.2 Warranty

Visit Freescale.com/warranty to submit a request for tool warranty.

13 Revision History

Revision	Date	Description of Changes
1.0	11/2012	• Initial Release
2.0	2/2013	• Updated document for the latest GUI Revision 3.0.0.20 • Added Figure 14 to section **8 Evaluation Board Schematic** • Added TBB operation Mode. • Updated section 12.4 Using the Script Editor • Updated section 12.5 Loading a Configuration File
3.0	12/2013	• Added section **5 MMPF0100 Features** • Added section **6 Hardware/Software Requirements**
4.0	2/2015	• Removed references to older revision of EVB and GUI
5.0	8/2015	• Updated the Evaluation Board Schematic and related descriptions
	8/2015	• Deleted section 6 KITPF0100EPEVBE Hardware/Software Deviation • Deleted Manufacturer column from **Table 8**

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Rev. 5.0
8/2015