AP1155ADL

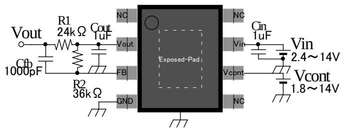
Suitable for High Power application
Low Noise, Adjustable Voltage LDO Regulator

1. Genaral Description

The AP1155ADL is a low dropout linear regulator with ON/OFF control, which can supply 1A load current. The AP1155ADL is housed in HSOP-8 with Exposed-Pad package, and therefore suitable for high power application. The AP1155ADL realizes high ripple rejection and low noise, because silicon monolithic bipolar structure is adopted. The suitable voltage for the set can be set from 1.3V to 13.5V by external resistors. The AP1155ADL realizes to downsize Printed Circuit Board, because the input and output capacitor is available to use a small ceramic capacitor. Also over-current protection circuit and thermal shut down are integrated. These functions will improve reliability of the system.

2. Features

- Operating Temperature Range -40～85℃
- Operating Voltage Range 2.4～14.0V
- Output Current 1A
- Programmable Output Voltage 1.3～13.5V
- Reference Voltage Precision 1.21V ± 35mV
- Dropout Voltage 300mV at Iout=1A
- Ripple Rejection Ratio 80dB at 1kHz
- Available very low noise application
- Available to use a small ceramic capacitor
- On/Off control (High active)
- Built-in Over Current Protection, Thermal Shutdown Protection
- Package HSOP-8pin with Exposed-Pad



3. Applications

- RF Power Supplies — PLL, VCO, Mixers, LNA
- Low Noise Imaging Equipment — Digital Camera
- High Speed/High Precision A-D, D-A, Amplifier — Audio Equipment, Medical Equipment, Instrumentation
- Precision Power Supplies
- Post Regulator for Switching Supplies — Car Infotainment

4. Table of Contents

5. Block Diagram

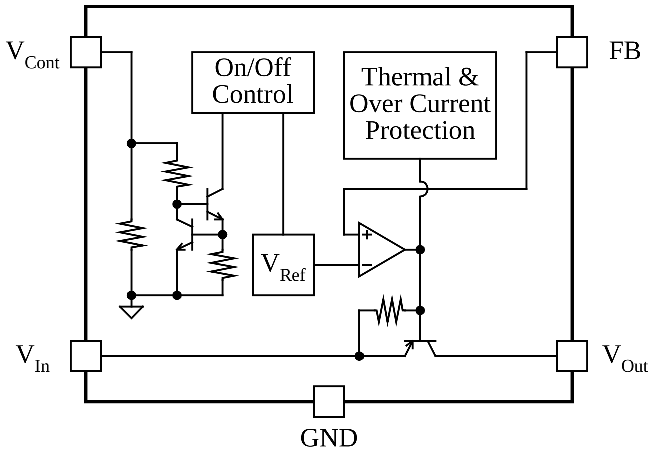


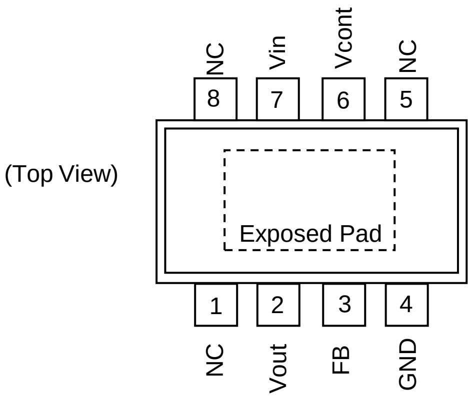
Figure 1.Block Diagram

6. Ordering Information

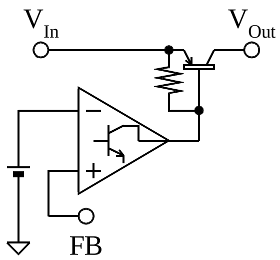
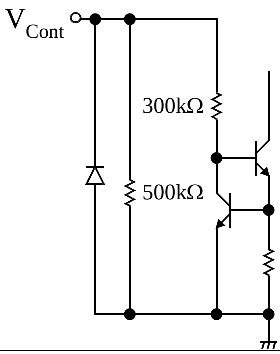
AP1155ADL   Ta = -40 to 85°C   HSOP-8

7. Pin Configurations and Functions

■ Pin Configurations



■ Function

Pin Number	Symbol	Internal Equivalent Circuit	Description
1,5,8	NC	–	**Non connection Terminal**
2	V_{Out}		**Output Terminal** Connect resistance R_1 between V_{Out} terminal and Fb terminal, and resistance R_2 between Fb terminal and GND. Output voltage $V_{Out,TYP}$ is determined by the following equation: $V_{Out,TYP} = V_{Fb} \times \frac{R_1 + R_2}{R_2}$ Connect a ceramic capacitor with a capacitance higher than the following values between V_{Out} terminal and GND. $V_{Out,TYP} \geq 2.4V$: 1μF $V_{Out,TYP} < 2.4V$: 2.2μF
3	FB		**Feedback Terminal** Connecting a capacitor between V_{Out} terminal and Fb terminal reduces output noise. This terminal features very high impedance; please note that it is susceptible to external noise, etc.
4	GND	-	**GND Terminal**
6	V_{Cont}		**On/Off control Terminal** The On/Off voltages are as follows: $V_{Cont} \geq 1.8V$: V_{Out} On state $V_{Cont} \leq 0.35V$: V_{Out} Off state Pull-down resistance (500kΩ) is built-in.
7	V_{In}	-	**Input Terminal** Connect a capacitor of 1μF or higher between V_{In} terminal and GND.
-	Exposed Pad	–	**Ground Terminal** **Heat dissipation pad** Exposed Pad must be connected to GND.

8. Absolute Maximum Ratings

Parameter	Symbol	min	Max	Unit	Condition
Input Voltage	$V_{In,MAX}$	-0.4	16	V	
Reverse Bias Voltage	$V_{Rev,MAX}$	-0.4	14	V	V_{Out}-V_{In}
FB Terminal Voltage	$V_{FB,MAX}$	-0.4	5	V	
Control Voltage	$V_{Cont,MAX}$	-0.4	16	V	
Junction temperature	Tj	-	150	°C	
Storage Temperature Range	T_{Stg}	-55	150	°C	
Power Dissipation	P_D	-	2300	mW	Ta=25°C (Note 1)

Note 1. A 2-layer board is used(x=30mm, y=30mm,t=1.0mm). $R_{\theta JA}$ = 50°C/W.
Please refer to Section 11.8 on page 17 for more information.

WARNING: The maximum ratings are the absolute limitation values with the possibility of the IC breakage. When the operation exceeds this standard quality cannot be guaranteed.

9. Recommended Operating Conditions

Parameter	Symbol	min	typ	max	Unit	Condition
Operating Temperature Range	Ta	-40	-	85	°C	
Operating Voltage Range	V_{OP}	2.4	-	14.0	V	
Output Voltage Range	V_{Out}	1.3	-	13.5	V	

10. Electrical Characteristics

■ Electrical Characteristics of Ta=Tj=25°C

The parameters with min or max values will be guaranteed at T_a=T_j=25°C.

(V_{In}=4.0V, R1=53kΩ, R2=36kΩ, Vcont=1.8V, Ta=Tj=25°C, unless otherwise specified.)

Parameter	Symbol	Condition	min	typ	max	Unit
Fb voltage	V_{FB}	I_{Out}=5mA	1.185	1.210	1.245	V
Line Regulation	LinReg	ΔV_{In}=5V, I_{Out}=5mA	-	0	10	mV
Load Regulation (Note 2)	LoaReg	I_{Out}=5~500mA	-	6	20	mV
		I_{Out}=5~1000mA	-	20	35	
Dropout Voltage (Note 3)	V_{Drop}	I_{Out}=500mA	-	150	260	mV
		I_{Out}=1000mA	-	300	490	
Maximum Output Current (Note 4)	$I_{Out,Max}$	V_{Out}=$V_{Out,TYP}$×0.9	1100	1400	1700	mA
Output Short-Circuit Current	I_{Short}	V_{Out}=0V	-	1500	-	mA
Quiescent Current	Iq	I_{Out}=0mA	-	300	480	μA
Standby Current	$I_{Standby}$	V_{Cont}=0V	-	-	0.1	μA
Control Current	I_{Cont}	V_{Cont}=1.8V	-	5	10	μA
Control Voltage	V_{Cont}	V_{Out} On state	1.8	-	-	V
		V_{Out} Off state	-	-	0.35	V

Note 2. Load Regulation changes with output voltage. The value mentioned above is guaranteed with the condition at $V_{Out,TYP}$=3.0V (R_1=53kΩ, R_2=36kΩ). The standard value is displayed by the absolute value.
Note 3. For $V_{Out,TYP}$≤2.0V , no regulations.
Note 4. The maximum output current is limited by power dissipation
Note 5. Parameters with only typical values are just reference. (Not guaranteed)

■ Electrical Characteristics of Ta=-40°C~85℃

The parameters with min or max values will be guaranteed at T_a = -40 ~ 85°C.

(V_{In}=4.0V, R1=53kΩ, R2=36kΩ, Vcont=1.8V, Ta= -40 ~ 85°C, unless otherwise specified.)

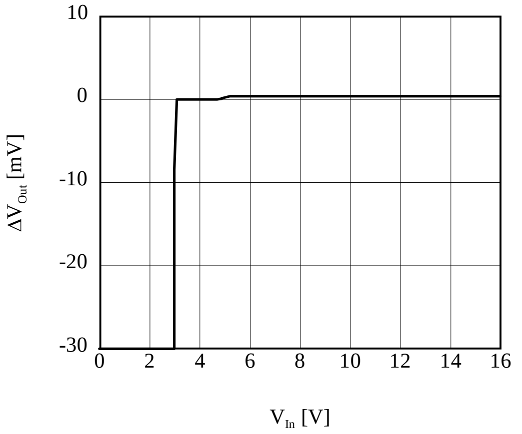
Parameter	Symbol	Condition	min	typ	max	Unit
Fb voltage	V_{FB}	I_{Out}=5mA	1.175	1.210	1.255	V
Line Regulation	LinReg	ΔV_{In}=5V, I_{Out}=5mA	-	0	16	mV
Load Regulation (Note 6)	LoaReg	I_{Out}=5~500mA	-	6	37	mV
		I_{Out}=5~1000mA	-	20	95	
Dropout Voltage (Note 7)	V_{Drop}	I_{Out}=500mA	-	150	335	mV
		I_{Out}=1000mA	-	300	550	
Maximum Output Current (Note 8)	$I_{Out,Max}$	V_{Out}=$V_{Out,TYP}$×0.9		1400	-	mA
Output Short-Circuit Current	I_{Short}	V_{Out}=0V	-	1500	-	mA
Quiescent Current	Iq	I_{Out}=0mA	-	300	585	μA
Standby Current	$I_{Standby}$	V_{Cont}=0V	-	-	1.5	μA
Control Current	I_{Cont}	V_{Cont}=1.8V	-	5	15	μA
Control Voltage	V_{Cont}	V_{Out} On state	1.8	-	-	V
		V_{Out} Off state	-	-	0.35	V

Note 6. Load Regulation changes with output voltage. The value mentioned above is guaranteed with the condition at $V_{Out,TYP}$=3.0V (R_1=53kΩ, R_2=36kΩ). The standard value is displayed by the absolute value.
Note 7. For $V_{Out,TYP}$≤2.0V , no regulations.
Note 8. The maximum output current is limited by power dissipation
Note 9. Parameters with only typical values are just reference. (Not guaranteed)

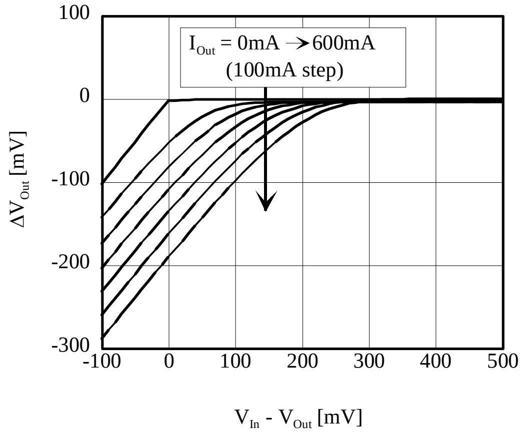
11. Description

11.1 DC Characteristics

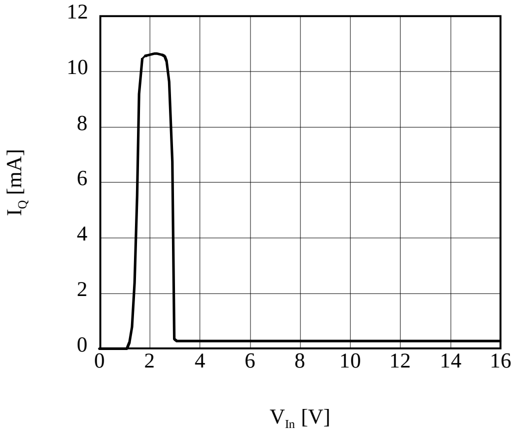
■ ΔV_{Out} vs V_{In} (AP1155ADL)



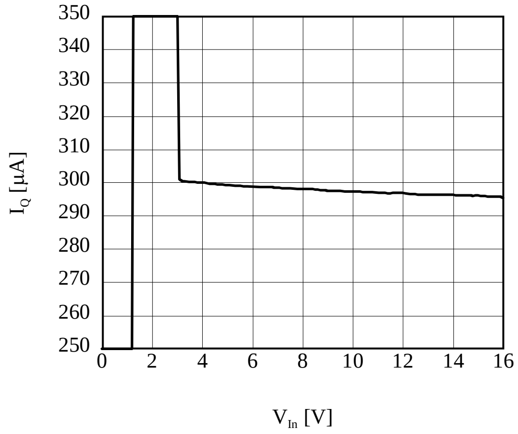
■ ΔV_{Out} vs V_{In} (AP1155ADL)



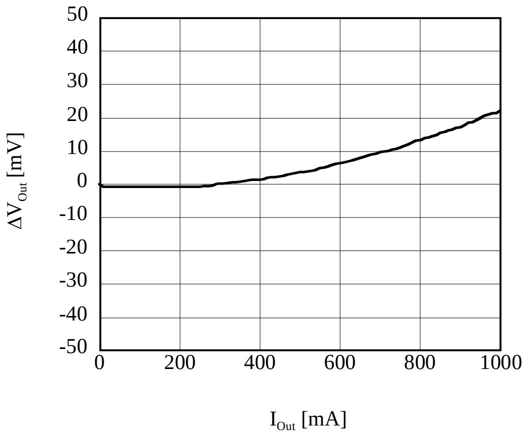
■ I_Q vs V_{In} (AP1155ADL)



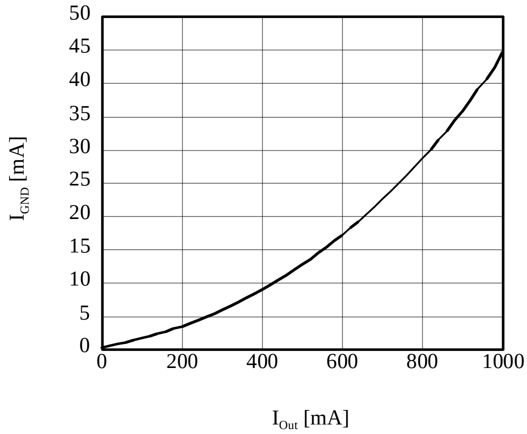
■ I_Q vs V_{In} (AP1155ADL)



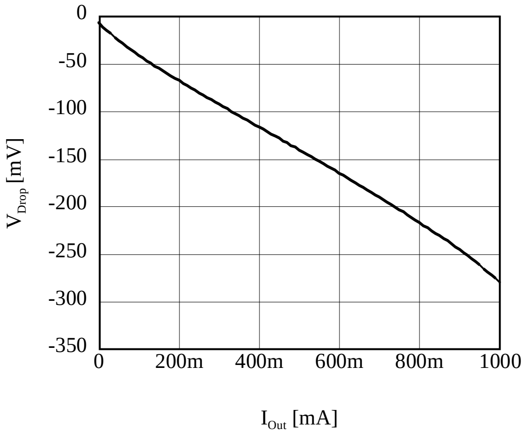
■ ΔV_{Out} vs I_{Out} (AP1155ADL)



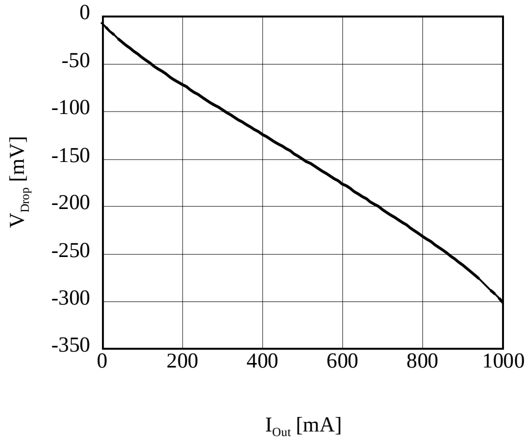
■ I_{GND} vs I_{Out} (AP1155ADL)



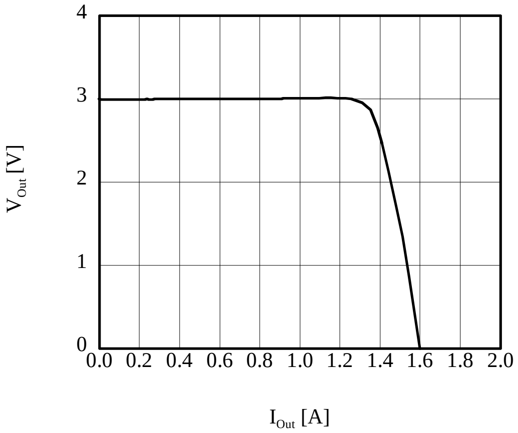
■ V_{Drop} vs I_{Out} (AP1155ADL)



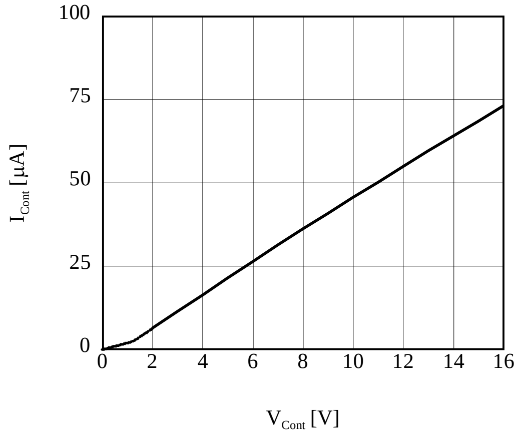
■ V_{Drop} vs I_{Out} (AP1155ADL)



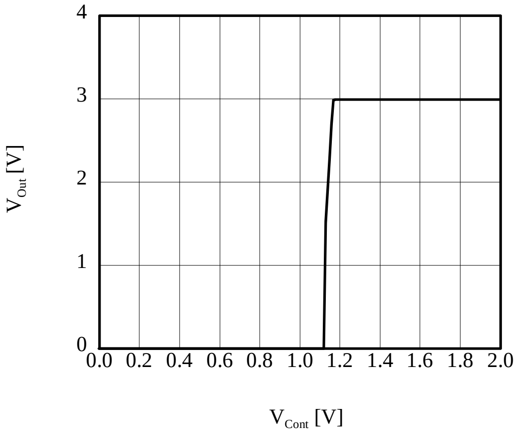
■ V_{Out} vs I_{Out} (AP1155ADL)



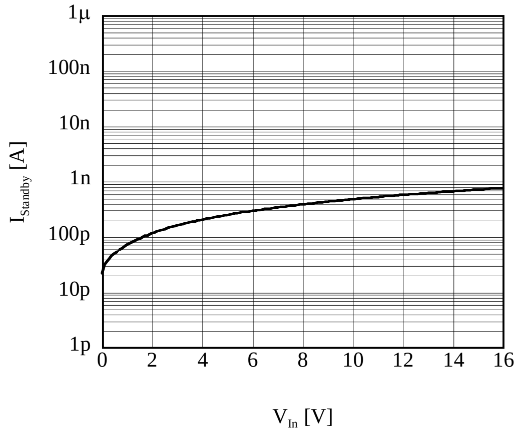
■ I_{Cont} vs V_{Cont} (AP1155ADL)



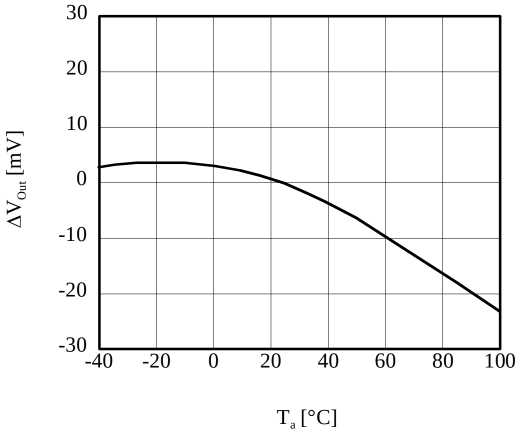
■ V_{Out} vs V_{Cont} (AP1155ADL)



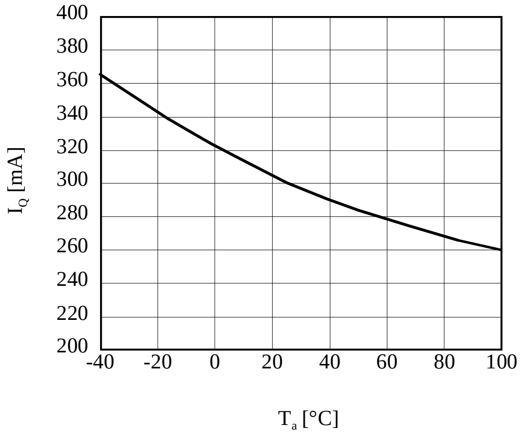
■ $I_{Standby}$ vs V_{In} (AP1155ADL)



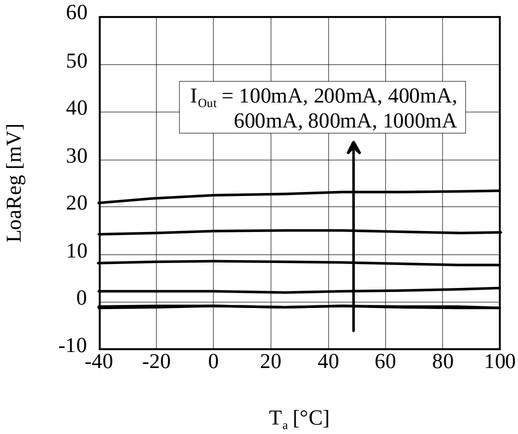
■ ΔV_{Out} vs T_a (AP1155ADL)



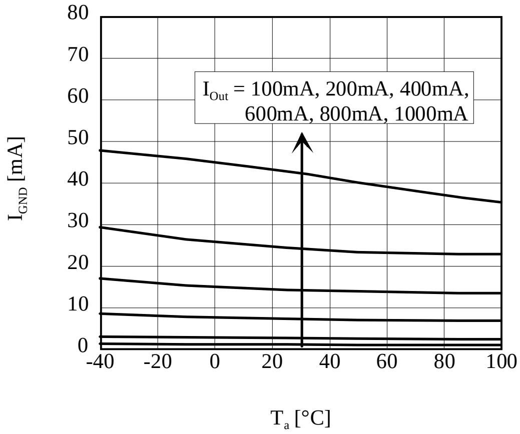
■ I_Q vs T_a (AP1155ADL)



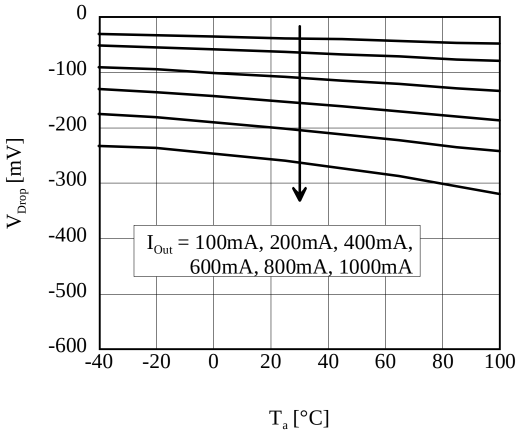
■ LoaReg vs T_a (AP1155ADL)



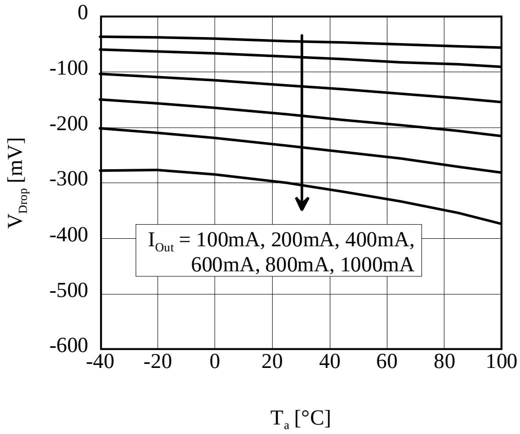
■ I_{GND} vs T_a (AP1155ADL)



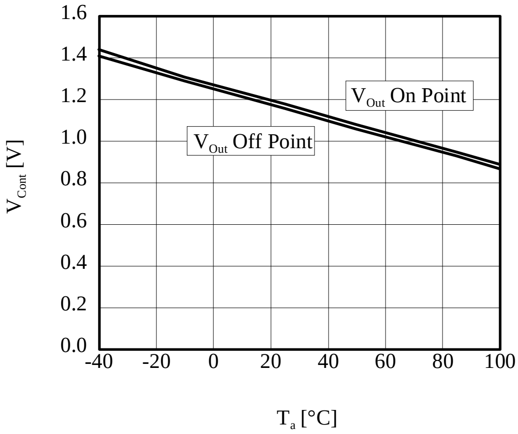
■ V_{Drop} vs T_a (AP1155ADL)



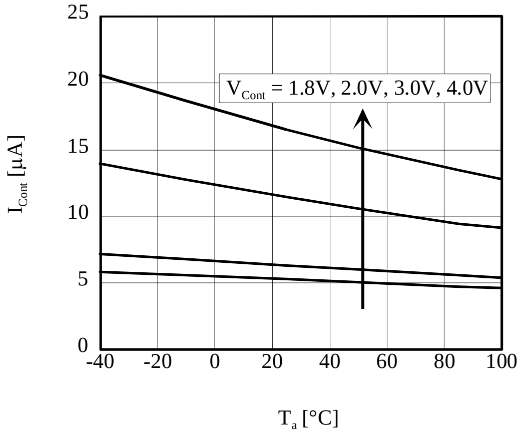
■ V_{Drop} vs T_a (AP1155ADL)



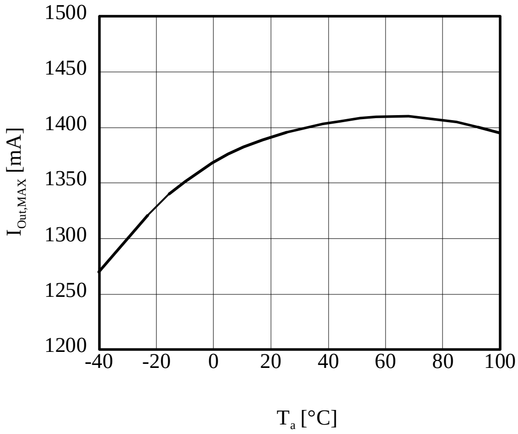
■ V_{Out} On/Off Point vs T_a (AP1155ADL)



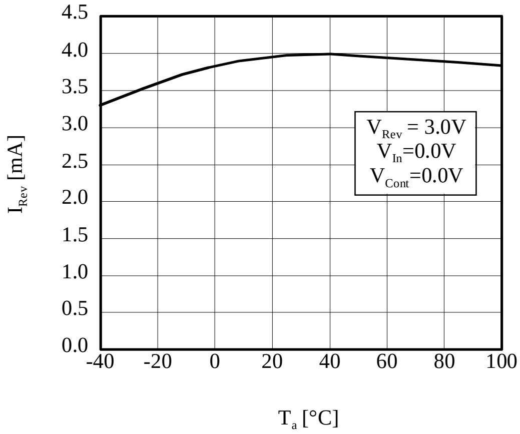
■ I_{Cont} vs T_a (AP1155ADL)



■ $I_{Out,MAX}$ vs T_a (AP1155ADL)

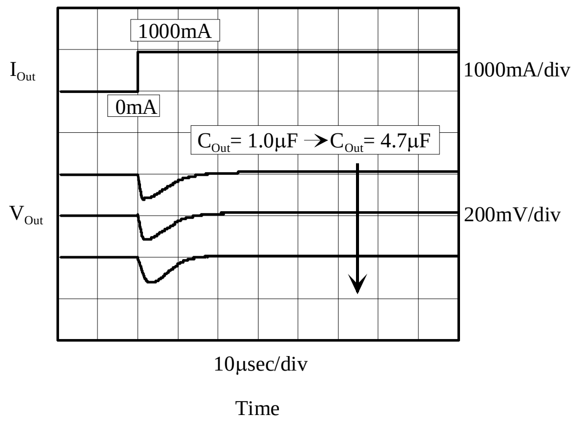


■ Reverse Bias Current(I_{Rev}) vs T_a (AP1155ADL)

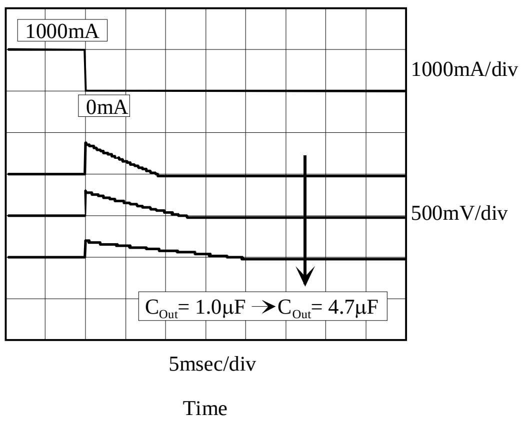


11.2 Load Transient

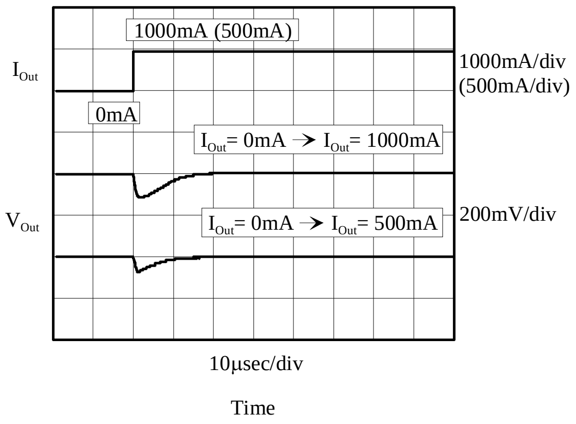
■ I_{Out}=0mA→1000mA, C_{Out}=1.0µF, 2.2µF, 4.7µF



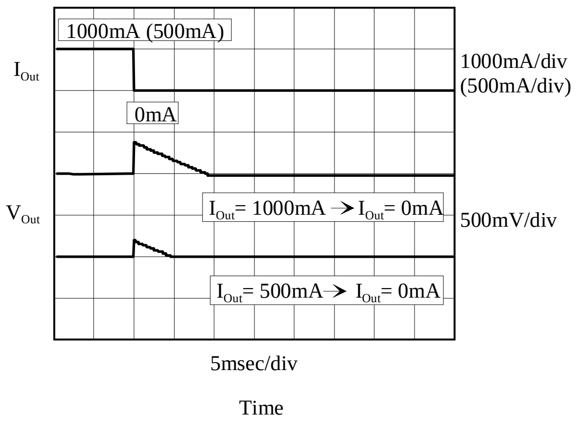
■ I_{Out}=1000mA→0mA, C_{Out}=1.0µF, 2.2µF, 4.7µF



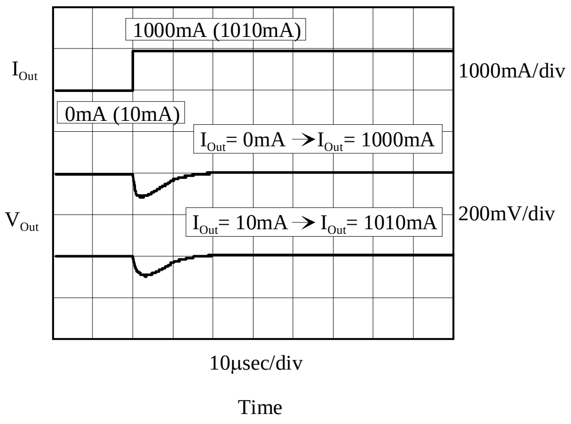
■ I_{Out}=0mA→500mA, 0mA→1000mA



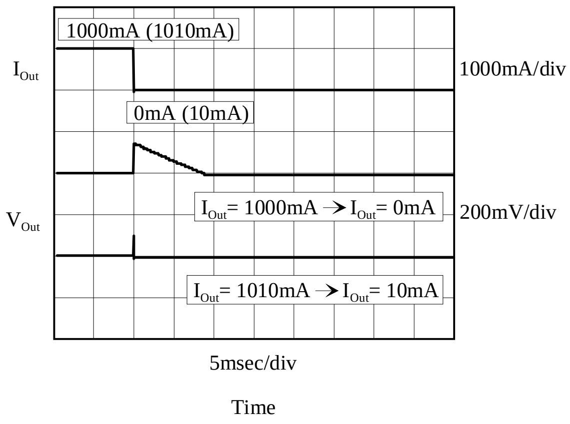
■ I_{Out}=500mA→0mA, 1000mA→0mA



■ I_{Out}=0mA→1000mA, 10mA→1010mA

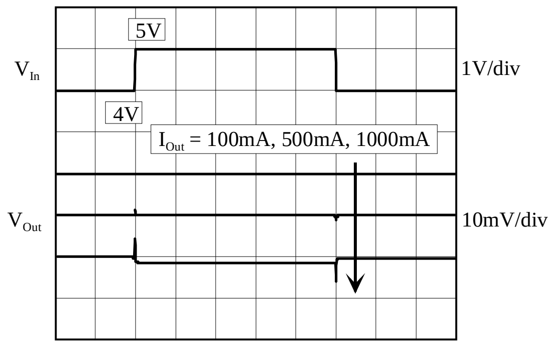


■ I_{Out}=1000mA→0mA, 1010mA→10mA



11.3 Line Transient

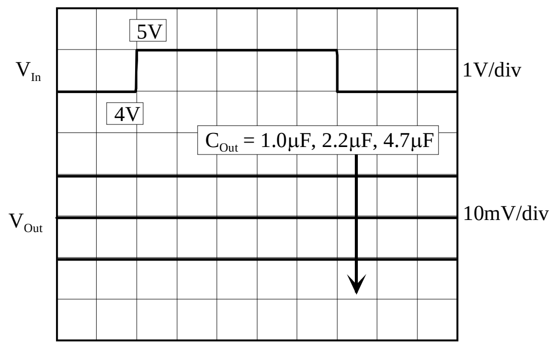
■ I_{Out}=100mA, 500mA, 1000mA



1msec/div

Time

■ C_{Out}=1.0μF, 2.2μF, 4.7μF



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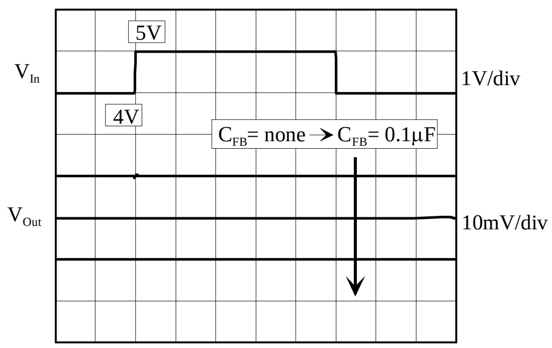
Time

■ C_{Fb}=none, 1000pF, 0.1μF

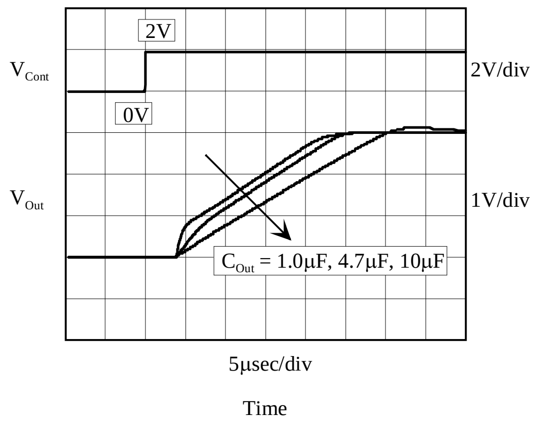


1msec/div

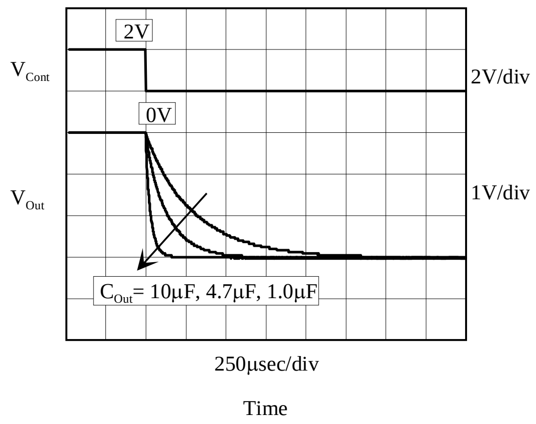
Time

11.4 On / Off Transient

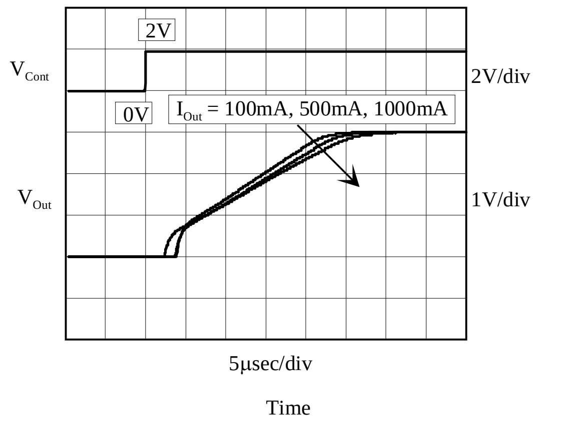
■ V_{Cont}=0.0V→2.0V, C_{Out}=1.0μF, 4.7μF, 10μF



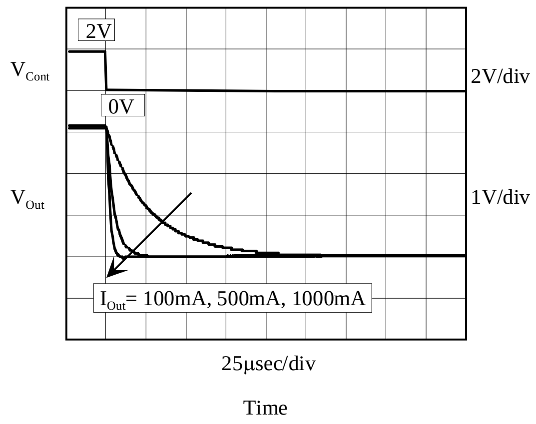
■ V_{Cont}=2.0V→0.0V, C_{Out}=1.0μF, 4.7μF, 10μF



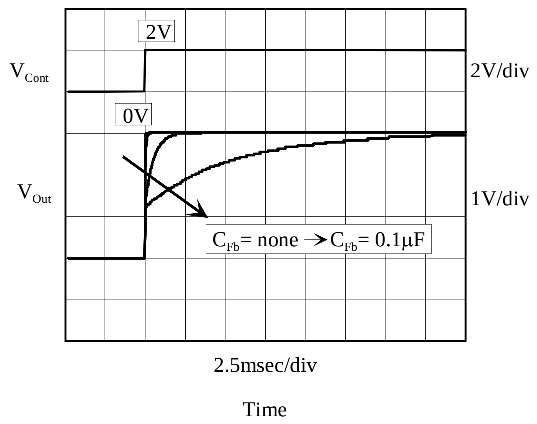
■ V_{Cont}=0.0V→2.0V, I_{Out}=100mA, 500mA, 1000mA



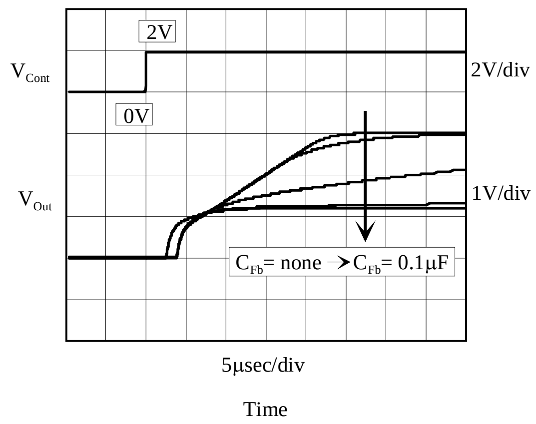
■ V_{Cont}=2.0V→0.0V, I_{Out}=100mA, 500mA, 1000mA



■ V_{Cont}=0.0V→2.0V, C_{Fb}=none~0.1μF*



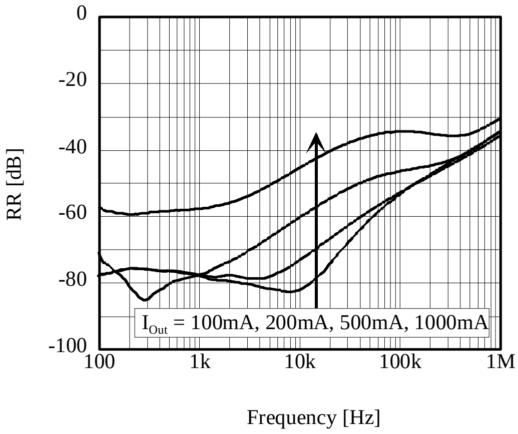
■ V_{Cont}=0.0V→2.0V, C_{Fb}=none~0.1μF*



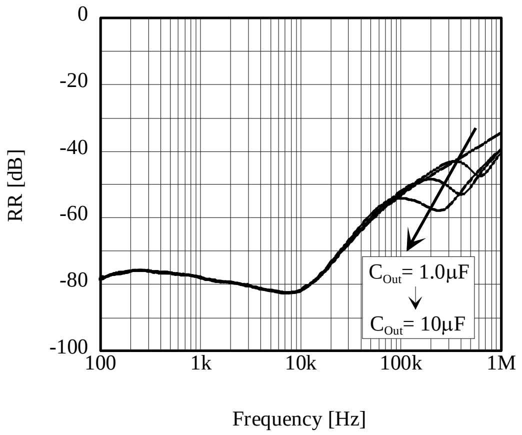
※ C_{Fb}=none, 100pF, 1000pF, 0.001μF, 0.01μF, 0.1μF

11.5 Ripple Rejection

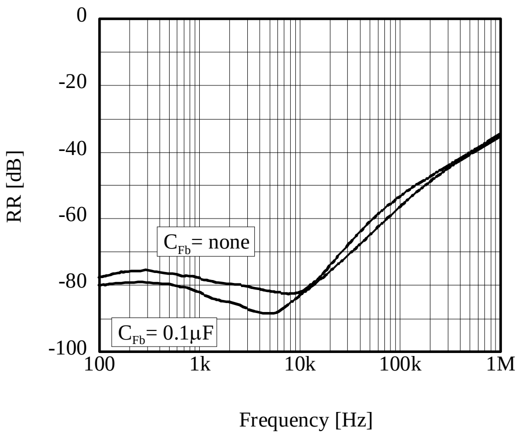
■ I_{Out}=100mA, 200mA, 500mA, 1000mA



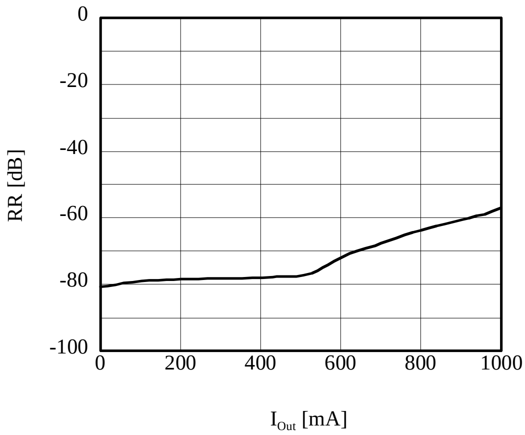
■ C_{Out}=1.0μF, 2.2μF, 4.7μF, 10μF



■ C_{Fb}=none, 0.1μF

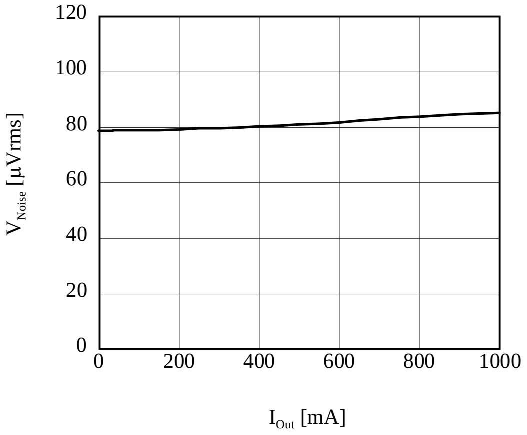


■ I_{Out}=1mA~1000mA, f=1kHz

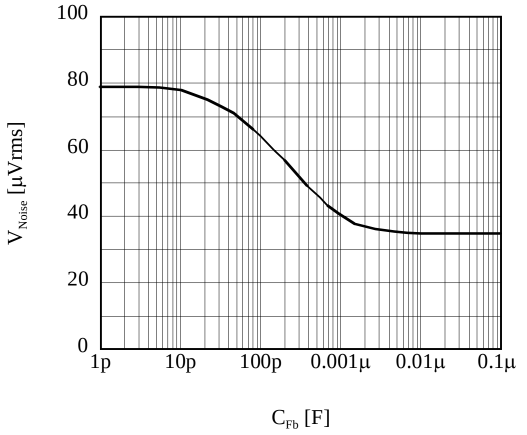


11.6 Output Noise

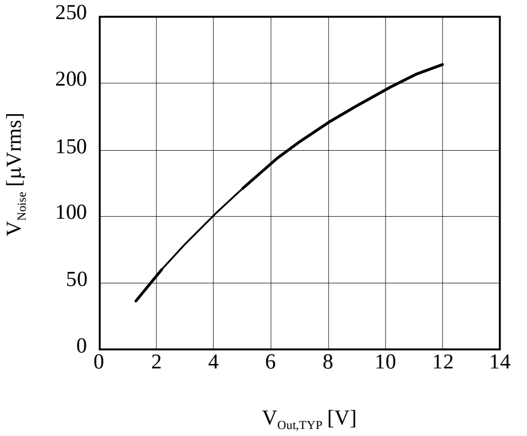
■ $V_{Out,TYP}$=3.0V, I_{Out}=0.1mA~1000mA



■ $V_{Out,TYP}$=3.0V, C_{Fb}=1pF~0.1μF



■ $V_{Out,TYP}$=1.3V ~ 12V



11.7 Stability

The standard capacitor recommended for use on the output side is a ceramic capacitor equal to or greater than 1.0μF. For operations at 2.4V or less, use at least a 2.2μF capacitor.

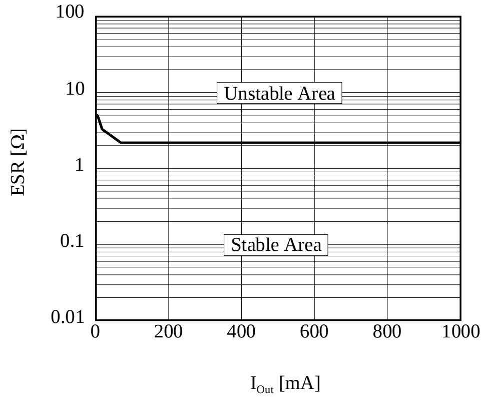


Figure 2. Stable operation area when $V_{Out,TYP}$=3.0V

The above graph indicates that operation is stable in the entire current range with a resistance of 1Ω or less (equivalent series resistance or 'ESR') connected in series to the output capacitor. Generally, the ESR of a ceramic capacitor is very low (several tens of mΩ), and no problems should arise in actual use. If an application requires use of a large ESR capacitor, connecting a ceramic capacitor with low ESR in parallel will enable operations at this level. When parallel output capacitors are used, be sure to position the ceramic capacitor as close to the IC as possible. The other capacitor connected in parallel may be located away from the IC. The IC will not be damaged by the increased capacitance. Input capacitors are necessary when the power supply impedance increases due to battery depletion or when the line to the power supply is particularly long. There is no general rule that can be used to determine the required number of capacitors used for such purposes. In some cases, only one capacitor is necessary for several regulator ICs. In some cases, one capacitor is required for each IC. To determine the required number of capacitors in a specific application, be sure to verify operation with all parts in the installed configuration.

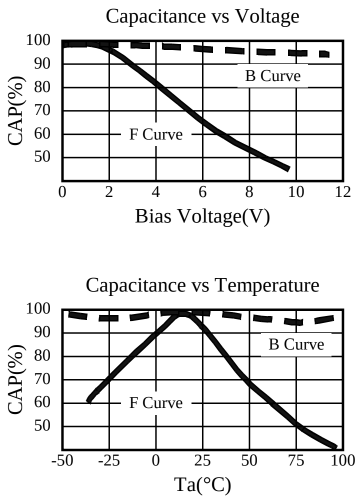


Figure 3. General characteristics of ceramic capacitors

Ceramic capacitors normally have specific temperature and voltage characteristics. Be sure to take the operating voltage and temperature into consideration when selecting parts for use. We recommend parts featuring B characteristics.

For evaluation

Kyocera : CM05B104K10AB , CM05B224K10AB ,CM105B104K16A ,CM105B224K16A ,CM21B225K10A

Murata : GRM36B104K10 , GRM42B104K10 ,GRM39B104K25 , GRM39B224K10 , GRM39B105K6.3

11.8 Operating Region and Power Dissipation

Power dissipation capability is limited by the junction temperature that triggers the built-in overheat protection circuit. Therefore, power dissipation capability is regarded as an internal limitation. The package itself does not offer high heat dissipation because of its small size. The package is, however, designed to release heat effectively when mounted on the PCB. Therefore, the heat-dissipation value will vary depending on the material, copper pattern, etc. of the PCB on which the package is mounted.
When the regulator loss is large (high ambient temperature, poor heat radiation), the overheat protection circuit is activated. When this occurs, output current cannot be obtained, and an output voltage drop is observed. When the junction temperature reaches the set value, the IC stops operating. However, after the IC has stopped operation and the junction temperature lowers sufficiently, the IC restarts operation immediately.

・How to determine the thermal resistance when installation on PCB

The chip junction temperature during operation is expressed by

$$T_j = \theta_{ja} \times P_D + 25$$

The junction temperature of the AP1155ADL is limited to approximately 140°C by the overheat protection circuit. P_D is the value observed when the overheat protection circuit is activated. The following example is based on an ambient temperature of 25°C.

$$140 = \theta_{ja} \times P_D + 25$$

$$\theta_{ja} \times P_D + 25 = 140$$

$$\theta_{ja} \times P_D = 115$$

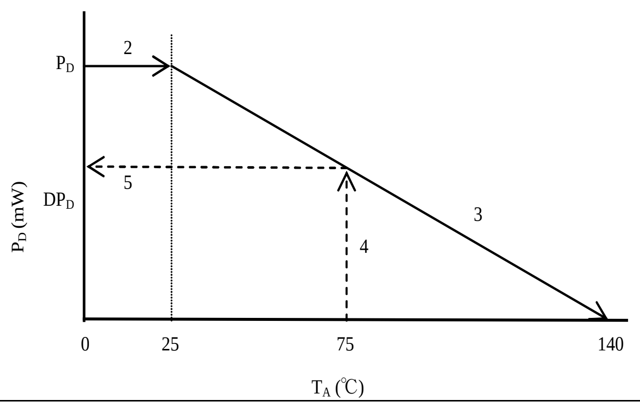
$$\theta_{ja} = \frac{115}{P_D}\ (°C/W)$$

Glass epoxy substrate with double-layer wiring
(x=30mm, y=30mm, t=1.0mm, copper pattern thickness: 35μm)
P_D is 2300mW. If the temperature exceeds 25°C, be sure to derate at -20mW/°C.

・P_D is easily calculated.

With the output terminal shorted-circuited to GND, gradually increase the input voltage and measure the input current. Slowly increase the input voltage to about 10V. The initial input current value becomes the maximum instantaneous output current value, but gradually lowers as the chip temperature rises, and ultimately reaches a state of thermal equilibrium (through natural air cooling). P_D is calculated using the input value for input current and the input voltage value in the equilibrium state.

$$P_D \cong V_{In} \times I_{In}$$



Procedure
(conducted at the time of installation on PCB)
1: Obtain P_D ($V_{In} \times I_{In}$ when output is short-circuited).
2: Plot P_D on the 25°C line.
3: Draw a straight line between P_D and the 140°C line.
4: Extend a straight-line perpendicular from the point of the designed maximum operating temperature (for example, 75°C).
5: Extend a line to the left from the intersection of the derating curve and the line drawn in 4, and read the P_D value (this value is DP_D).
6: $DP_D \div (V_{In,MAX} \times V_{Out}) = I_{Out}$ at 75°C

The maximum operating current at the maximum temperature is as follows:

$$I_{Out} \cong \{DP_D \div (V_{In,MAX} - V_{Out})\}$$

Try to achieve maximum heat dissipation in your design in order to minimize the part's temperature during operation. Generally speaking, lower part temperatures result in higher reliability in operation.

12. Definition of term

■ Characteristics

・Output Voltage (V_{Out})

The output voltage is specified with $V_{In}=V_{Out,TYP}+1V$ and $I_{Out}=5mA$.

・Output Current (I_{Out})

Output current, which can be used continuously (It is the range where overheating protection of the IC does not operate).

・Maximum output current ($I_{Out,Max}$)

The rated output current is specified under the condition where the output voltage drops 0.9V times the value specified with $I_{Out}=5mA$ by increasing the output current. The input voltage is set to $V_{OutTYP}+1V$ and the current is pulsed to minimize temperature effect.

・Dropout Voltage (V_{Drop})

It is the difference between the input voltage and the output voltage when the circuit stops the stable operation by decreasing the input voltage. It is measured when the output voltage drops 100mV from its nominal value by decreasing the input voltage gradually.

・Line Regulation (LinReg)

It is the fluctuations of the output voltage value when the input voltage is changed.

・Load Regulation (LoaReg)

It is the fluctuations of the output voltage value when the input voltage is assumed to be $V_{Out,TYP}+1V$, and the output current is changed.

・Ripple Rejection (RR)

Ripple rejection is the ability of the regulator to attenuate the ripple content of the input voltage at the output. It is measured with the condition of $V_{In}=V_{Out,TYP}+1.5V$. Ripple rejection is the ratio of the ripple content between the output vs. input and is expressed in dB

・Standby Current ($I_{Standby}$)

Standby current is the current which flows into the regulator when the output is turned off by the control function ($V_{Cont}=0V$).

■ Protections

・Over Current Protection

It is an function to protect the IC by limiting the output current when excessive current flows to IC, such as the output is connected to GND, ets.

・Thermal Protection

It protects the IC not to exceed the permissible power consumption of the package in case of large power loss inside the regulator. The output is turned off when the chip reaches around 140°C, but it turns on again when the temperature of the chip decreases.

・ESD

MM: 200pF 0Ω 200V or over

HBM: 100pF 1.5kΩ 2000V or over

13. Recommended External Circuits

■$V_{Out,TYP}$=3.0V: Example of selection of external components.

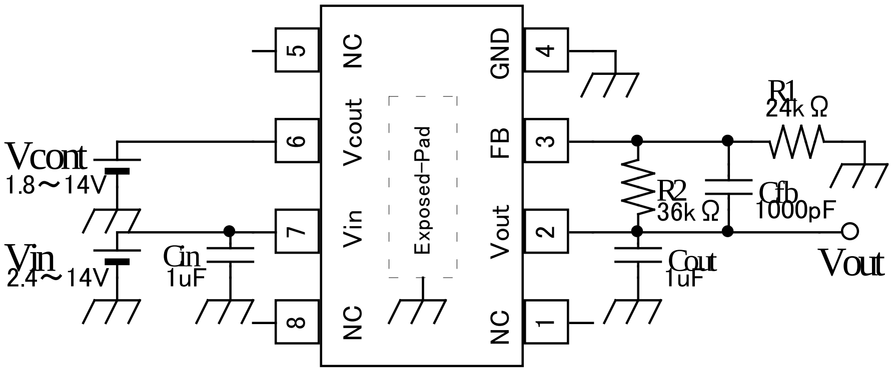


Figure 4. External Circuit

The output voltage value $V_{Out,TYP}$ is determined using the following equation:

$$V_{Out,TYP} = \frac{R_1 + R_2}{R_1} \times V_{FB}(1.21V)$$

The minimum required current through resistance R_1, R_2 is 30μA, which is determined by $\frac{V_{FB}}{R_1}$.

Only a ceramic capacitor should be used for C_{Out}. For C_{In} any type of capacitor may be selected. For C_{Out} and C_{In}, use capacitors rated at 1μF or higher. For details, refer to 11.7 Stability.

The Fb terminal has high impedance and is therefore susceptible to external noise, etc. Connecting capacitor C_{Fb} between the V_{Out} terminal and the Fb terminal minimizes the effects of external noise and also reduces output noise.

■Recommended Layout

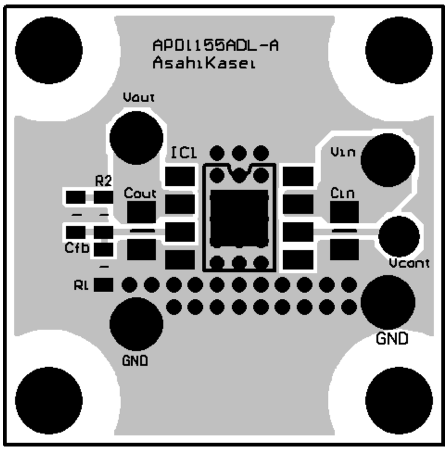
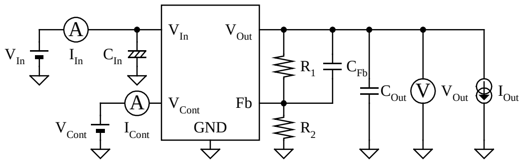


Figure 5. Recommended Layout

① Cin should be located as close as possible to V_{in} pin and GND.
② Cout should be located as close as possible to V_{OUT} pin and GND.
③ Feedback resistor R1, R2 should be placed as close as possible to the FB terminal.
When connecting Vout and R2, please wiring from "+" terminal of Cout.
④ Cfb should be located as close as possible to V_{OUT} pin and FB pin.
⑤ GND plane should be large as much as possible.
⑥ Exposed Pad is the ground and sharing of the IC.
Exposed Pad must be connected to GND.
⑦ Via hall is effective to heat dissipation to each layer of PCB.

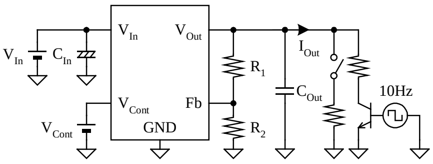
■Test Circuit

■ Test circuit for DC characteristics



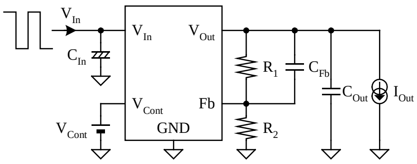
$V_{Out,TYP}$=3.0V(R_1=53kΩ, R_2=36kΩ)
V_{In}=4.0V, V_{Cont}=1.8V, I_{Out}=5mA
C_{In}=1.0μF(Tantalum), C_{Fb}=0.001μF(Ceramic),
C_{Out}=1.0μF(Ceramic), T_a=25°C

■ Test circuit for Load Transient



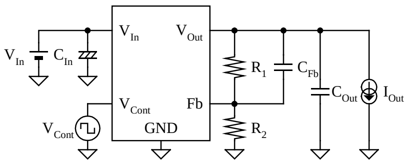
$V_{Out,TYP}$=3.0V(R_1=53kΩ, R_2=36kΩ)
V_{In}=4.0V, V_{Cont}=1.8V
C_{In}=1.0μF(Tantalum), T_a=25°C

■ Test circuit for Line Transient



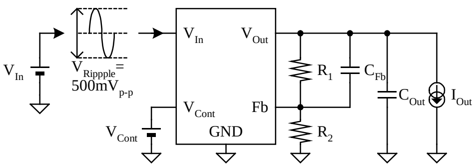
$V_{Out,TYP}$=3.0V(R_1=53kΩ, R_2=36kΩ)
V_{In}=4.0V↔5.0V(100Hz), V_{Cont}=1.8V, I_{Out}=100mA
C_{In}=1.0μF(Tantalum), C_{Fb}=none, T_a=25°C

■ Test circuit for On/Off Transient



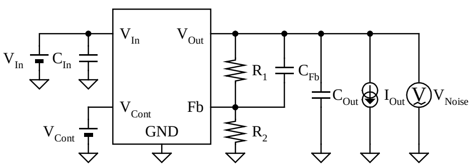
$V_{Out,TYP}$=3.0V(R_1=53kΩ, R_2=36kΩ)
V_{In}=4.0V, V_{Cont}=0.0V↔2.0V(10Hz), I_{Out}=100mA
C_{In}=1.0μF(Tantalum), C_{Fb}=none, T_a=25°C

■ Test circuit for Ripple Rejection



$V_{Out,TYP}$=3.0V(R_1=53kΩ, R_2=36kΩ)
V_{In}=4.5V, V_{Cont}=2.0V, V_{Ripple}=500mV_{p-p}, I_{Out}=100mA
C_{In}=none, C_{Fb}=none, T_a=25°C

■ Test circuit for Output Noise

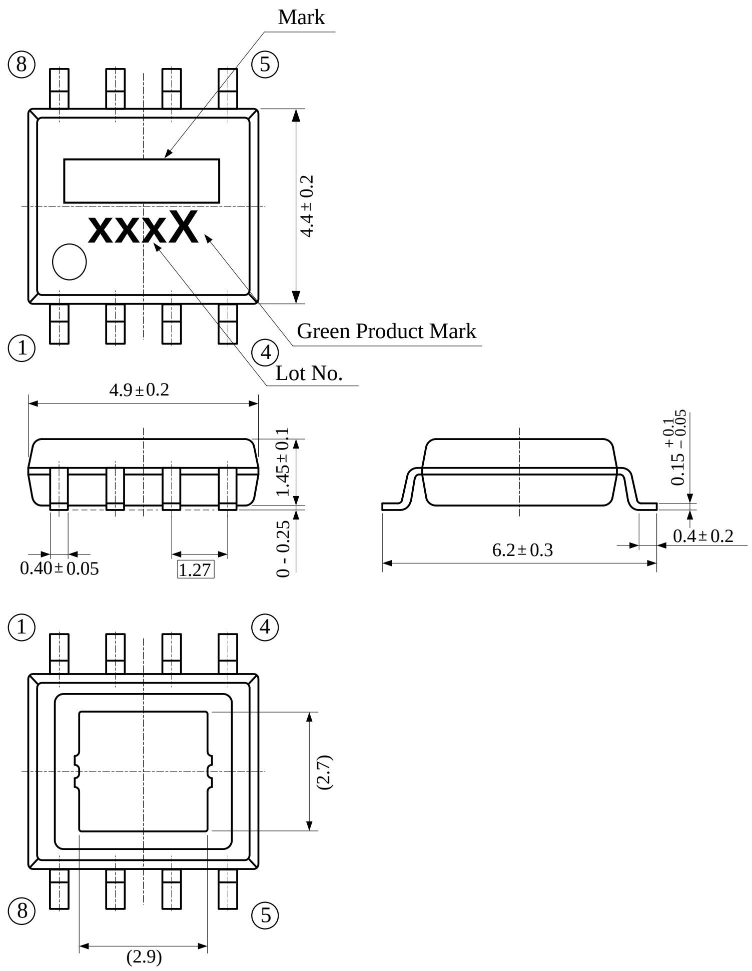


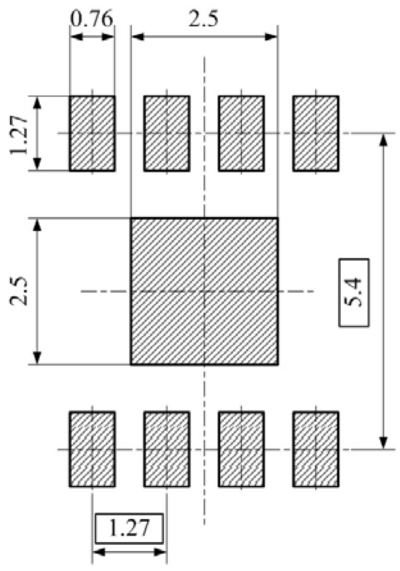
R_2=36kΩ
V_{In}=$V_{Out,TYP}$+1.0V, V_{Cont}=2.0V, I_{Out}=100mA
BPF=400Hz~80kHz
C_{In}=C_{Out}=1.0μF(Ceramic), C_{Fb}=none, T_a=25°C

14. Package

■ Outline Dimensions

(Unit:mm)





Mount Pad of Current Part

15. Revise History

Date (YY/MM/DD)	Revision	Page	Contents
15/12/25	00	-	First Edition
16/01/19	01	1	Added a Recommend Circuit to “2.Features”.
		1	Fixed “3.Applications”.
		19	Added a Recommend Layout to “13. Recommended External Circuits”.

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