TDA8932

Class-D audio amplifier

Rev. 02 — 12 December 2006 Preliminary data sheet

1. General description

The TDA8932 is a high efficiency class-D amplifier with low power dissipation.

The typical output power is 2×15 W in stereo half-bridge application ($R_L = 4\ \Omega$) or 1×30 W typical in full-bridge application ($R_L = 8\ \Omega$). Due to the low power dissipation the device can be used without any external heat sink when playing music. If proper cooling via the printed-circuit board is implemented, a continuous output power of 2×15 W is feasible. Due to the implementation of thermal foldback, even for high supply voltages and/or lower load impedances, the device remains operating with considerable music output power without the need for an external heat sink.

The device has two full-differential inputs driving two independent outputs. It can be used as mono full-bridge configuration (BTL) or as stereo half-bridge configuration (SE).

2. Features

- Operating voltage from 10 V to 36 V asymmetrical or ±5 V to ±18 V symmetrical
- Mono-bridged tied load (full-bridge) or stereo single-ended (half-bridge) application
- Application without heatsink using thermally enhanced small outline package
- High efficiency and low-power dissipation
- Thermally protected and thermal foldback
- Current limiting to avoid audio holes
- Full short-circuit proof across load and to supply lines (using advanced current protection)
- Switchable internal or external oscillator (master-slave setting)
- No pop noise
- Full-differential inputs

3. Applications

- Flat panel television sets
- Flat panel monitor sets
- Multimedia systems
- Wireless speakers
- Mini and micro systems
- Home sound sets

4. Quick reference data

Table 1. Quick reference data

V_P = 22 V; f_{osc} = 320 kHz; T_{amb} = 25 °C; unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Supplies						
V_P	supply voltage	asymmetrical supply	10	22	36	V
I_P	supply current	Sleep mode; no load	-	0.6	1	mA
$I_{q(tot)}$	total quiescent current	Operating mode; no load, no snubbers and no filter connected	-	40	80	mA
Stereo SE channel; R_S < 0.1 Ω [1][2]						
$P_{o(RMS)}$	RMS output power	continuous time output power per channel; THD+N = 10 %; f_i = 1 kHz				
		R_L = 4 Ω; V_P = 22 V	14	15	-	W
		R_L = 8 Ω; V_P = 30 V	14	15	-	W
		short time output power per channel; THD+N = 10 %; f_i = 1 kHz				
		R_L = 4 Ω; V_P = 29 V	23	25	-	W
Mono BTL; R_S < 0.1 Ω [1][2]						
$P_{o(RMS)}$	RMS output power	continuous time output power; THD+N = 10 %; f_i = 1 kHz				
		R_L = 4 Ω; V_P = 12 V	14	15	-	W
		R_L = 8 Ω; V_P = 22 V	28	30	-	W
		short time output power; THD+N = 10 %; f_i = 1 kHz				
		R_L = 8 Ω; V_P = 29 V	47	50	-	W

[1] Output power is measured indirectly; based on R_{DSon} measurement.

[2] R_S is the series resistance of inductor of low-pass LC filter in the application.

5. Ordering information

Table 2. Ordering information

Type number	Package		
	Name	Description	Version
TDA8932T	SO32	plastic small outline package; 32 leads; body width 7.5 mm	SOT287-1

6. Block diagram

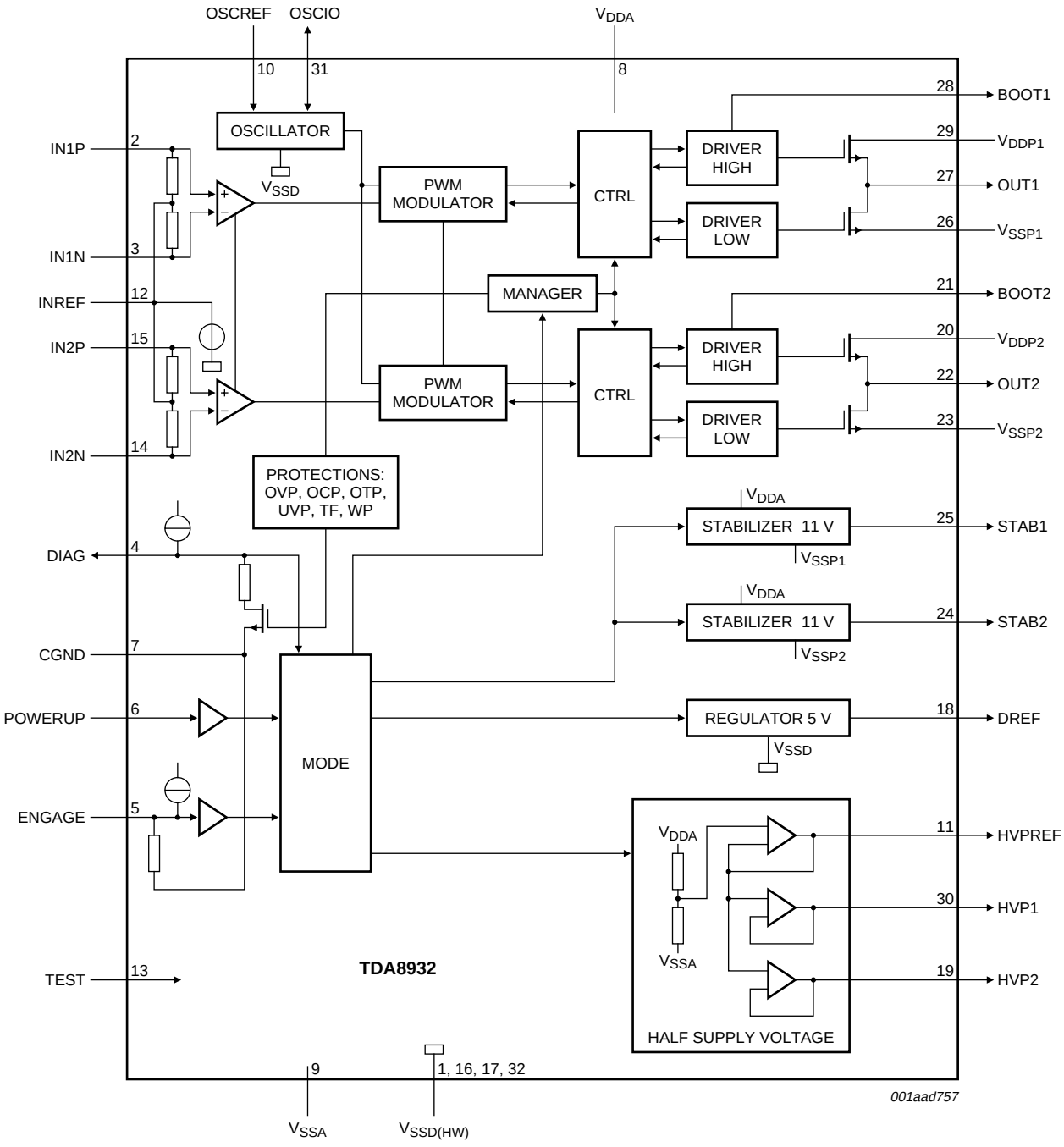


Fig 1. Block diagram

7. Pinning information

7.1 Pinning

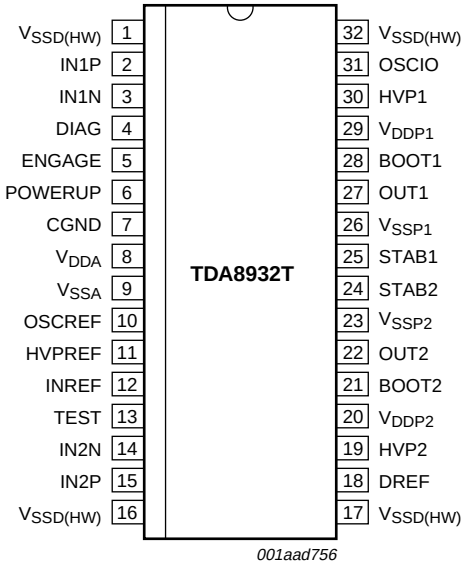


Fig 2. Pin configuration SO32

7.2 Pin description

Table 3. Pin description

Symbol	Pin	Description
$V_{SSD(HW)}$	1	negative digital supply voltage and handle wafer connection
IN1P	2	positive audio input for channel 1
IN1N	3	negative audio input for channel 1
DIAG	4	diagnostic output; open-drain
ENGAGE	5	engage input to switch between Mute mode and Operating mode
POWERUP	6	power-up input to switch between Sleep mode and Mute mode
CGND	7	control ground; reference for POWERUP, ENGAGE and DIAG
V_{DDA}	8	positive analog supply voltage
V_{SSA}	9	negative analog supply voltage
OSCREF	10	input internal oscillator setting (only master setting)
HVPREF	11	decoupling of internal half supply voltage reference
INREF	12	decoupling for input reference voltage
TEST	13	test signal input; for testing purpose only
IN2N	14	negative audio input for channel 2
IN2P	15	positive audio input for channel 2
$V_{SSD(HW)}$	16	negative digital supply voltage and handle wafer connection
$V_{SSD(HW)}$	17	negative digital supply voltage and handle wafer connection
DREF	18	decoupling of internal (reference) 5 V regulator for logic supply

Table 3. Pin description *…continued*

Symbol	Pin	Description
HVP2	19	half supply output voltage 2 for charging single-ended capacitor for channel 2
V_{DDP2}	20	positive power supply voltage for channel 2
BOOT2	21	bootstrap high-side driver channel 2
OUT2	22	PWM output channel 2
V_{SSP2}	23	negative power supply voltage for channel 2
STAB2	24	decoupling of internal 11 V regulator for channel 2 drivers
STAB1	25	decoupling of internal 11 V regulator for channel 1 drivers
V_{SSP1}	26	negative power supply voltage for channel 1
OUT1	27	PWM output channel 1
BOOT1	28	bootstrap high-side driver channel 1
V_{DDP1}	29	positive power supply voltage for channel 1
HVP1	30	half supply output voltage 1 for charging single-ended capacitor for channel 1
OSCIO	31	oscillator input in slave configuration or oscillator output in master configuration
$V_{SSD(HW)}$	32	negative digital supply voltage and handle wafer connection

8. Functional description

8.1 General

The TDA8932 is a mono full-bridge or stereo half-bridge audio power amplifier using class-D technology. The audio input signal is converted into a Pulse Width Modulated (PWM) signal via an analog input stage and PWM modulator. To enable the output power Diffusion Metal Oxide Semiconductor (DMOS) transistors to be driven, this digital PWM signal is applied to a control and handshake block and driver circuits for both the high side and low side. A 2nd-order low-pass filter converts the PWM signal to an analog audio signal across the loudspeakers.

The TDA8932 contains two independent half-bridges with full differential input stages. The loudspeakers can be connected in the following configurations:

- Mono full-bridge: Bridge Tied Load (BTL)
- Stereo half-bridge: Single-Ended (SE)

The TDA8932 contains common circuits to both channels such as the oscillator, all reference sources, the mode functionality and a digital timing manager. The following protections are built-in: thermal foldback, temperature, current and voltage protections.

8.2 Mode selection and interfacing

The TDA8932 can be switched in three operating modes using pins POWERUP and ENGAGE:

- Sleep mode: with low supply current.
- Mute mode: the amplifiers are switching idle (50 % duty cycle), but the audio signal at the output is suppressed by disabling the VI-converter input stages. The capacitors on pins HVP1 and HVP2 have been charged to half the supply voltage (asymmetrical supply only).
- Operating mode: the amplifiers are fully operational with output signal.
- Fault mode.

Both pins POWERUP and ENGAGE refer to pin CGND.

Table 4 shows the different modes as a function of the voltages on the POWERUP and ENGAGE pins.

Table 4. Mode selection

Mode	Pin		
	POWERUP	ENGAGE	DIAG
Sleep	< 0.8 V	< 0.8 V	don't care
Mute	2 V to 6.0 V[1]	< 0.8 V[1]	> 2 V
Operating	2 V to 6.0 V[1]	3 V to 6.0 V[1]	> 2 V
Fault	2 V to 6.0 V[1]	don't care	< 0.8 V

[1] In case of symmetrical supply conditions the voltage applied to pins POWERUP and ENGAGE must never exceed the supply voltage (V_{DDA}, V_{DDP1} or V_{DDP2}).

If the transition between Mute mode and Operating mode is controlled via a time constant, the start-up will be pop free since the DC output offset voltage is applied gradually to the output between Mute mode and Operating mode. The bias current setting of the VI-converters is related to the voltage on pin ENGAGE:

- Mute mode: the bias current setting of the VI-converters is zero (VI-converters disabled)
- Operating mode: the bias current is at maximum

The time constant required to apply the DC output offset voltage gradually between Mute mode and Operating mode can be generated by applying a decoupling capacitor on pin ENGAGE. The value of the capacitor on pin ENGAGE should be 470 nF.

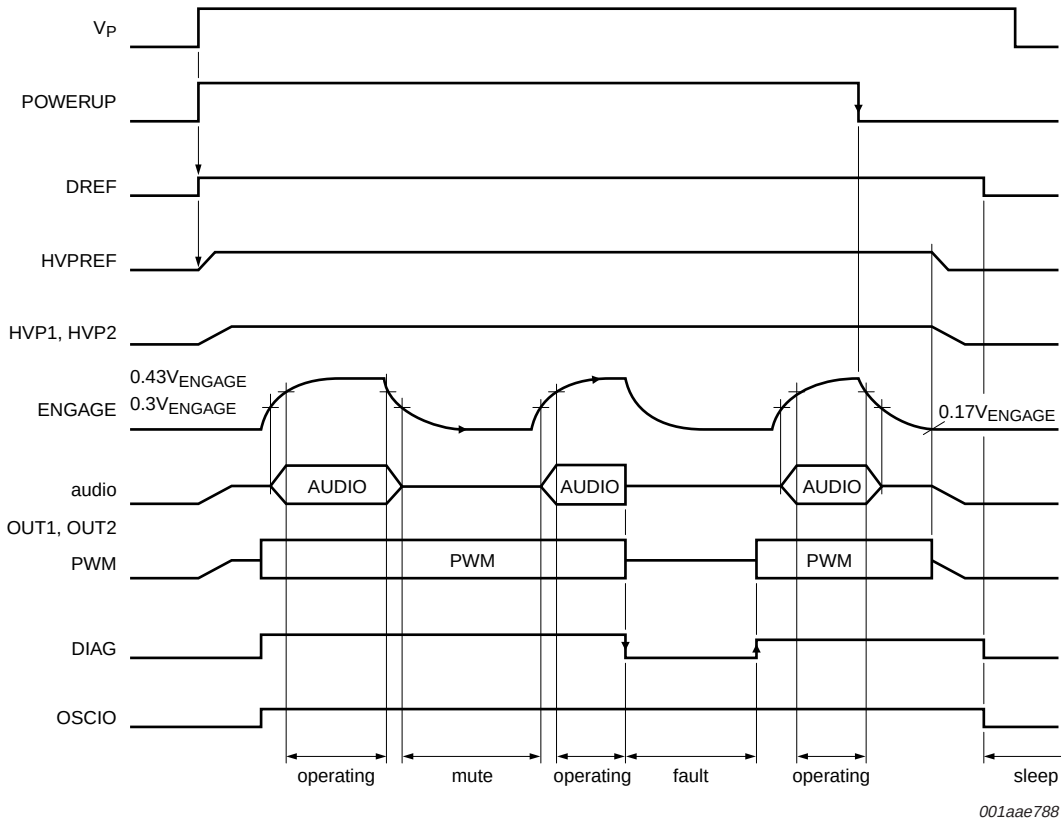


Fig 3. Start-up sequence

8.3 Pulse width modulation frequency

The output signal of the amplifier is a PWM signal with a carrier frequency of approximately 320 kHz. Using a 2nd-order low-pass filter in the application results in an analog audio signal across the loudspeaker. The PWM switching frequency can be set by an external resistor R_{osc} connected between pins OSCREF and $V_{SSD(HW)}$. The carrier frequency can be set between 300 kHz and 500 kHz. Using an external resistor of 39 kΩ, the carrier frequency is set to an optimized value of 320 kHz (see Figure 4).

If two or more TDA8932 devices are used in the same audio application, it is recommended to synchronize the switching frequency of all devices. This can be realized by connecting all pins OSCIO together and configure one of the TDA8932 in the application as clock master, while the other TDA8932 devices are configured in slave mode.

Pin OSCIO is a 3-state input or output buffer. Pin OSCIO is configured in master mode as oscillator output and in slave mode as oscillator input. Master mode is enabled by applying a resistor while slave mode is entered by connecting pin OSCREF directly to pin $V_{SSD(HW)}$ (without any resistor).

The value of the resistor also sets the frequency of the carrier which can be estimated by the following formula:

$$f_{osc} = \frac{12.45 \times 10^9}{R_{osc}} \quad (1)$$

Where:

f_{osc} = oscillator frequency

R_{osc} = oscillator resistor (on pin OSCREF)

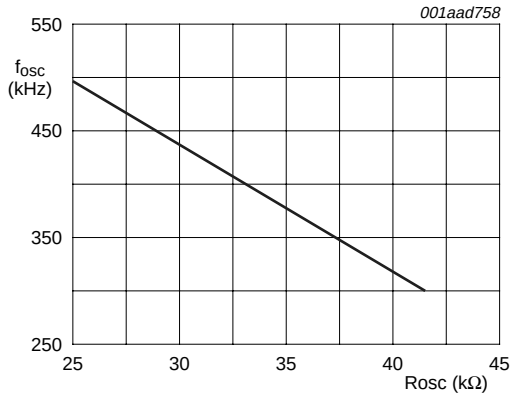


Fig 4. Oscillation frequency as a function of resistor R_{osc}

Table 5 summarizes how to configure the TDA8932 in master or slave configuration.

For device synchronization see Section 14.6 “Device synchronization”.

Table 5. Master or slave configuration

Configuration	Pin	
	OSCREF	OSCIO
Master	R_{osc} > 25 kΩ to $V_{SSD(HW)}$	output
Slave	R_{osc} = 0 Ω; shorted to $V_{SSD(HW)}$	input

8.4 Protection

The following protection is included in the TDA8932:

- Thermal Foldback (TF)
- OverTemperature Protection (OTP)
- OverCurrent Protection (OCP)
- Window Protection (WP)
- Supply voltage protection:
  - UnderVoltage Protection (UVP)
  - OverVoltage Protection (OVP)
  - UnBalance Protection (UBP)
- ESD

The reaction of the device to the different fault conditions differs per protection.

8.4.1 Thermal Foldback (TF)

If the junction temperature of the TDA8932 exceeds the threshold level (T_j > 140 °C) the gain of the amplifier is decreased gradually to a level where the combination of dissipation (P) and the thermal resistance from junction to ambient [$R_{th(j-a)}$] results in a junction temperature around the threshold level.

This means that the device will not completely switch off, but remains operational at lower output power levels. Especially with music output signals this feature enables high peak output power while still operating without any external heat sink other than the printed-circuit board area.

If the junction temperature still increases due to external causes, the OTP shuts down the amplifier completely.

8.4.2 OverTemperature Protection (OTP)

If the junction temperature T_j > 155 °C, then the power stage will shut down immediately.

8.4.3 OverCurrent Protection (OCP)

When the loudspeaker terminals are short-circuited or if one of the demodulated outputs of the amplifier is short-circuited to one of the supply lines, this will be detected by the OCP.

If the output current exceeds the maximum output current ($I_{O(ocp)}$ > 4 A), this current will be limited by the amplifier to 4 A while the amplifier outputs remain switching (the amplifier is not shut down completely). This is called current limiting.

The amplifier can distinguish between an impedance drop of the loudspeaker and a low-ohmic short-circuit across the load or to one of the supply lines. This impedance threshold depends on the supply voltage used:

- In case of a short-circuit across the load, the audio amplifier is switched off completely and after approximately 100 ms it will try to restart again. If the short-circuit condition is still present after this time, this cycle will be repeated. The average dissipation will be low because of this low duty cycle.

- In case of a short to one of the supply lines, this will trigger the OCP and the amplifier will be shut down. During restart the window protection will be activated. As a result the amplifier will not start until 100 ms after the short to the supply lines is removed.
- In case of impedance drop (e.g. due to dynamic behavior of the loudspeaker) the same protection will be activated. The maximum output current is again limited to 4 A, but the amplifier will not switch off completely (thus preventing audio holes from occurring). The result will be a clipping output signal without any artifacts.

8.4.4 Window Protection (WP)

The WP checks the PWM output voltage before switching from Sleep mode to Mute mode (outputs switching) and is activated:

- During the start-up sequence, when pin POWERUP is switched from Sleep mode to Mute mode. In the event of a short-circuit at one of the output terminals to V_{DDP1}, V_{SSP1}, V_{DDP2} or V_{SSP2} the start-up procedure is interrupted and the TDA8932 waits for open-circuit outputs. Because the check is done before enabling the power stages, no large currents will flow in the event of a short-circuit.
- When the amplifier is completely shut down due to activation of the OCP because a short-circuit to one of the supply lines is made, then during restart (after 100 ms) the window protection will be activated. As a result the amplifier will not start until the short-circuit to the supply lines is removed.

8.4.5 Supply voltage protection

If the supply voltage drops below 10 V, the UnderVoltage Protection (UVP) circuit is activated and the system will shut down directly. This switch-off will be silent and without pop noise. When the supply voltage rises above the threshold level, the system is restarted again after 100 ms.

If the supply voltage exceeds 36 V the OverVoltage Protection (OVP) circuit is activated and the power stages will shut down. It is re-enabled as soon as the supply voltage drops below the threshold level. The system is restarted again after 100 ms.

It should be noted that supply voltages > 40 V may damage the TDA8932. Two conditions should be distinguished:

1. If the supply voltage is pumped to higher values by the TDA8932 application itself (see also Section 14.3), the OVP is triggered and the TDA8932 is shut down. The supply voltage will decrease and the TDA8932 is protected against any overstress.
2. If a supply voltage > 40 V is caused by other or external causes, then the TDA8932 will shut down, but the device can still be damaged since the supply voltage will remain > 40 V in this case. The OVP protection is not a supply voltage clamp.

An additional UnBalance Protection (UBP) circuit compares the positive analog supply voltage (V_{DDA}) and the negative analog supply voltage (V_{SSA}) and is triggered if the voltage difference between them exceeds a certain level. This level depends on the sum of both supply voltages. The unbalance threshold levels can be defined as follows:

- LOW-level threshold: $V_{P(th)(ubp)l} < {}^{8}\!/_{5} \times V_{HVPREF}$
- HIGH-level threshold: $V_{P(th)(ubp)h} > {}^{8}\!/_{3} \times V_{HVPREF}$

In a symmetrical supply the UBP is released when the unbalance of the supply voltage is within 6 % of its starting value.

Table 6 shows an overview of all protection and the effect on the output signal.

Table 6. Protection overview

Protection	Restart	
	When fault is removed	Every 100 ms
OTP	no	yes
OCP	yes	no
WP	yes	no
UVP	no	yes
OVP	no	yes
UBP	no	yes

8.5 Diagnostic input and output

Whenever a protection is triggered, except for TF, pin DIAG is activated to LOW level (see Table 6). An internal reference supply will pull-up the open-drain DIAG output to approximately 2.4 V. This internal reference supply can deliver approximately 50 μA. Pin DIAG refers to pin CGND. The diagnostic output signal during different short conditions is illustrated in Figure 5. Using pin DIAG as input, a voltage < 0.8 V will put the device into Fault mode.

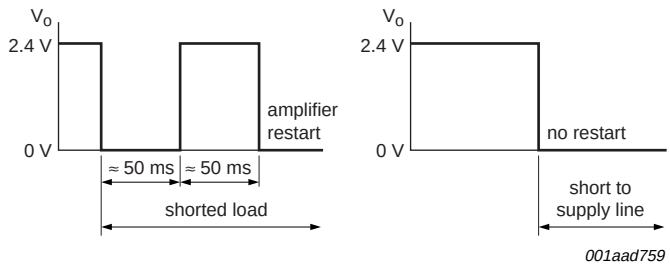


Fig 5. Diagnostic output for different short-circuit conditions

8.6 Differential inputs

For a high common-mode rejection ratio and a maximum of flexibility in the application, the audio inputs are fully differential. By connecting the inputs anti-parallel, the phase of one of the two channels can be inverted, so that the amplifier can operate as a mono BTL amplifier. The input configuration for a mono BTL application is illustrated in Figure 6.

In SE configuration it is also recommended to connect the two differential inputs in anti-phase. This has advantages for the current handling of the power supply at low signal frequencies and minimizes supply pumping (see also Section 14.8).

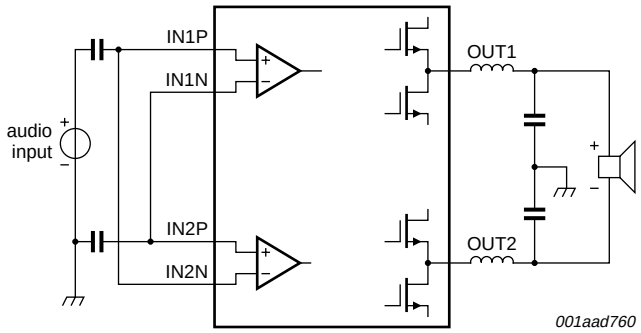


Fig 6. Input configuration for mono BTL application

8.7 Output voltage buffers

When pin POWERUP is set HIGH, the half supply output voltage buffers are switched on in asymmetrical supply configuration. The start-up will be pop free since the device starts switching when the capacitor on pin HVPREF and the SE capacitors are completely charged.

Output voltage buffers:

- Pins HVP1 and HVP2: The time required for charging the SE capacitor depends on its value. The half supply voltage output is disabled when the TDA8932 is used in a symmetrical supply application.
- Pin HVPREF: This output voltage reference buffer charges the capacitor on pin HVPREF.
- Pin INREF: This output voltage reference buffer charges the input reference capacitor on pin INREF. Pin INREF applies the bias voltage for the inputs.

9. Internal circuitry

Table 7. Internal circuitry

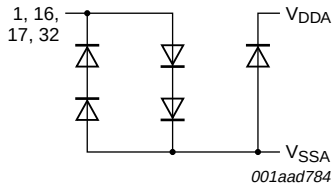
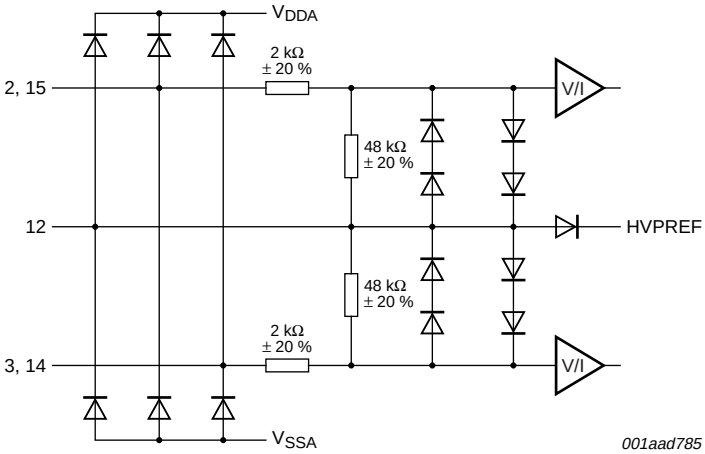
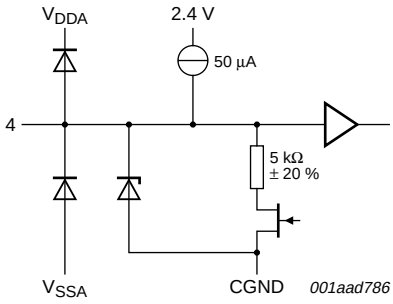
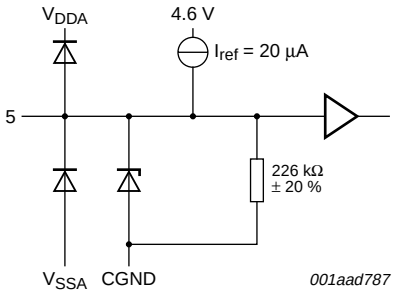
Pin	Symbol	Equivalent circuit
1	$V_{SSD(HW)}$	
16	$V_{SSD(HW)}$	
17	$V_{SSD(HW)}$	
32	$V_{SSD(HW)}$	
2	IN1P	
3	IN1N	
12	INREF	
14	IN2N	
15	IN2P	
4	DIAG	
5	ENGAGE	

Table 7. Internal circuitry *...continued*

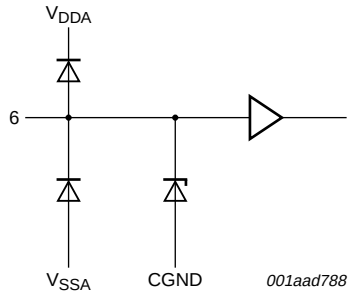
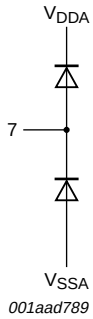
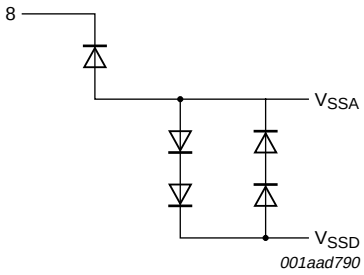
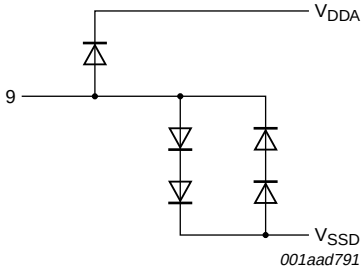
Pin	Symbol	Equivalent circuit
6	POWERUP	
7	CGND	
8	V_{DDA}	
9	V_{SSA}	

Table 7. Internal circuitry *...continued*

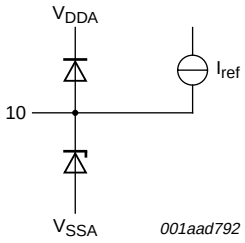
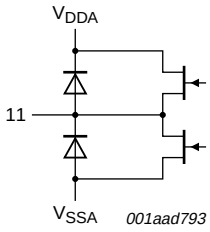
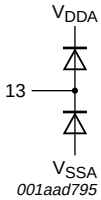
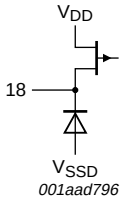
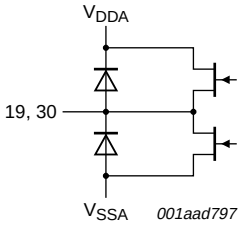
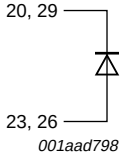
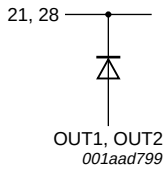
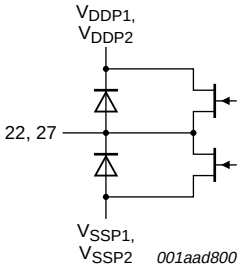
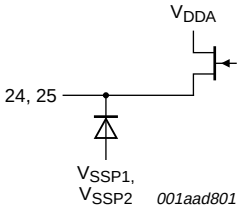
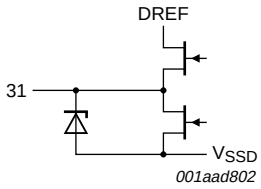
Pin	Symbol	Equivalent circuit
10	OSCREF	
11	HVPREF	
13	TEST	
18	DREF	
19	HVP2	
30	HVP1	
20	V_{DDP2}	
23	V_{SSP2}	
26	V_{SSP1}	
29	V_{DDP1}	

Table 7. Internal circuitry *...continued*

Pin	Symbol	Equivalent circuit
21	BOOT2	
28	BOOT1	
22	OUT2	
27	OUT1	
24	STAB2	
25	STAB1	
31	OSCIO	

10. Limiting values

Table 8. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions		Min	Max	Unit
V_P	supply voltage	asymmetrical supply	[1]	–0.3	+40	V
V_x	voltage on pin x					
	IN1P, IN1N, IN2P, IN2N		[2]	–5	+5	V
	OSCREF, OSCIO, TEST		[3]	$V_{SSD(HW)}$ – 0.3	5	V
	POWERUP, ENGAGE, DIAG		[4]	V_{CGND} – 0.3	6	V
	all other pins		[5]	V_{SS} – 0.3	V_{DD} + 0.3	V
I_{ORM}	repetitive peak output current	maximum output current limiting	[6]	4	-	A
T_j	junction temperature			-	150	°C
T_{stg}	storage temperature			–55	+150	°C
T_{amb}	ambient temperature			–40	+85	°C
P	power dissipation			-	5	W

[1] $V_P = V_{DDP1} – V_{SSP1} = V_{DDP2} – V_{SSP2}$.

[2] Measured with respect to pin INREF; $V_x < V_{DD} + 0.3$ V.

[3] Measured with respect to pin $V_{SSD(HW)}$; $V_x < V_{DD} + 0.3$ V.

[4] Measured with respect to pin CGND; $V_x < V_{DD} + 0.3$ V.

[5] $V_{SS} = V_{SSP1} = V_{SSP2}$; $V_{DD} = V_{DDP1} = V_{DDP2}$.

[6] Current limiting concept.

11. Thermal characteristics

Table 9. Thermal characteristics

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
$R_{th(j-a)}$	thermal resistance from junction to ambient	free air natural convection					
		JEDEC test board	[1]	-	41	44	K/W
		2 layer application board		-	44	-	K/W
Ψ_{j-lead}	thermal characterization parameter from junction to lead			-	-	30	K/W
Ψ_{j-top}	thermal characterization parameter from junction to top of package		[2]	-	-	8	K/W

[1] Measured on a JEDEC high K-factor test board (standard EIA/JESD 51-7) in free air with natural convection.

[2] Strongly depends on where you measure on the package.

12. Static characteristics

Table 10. Static characteristics

V_P = 22 V; f_{osc} = 320 kHz; T_{amb} = 25 °C; unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Supply						
V_P	supply voltage	asymmetrical supply	10	22	36	V
		symmetrical supply	±5	±11	±18	V
I_P	supply current	Sleep mode; no load	-	0.6	1	mA
$I_{q(tot)}$	total quiescent current	Operating mode; no load, no snubbers and no filter connected	-	40	80	mA
Series resistance output power switches						
R_{DSon}	drain-source on-state resistance	T_j = 25 °C	-	150	-	mΩ
		T_j = 125 °C	-	234	-	mΩ
Power-up input: pin POWERUP[1]						
V_I	input voltage		0	-	6.0	V
I_I	input current	V_I = 3 V	-	1	20	µA
V_{IL}	LOW-level input voltage		0	-	0.8	V
V_{IH}	HIGH-level input voltage		2	-	6.0	V
Engage input: pin ENGAGE[1]						
V_O	output voltage		4.2	4.6	5.0	V
V_I	input voltage		0	-	6.0	V
I_O	output current	V_I = 3 V	-	20	40	µA
V_{IL}	LOW-level input voltage		0	-	0.8	V
V_{IH}	HIGH-level input voltage		3	-	6.0	V
Diagnostic output: pin DIAG[1]						
V_O	output voltage	protection activated; see Table 6	-	-	0.8	V
		Operating mode	2	2.5	3.3	V
Bias voltage for inputs: pin INREF						
$V_{O(bias)}$	bias output voltage	with respect to pin V_{SSA}	-	2.1	-	V
Half supply voltage						
Pins HVP1 and HVP2						
V_O	output voltage	half supply voltage to charge SE capacitor	$0.5V_P$ – 0.2	$0.5V_P$	$0.5V_P$ + 0.2	V
I_O	output current	$V_{HVP1} = V_O - 1$ V; $V_{HVP2} = V_O - 1$ V	-	50	-	mA
Pin HVPREF						
V_O	output voltage	half supply reference voltage in Mute mode	$0.5V_P$ – 0.2	$0.5V_P$	$0.5V_P$ + 0.2	V
Reference voltage for internal logic: pin DREF						
V_O	output voltage		4.5	4.8	5.1	V

Table 10. Static characteristics *…continued*

V_P = 22 V; f_{osc} = 320 kHz; T_{amb} = 25 °C; unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Amplifier outputs: pins OUT1 and OUT2						
$\|V_{O(offset)}\|$	output offset voltage	SE; with respect to pin HVPREF				
		Mute mode	-	-	15	mV
		Operating mode	-	-	100	mV
		BTL				
		Mute mode	-	-	20	mV
		Operating mode	-	-	150	mV
Stabilizer output: pins STAB1 and STAB2						
V_O	output voltage	Mute mode and Operating mode; with respect to pins V_{SSP1} and V_{SSP2}	10	11	12	V
Voltage protection						
$V_{P(uvp)}$	undervoltage protection supply voltage		8.0	9.5	10	V
$V_{P(ovp)}$	overvoltage protection supply voltage		36	38.5	40	V
$V_{P(th)(ubp)l}$	low unbalance protection threshold supply voltage	V_{HVPREF} = 11 V	-	-	18	V
$V_{P(th)(ubp)h}$	high unbalance protection threshold supply voltage	V_{HVPREF} = 11 V	29	-	-	V
Current protection						
$I_{O(ocp)}$	overcurrent protection output current	current limiting	4	5	-	A
Temperature protection						
$T_{act(th\_prot)}$	thermal protection activation temperature		155	-	160	°C
$T_{act(th\_fold)}$	thermal foldback activation temperature		140	-	150	°C
Oscillator reference; pin OSCIO[2]						
V_{IH}	HIGH-level input voltage		4.0	-	5	V
V_{IL}	LOW-level input voltage		0	-	0.8	V
V_{OH}	HIGH-level output voltage		4.0	-	5	V
V_{OL}	LOW-level output voltage		0	-	0.8	V
$N_{slave(max)}$	maximum number of slaves	driven by one master	12	-	-	

[1] Measured with respect to pin CGND.

[2] Measured with respect to pin $V_{SSD(HW)}$.

13. Dynamic characteristics

Table 11. Switching characteristics

V_P = 22 V; T_{amb} = 25 °C; unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Internal oscillator						
f_{osc}	oscillator frequency	R_{osc} = 39 kΩ	-	320	-	kHz
		range	300	-	500	kHz
Timing PWM output: pins OUT1 and OUT2						
t_r	rise time	I_O = 0 A	-	10	-	ns
t_f	fall time	I_O = 0 A	-	10	-	ns
$t_{w(min)}$	minimum pulse width	I_O = 0 A	-	80	-	ns

Table 12. SE characteristics

V_P = 22 V; R_L = 2 × 4 Ω; f_i = 1 kHz; f_{osc} = 320 kHz; R_s < 0.1 Ω[1]; T_{amb} = 25 °C; unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
$P_{o(RMS)}$	RMS output power	continuous time output power per channel	[2]				
		R_L = 4 Ω; V_P = 22 V					
		THD+N = 0.5 %, f_i = 1 kHz		11	12	-	W
		THD+N = 0.5 %, f_i = 100 Hz		-	12	-	W
		THD+N = 10 %, f_i = 1 kHz		14	15	-	W
		THD+N = 10 %, f_i = 100 Hz		-	15	-	W
		R_L = 8 Ω; V_P = 30 V					
		THD+N = 0.5 %, f_i = 1 kHz		11	12	-	W
		THD+N = 0.5 %, f_i = 100 Hz		-	12	-	W
		THD+N = 10 %, f_i = 1 kHz		14	15	-	W
		THD+N = 10 %, f_i = 100 Hz		-	15	-	W
		short time output power per channel	[2]				
		R_L = 4 Ω; V_P = 29 V					
		THD+N = 0.5 %		19	20	-	W
		THD+N = 10 %		23	25	-	W
THD+N	total harmonic distortion-plus-noise	P_o = 1 W	[3]				
		f_i = 1 kHz		-	0.015	0.05	%
		f_i = 6 kHz		-	0.08	0.10	%
$G_{v(cl)}$	closed-loop voltage gain	V_i = 100 mV; no load		29	30	31	dB
$\|\Delta G_v\|$	voltage gain difference			-	0.5	1	dB
α_{cs}	channel separation	P_o = 1 W; f_i = 1 kHz		70	80	-	dB
SVRR	supply voltage ripple rejection	Operating mode	[4]				
		f_i = 100 Hz		-	60	-	dB
		f_i = 1 kHz		40	50	-	dB
$\|Z_i\|$	input impedance	differential		70	100	-	kΩ
$V_{n(o)}$	noise output voltage	Operating mode; R_s = 0 Ω	[5]	-	100	150	μV
		Mute mode	[5]	-	70	100	μV

Table 12. SE characteristics *...continued*

V_P = 22 V; R_L = 2 × 4 Ω; f_i = 1 kHz; f_{osc} = 320 kHz; R_s < 0.1 Ω[1]; T_{amb} = 25 °C; unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{O(mute)}$	mute output voltage	Mute mode; V_i = 1 V (RMS) and f_i = 1 kHz	-	100	-	μV
CMRR	common mode rejection ratio	$V_{i(cm)}$ = 1 V (RMS)	56	75	-	dB
η_{po}	output power efficiency	P_o = 15 W				
		V_P = 22 V; R_L = 4 Ω	90	92	-	%
		V_P = 30 V; R_L = 8 Ω	91	93	-	%

[1] R_s is the series resistance of inductor of low-pass LC filter in the application.

[2] Output power is measured indirectly; based on R_{DSon} measurement.

[3] THD+N is measured in a bandwidth of 20 Hz to 20 kHz, AES17 brick wall.

[4] Maximum V_{ripple} = 2 V (p-p); R_s = 0 Ω.

[5] B = 20 Hz to 20 kHz, AES17 brick wall.

Table 13. BTL characteristics

V_P = 22 V; R_L = 8 Ω; f_i = 1 kHz; f_{osc} = 320 kHz; R_s < 0.1 Ω[1]; T_{amb} = 25 °C; unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
$P_{o(RMS)}$	RMS output power	continuous time output power	[2]				
		R_L = 4 Ω; V_P = 12 V					
		THD+N = 0.5 %; f_i = 1 kHz		11	12	-	W
		THD+N = 0.5 %; f_i = 100 Hz		-	12	-	W
		THD+N = 10 %; f_i = 1 kHz		14	15	-	W
		THD+N = 10 %; f_i = 100 Hz		-	15	-	W
		R_L = 8 Ω; V_P = 22 V					
		THD+N = 0.5 %; f_i = 1 kHz		23	24	-	W
		THD+N = 0.5 %; f_i = 100 Hz		-	24	-	W
		THD+N = 10 %; f_i = 1 kHz		28	30	-	W
		THD+N = 10 %; f_i = 100 Hz		-	30	-	W
		short time output power	[2]				
		R_L = 4 Ω; V_P = 15 V					
		THD+N = 0.5 %		19	20	-	W
		THD+N = 10 %		23	25	-	W
		R_L = 8 Ω; V_P = 29 V					
		THD+N = 0.5 %		38	40	-	W
		THD+N = 10 %		47	50	-	W
THD+N	total harmonic distortion-plus-noise	P_o = 1 W	[3]				
		f_i = 1 kHz		-	0.04	0.1	%
		f_i = 6 kHz		-	0.04	0.1	%
$G_{v(cl)}$	closed-loop voltage gain			35	36	37	dB
SVRR	supply voltage ripple rejection	Operating mode	[4]				
		f_i = 100 Hz		-	75	-	dB
		f_i = 1000 Hz		70	75	-	dB
		sleep; f_i = 100 Hz	[4]	-	80	-	dB

Table 13. BTL characteristics *…continued*

V_P = 22 V; R_L = 8 Ω; f_i = 1 kHz; f_{osc} = 320 kHz; R_s < 0.1 Ω[1]; T_{amb} = 25 °C; unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
$\|Z_i\|$	input impedance	differential		35	50	-	kΩ
$V_{n(o)}$	noise output voltage	R_s = 0 Ω					
		Operating mode	[5]	-	100	150	μV
		Mute mode	[5]	-	70	100	μV
$V_{O(mute)}$	mute output voltage	Mute mode; V_i = 1 V (RMS) and f_i = 1 kHz		-	100	-	μV
CMRR	common mode rejection ratio	$V_{i(cm)}$ = 1 V (RMS)		56	75	-	dB
η_{po}	output power efficiency	P_o = 15 W; V_P = 12 V and R_L = 4 Ω		88	90	-	%
		P_o = 30 W; V_P = 22 V and R_L = 8 Ω		90	92	-	%

[1] R_s is the series resistance of inductor of low-pass LC filter in the application.

[2] Output power is measured indirectly; based on R_{DSon} measurement.

[3] THD+N is measured in a bandwidth of 20 Hz to 20 kHz, AES17 brick wall.

[4] Maximum V_{ripple} = 2 V (p-p); R_s = 0 Ω.

[5] B = 20 Hz to 20 kHz, AES17 brick wall.

14. Application information

14.1 Output power estimation

The output power P_o at THD+N = 0.5 %, just before clipping, for the SE and BTL configuration can be estimated using Equation 2 and Equation 3.

SE configuration:

$$P_{o(0.5\%)} = \frac{\left[\left(\frac{R_L}{R_L + R_{DSon} + R_s + R_{ESR}}\right) \times (1 - t_{w(min)} \times f_{osc}) \times V_P\right]^2}{8 \times R_L} \quad (2)$$

BTL configuration:

$$P_{o(0.5\%)} = \frac{\left[\left(\frac{R_L}{R_L + 2 \times (R_{DSon} + R_s)}\right) \times (1 - t_{w(min)} \times f_{osc}) \times V_P\right]^2}{2 \times R_L} \quad (3)$$

Where:

V_P = supply voltage $V_{DDP1} - V_{SSP1}$ [V] or $V_{DDP2} - V_{SSP2}$ [V]

R_L = load impedance [Ω]

R_{DSon} = on-resistance power switch [Ω]

R_s = series resistance output inductor [Ω]

R_{ESR} = equivalent series resistance SE capacitor [Ω]

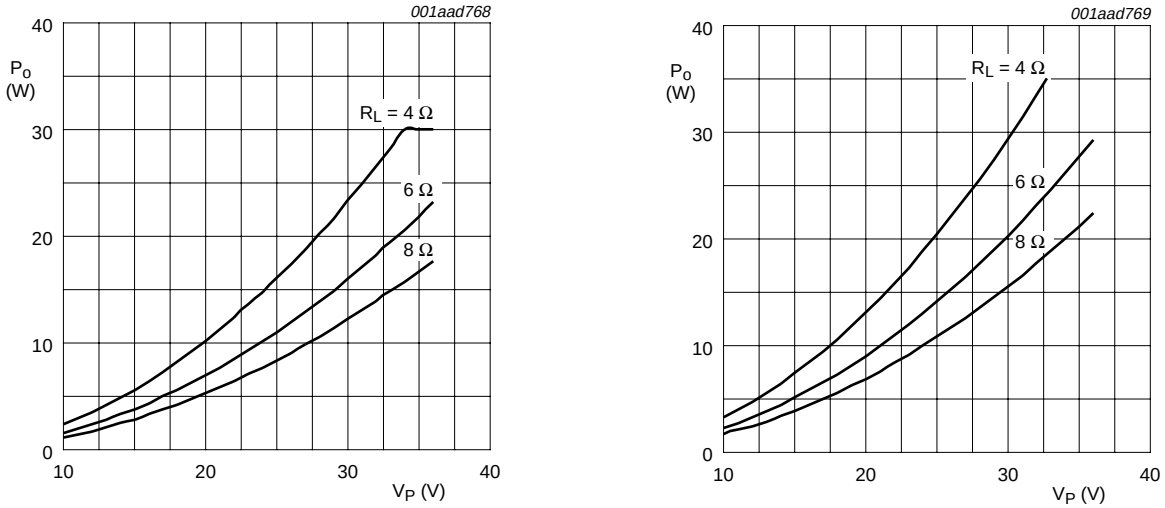
$t_{w(min)}$ = minimum pulse width [s]; 80 ns typical

f_{osc} = oscillator frequency [Hz]; 320 kHz typical with R_{osc} = 39 kΩ

The output power P_o at THD+N = 10 % can be estimated by:

$$P_{o(10\%)} = 1.25 \times P_{o(0.5\%)} \quad (4)$$

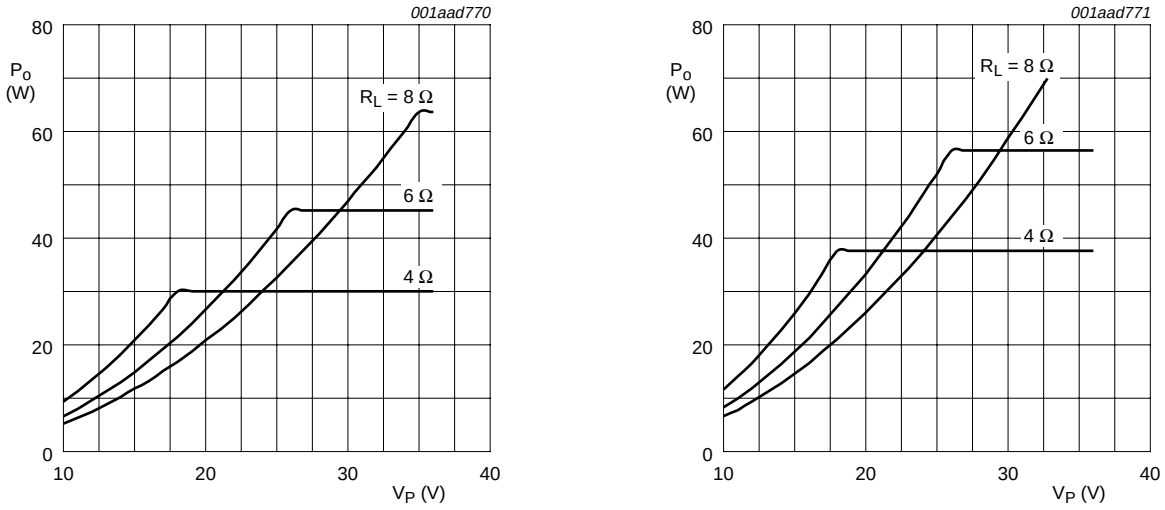
Figure 7 and Figure 8 show the estimated output power at THD+N = 0.5 % and THD+N = 10 % as a function of the supply voltage for SE and BTL configurations at different load impedances. The output power is calculated with: R_{DSon} = 0.15 Ω (at T_j = 25 °C), R_s = 0.05 Ω, R_{ESR} = 0.05 Ω and $I_{O(ocp)}$ = 4 A (minimum).



a. THD+N = 0.5 %

b. THD+N = 10 %

Fig 7. SE output power as a function of supply voltage



a. THD+N = 0.5 %

b. THD+N = 10 %

Fig 8. BTL output power as a function of supply voltage

14.2 Output current limiting

The peak output current $I_{O(max)}$ is internally limited above a level of 4 A (minimum). During normal operation the output current should not exceed this threshold level of 4 A otherwise the output signal is distorted. The peak output current in SE or BTL configurations can be estimated using Equation 5 and Equation 6.

SE configuration:

$$I_{O(max)} \leq \frac{0.5 \times V_P}{R_L + R_{DSon} + R_s + R_{ESR}} \leq 4\ A \quad (5)$$

BTL configuration:

$$I_{O(max)} \leq \frac{V_P}{R_L + 2 \times (R_{DSon} + R_s)} \leq 4\ A \quad (6)$$

Where:

V_P = supply voltage $V_{DDP1} - V_{SSP1}$ [V] or $V_{DDP2} - V_{SSP2}$ [V]

R_L = load impedance [Ω]

R_{DSon} = on-resistance power switch [Ω]

R_s = series resistance output inductor [Ω]

R_{ESR} = equivalent series resistance SE capacitor [Ω]

Example:

A 4 Ω speaker in the BTL configuration can be used up to a supply voltage of 18 V without running into current limiting. Current limiting (clipping) will avoid audio holes but it causes a comparable distortion like voltage clipping.

14.3 Speaker configuration and impedance

For a flat frequency response (second-order Butterworth filter) it is necessary to change the low-pass filter components Llc and Clc according to the speaker configuration and impedance. Table 14 shows the practical required values.

Table 14. Filter component values

Configuration	R_L (Ω)	Llc (μH)	Clc (nF)
SE	4	22	680
	6	33	470
	8	47	330
BTL	4	10	1500
	6	15	1000
	8	22	680

14.4 Single-ended capacitor

The SE capacitor forms a high-pass filter with the speaker impedance. So the frequency response will roll-off with 20 dB per decade below f_{-3dB} (3 dB cut-off frequency).

The 3 dB cut-off frequency is equal to:

$$f_{-3dB} = \frac{1}{2\pi \times R_L \times Cse} \quad (7)$$

Where:

f_{-3dB} = 3 dB cut-off frequency [Hz]

R_L = load impedance [Ω]

Cse = single-ended capacitance [F]; see Figure 28

Table 15 shows an overview of the required SE capacitor values in case of 60 Hz, 40 Hz or 20 Hz 3 dB cut-off frequency.

Table 15. SE capacitor values

Impedance (Ω)	Cse (μF)		
	f_{-3dB} = 60 Hz	f_{-3dB} = 40 Hz	f_{-3dB} = 20 Hz
4	680	1000	2200
6	470	680	1500
8	330	470	1000

14.5 Gain reduction

The gain of the TDA8932 is internally fixed at 30 dB for SE (or 36 dB for BTL). The gain can be reduced by a resistive voltage divider at the input (see Figure 9).

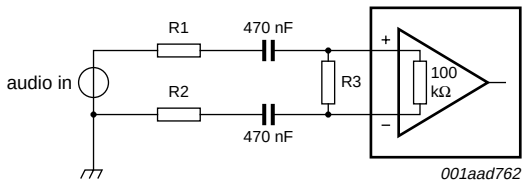


Fig 9. Input configuration for reducing gain

When applying a resistive divider, the total closed-loop gain $G_{v(tot)}$ can be calculated by Equation 8 and Equation 9:

$$G_{v(tot)} = G_{v(cl)} + 20log\left[\frac{R_{EQ}}{R_{EQ} + (R1 + R2)}\right] \quad (8)$$

Where:

$G_{v(tot)}$ = total closed-loop voltage gain [dB]

$G_{v(cl)}$ = closed-loop voltage gain, fixed at 30 dB for SE [dB]

R_{EQ} = equivalent resistance, R3 and Z_i [Ω]

R1 = series resistor [Ω]

R2 = series resistor [Ω]

$$R_{EQ} = \frac{R3 \times Z_i}{R3 + Z_i} \quad (9)$$

Where:

R_{EQ} = equivalent resistance [Ω]

R3 = parallel resistor [Ω]

Z_i = internal input impedance

Example:

Substituting R1 = R2 = 4.7 kΩ, Z_i = 100 kΩ and R3 = 22 kΩ in Equation 8 and Equation 9 results in a gain of $G_{v(tot)}$ = 26.3 dB.

14.6 Device synchronization

If two or more TDA8932 devices are used in one application it is recommended that all devices are synchronized running at the same switching frequency to avoid beat tones. Synchronization can be realized by connecting all OSCIO pins together and configure one of the TDA8932 devices as master, while the other TDA8932 devices are configured as slaves (see Figure 10).

A device is configured as master by connecting a resistor between pins OSCREF and $V_{SSD(HW)}$ setting the carrier frequency. Pin OSCIO of the master is then configured as an oscillator output for synchronization. The OSCREF pins of the slave devices should be shorted to $V_{SSD(HW)}$ configuring pin OSCIO as an input.

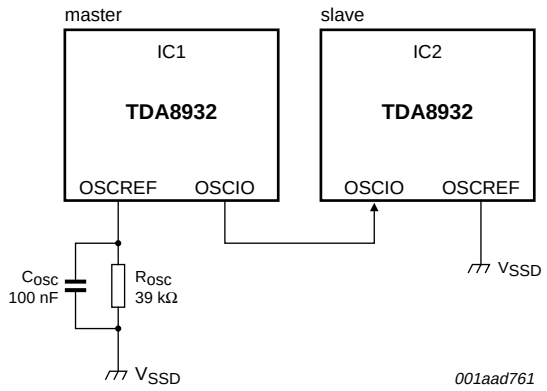


Fig 10. Master slave concept in two chip application

14.7 Thermal behavior (printed-circuit board considerations)

The heatsink in the application with the TDA8932 is made with the copper on the Printed-Circuit Board (PCB). The TDA8932 uses the four corner leads (pins 1, 16, 17 and 32) for heat transfer from the die to the PCB. The thermal foldback will limit the maximum junction temperature to 140 °C.

Equation 10 shows the relation between the maximum allowable power dissipation P and the thermal resistance from junction to ambient.

$$R_{th(j-a)} = \frac{T_{j(max)} - T_{amb}}{P} \quad (10)$$

Where:

$R_{th(j-a)}$ = thermal resistance from junction to ambient

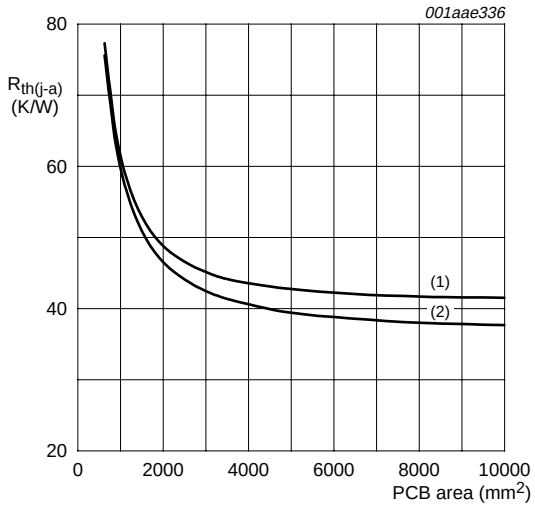
$T_{j(max)}$ = maximum junction temperature

T_{amb} = ambient temperature

P = power dissipation which is determined by the efficiency of the TDA8932

The power dissipation is shown in Figure 20 (SE) and Figure 27 (BTL).

The thermal resistance as a function of the PCB area (35 µm copper) is shown in Figure 11.



(1) Single layer FR2 PCB; copper plane at device side (100 % coverage).

(2) Double layer FR4 PCB; copper plane on both sides (100 % coverage).

Fig 11. Thermal resistance as a function of the PCB area

Example 1

- At V_P = 30 V and P_o = 2 × 15 W into 8 Ω (THD+N = 10 % continuous), the power dissipation P = 2.3 W at P_o = 15 W (see Figure 20).
- $T_{j(max)}$ = 125 °C and T_{amb} = 25 °C.

The required thermal resistance $R_{th(j-a)}$ = 100 / 2.3 = 43 K/W.

Example 2

In case of music output power at 25 % of the rated power, the $T_{j(max)}$ is much lower.

- At V_P = 30 V and $P_o = 2 \times (0.25 \times 15) = 2 \times 3.75$ W into 8 Ω, the power dissipation P = 1.6 W at P_o = 3.75 W (see Figure 20)
- $R_{th(j-a)}$ = 43 K/W

The maximum junction temperature $T_{j(max)} = 25 + 1.6 \times 43 = 93.8$ °C.

14.8 Pumping effects

When the amplifier is used in a SE configuration, a so-called 'pumping effect' can occur. During one switching interval, energy is taken from one supply (e.g. V_{DDP1}), while a part of that energy is delivered back to the other supply line (e.g. V_{SSP1}) and visa versa. When the power supply cannot sink energy, the voltage across the output capacitors of that power supply will increase.

The voltage increase caused by the pumping effect depends on:

- Speaker impedance
- Supply voltage
- Audio signal frequency
- Value of decoupling capacitors on supply lines
- Source and sink currents of other channels

The pumping effect should not cause a malfunction of either the audio amplifier and/or the power supply. For instance, this malfunction can be caused by triggering of the undervoltage or overvoltage protection of the amplifier.

Pumping effects in a SE configuration can be minimized by connecting audio inputs in anti-phase and change the polarity of one speaker. This is illustrated in Figure 12.

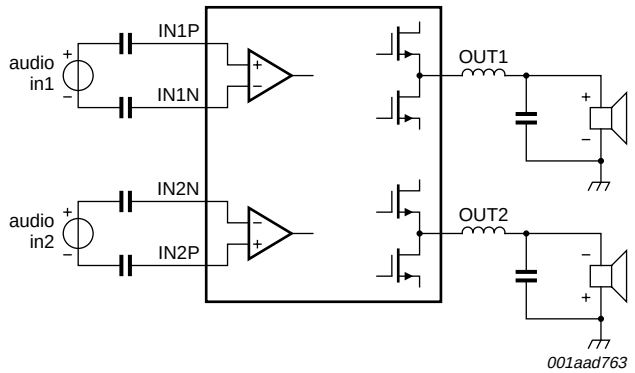
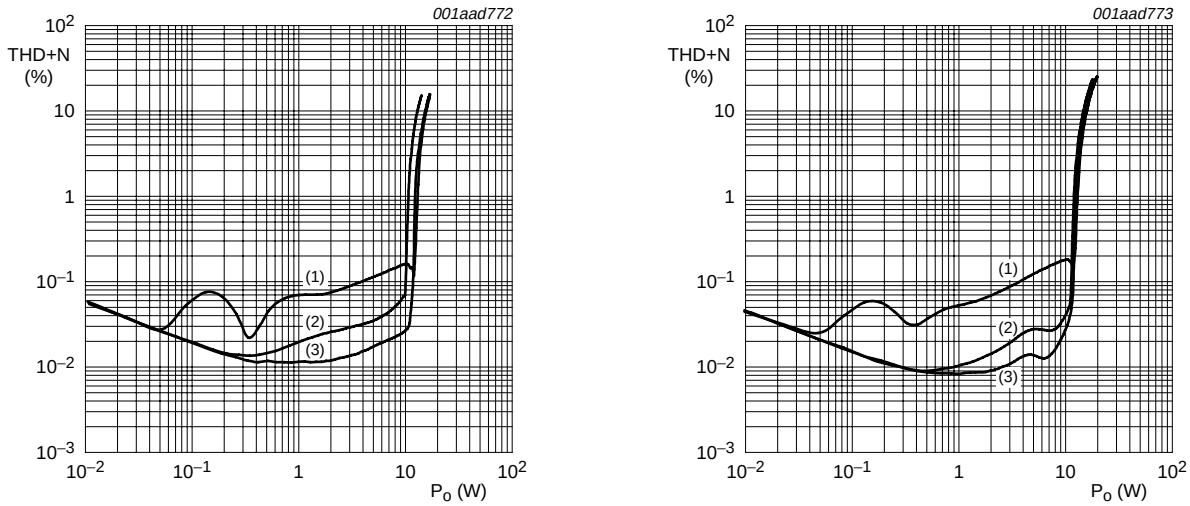


Fig 12. SE application for reducing pumping effects

14.9 SE curves measured in reference design



a. V_P = 22 V; R_L = 2 × 4 Ω

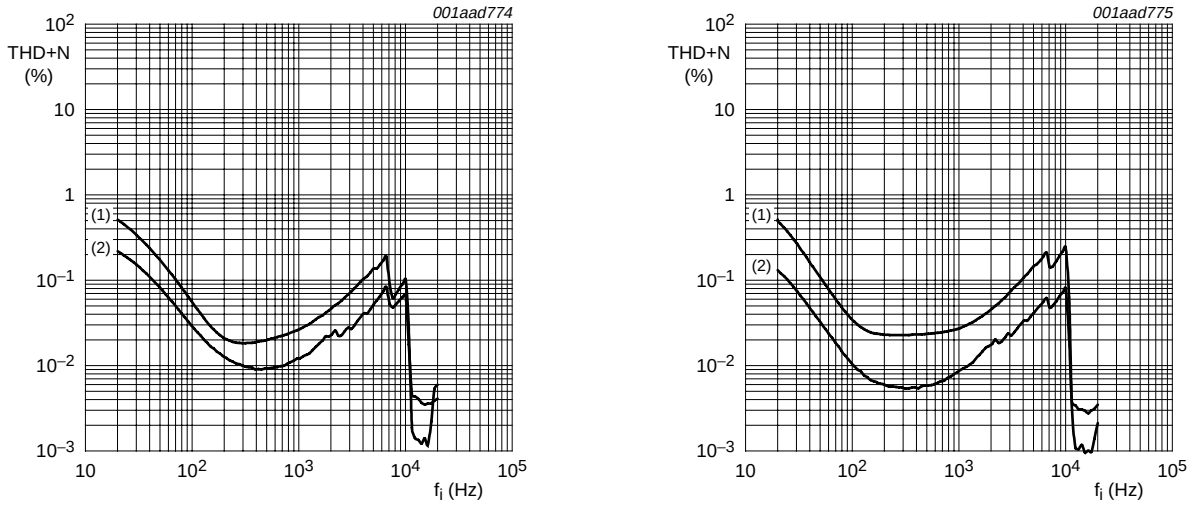
b. V_P = 30 V; R_L = 2 × 8 Ω

(1) f_i = 6 kHz

(2) f_i = 100 Hz

(3) f_i = 1 kHz

Fig 13. Total harmonic distortion-plus-noise as a function of output power



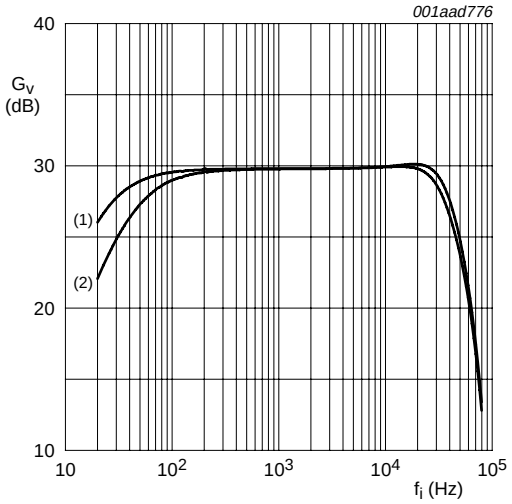
a. V_P = 22 V; R_L = 2 × 4 Ω

b. V_P = 30 V; R_L = 2 × 8 Ω

(1) P_o = 10 W

(2) P_o = 1 W

Fig 14. Total harmonic distortion-plus-noise as a function of frequency

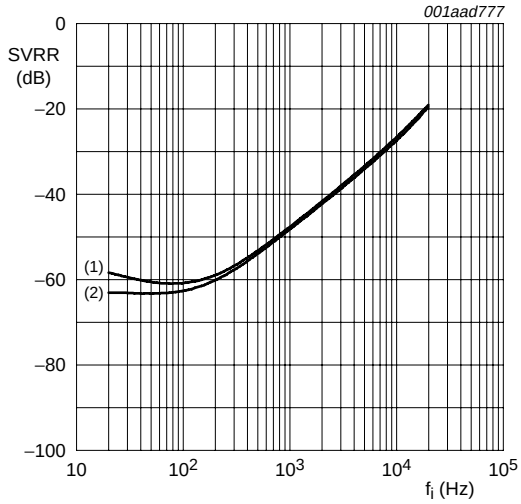


V_i = 100 mV (RMS); R_i = 0 Ω; Cse = 1000 µF

(1) V_P = 30 V; R_L = 2 × 8 Ω

(2) V_P = 22 V; R_L = 2 × 4 Ω

Fig 15. Gain as a function of frequency

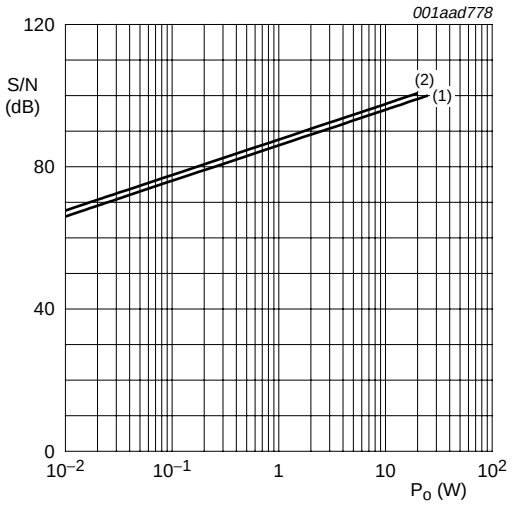


V_{ripple} = 500 mV (RMS) referenced to ground; R_i = 0 Ω (shorted input)

(1) V_P = 30 V; R_L = 2 × 8 Ω

(2) V_P = 22 V; R_L = 2 × 4 Ω

Fig 16. Supply voltage ripple rejection as a function of frequency

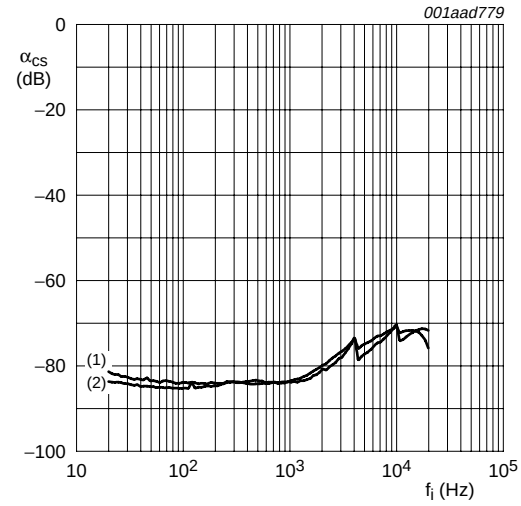


V_P = 22 V; R_i = 0 Ω; 20 kHz brick-wall filter AES17

(1) R_L = 2 × 4 Ω

(2) R_L = 2 × 8 Ω

Fig 17. Signal-to-noise ratio as a function of output power

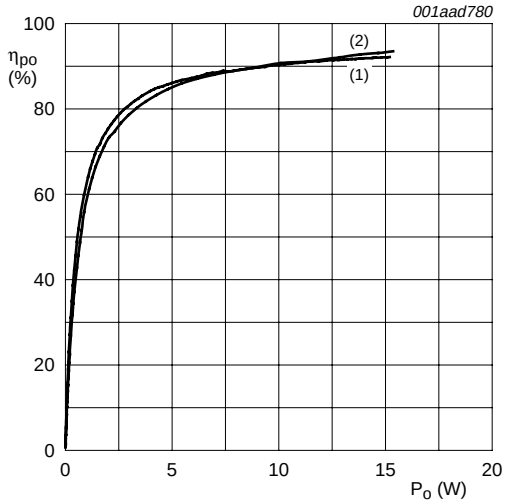


P_o = 1 W; Chvpref = 47 µF

(1) V_P = 22 V; R_L = 2 × 4 Ω

(2) V_P = 30 V; R_L = 2 × 8 Ω

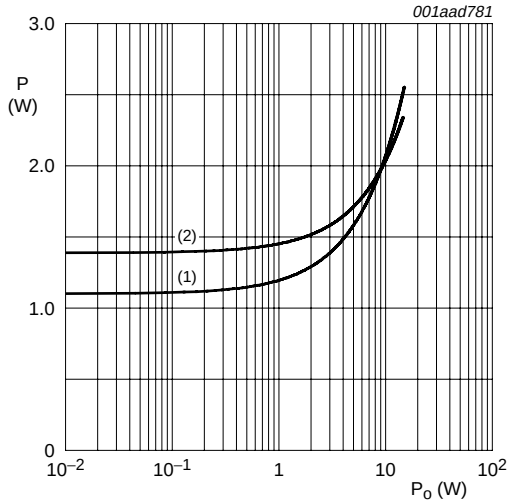
Fig 18. Channel separation as a function of frequency



(1) V_P = 22 V; R_L = 2 × 4 Ω; f_i = 1 kHz

(2) V_P = 30 V; R_L = 2 × 8 Ω; f_i = 1 kHz

Fig 19. Output power efficiency as a function of output power

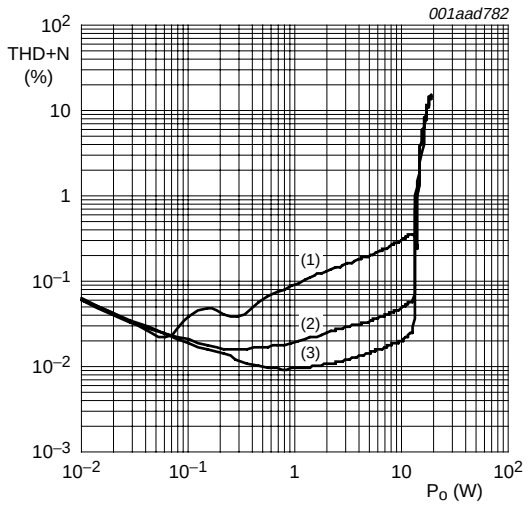


(1) V_P = 22 V; R_L = 2 × 4 Ω; f_i = 1 kHz

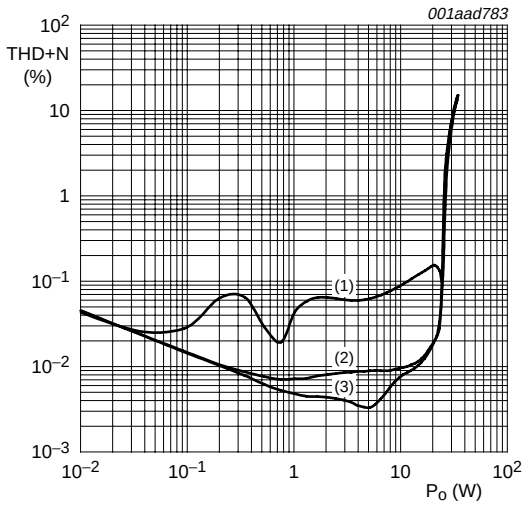
(2) V_P = 30 V; R_L = 2 × 8 Ω; f_i = 1 kHz

Fig 20. Power dissipation as a function of output power per channel (two channels driven)

14.10 BTL curves measured in reference design



a. V_P = 12 V; R_L = 4 Ω



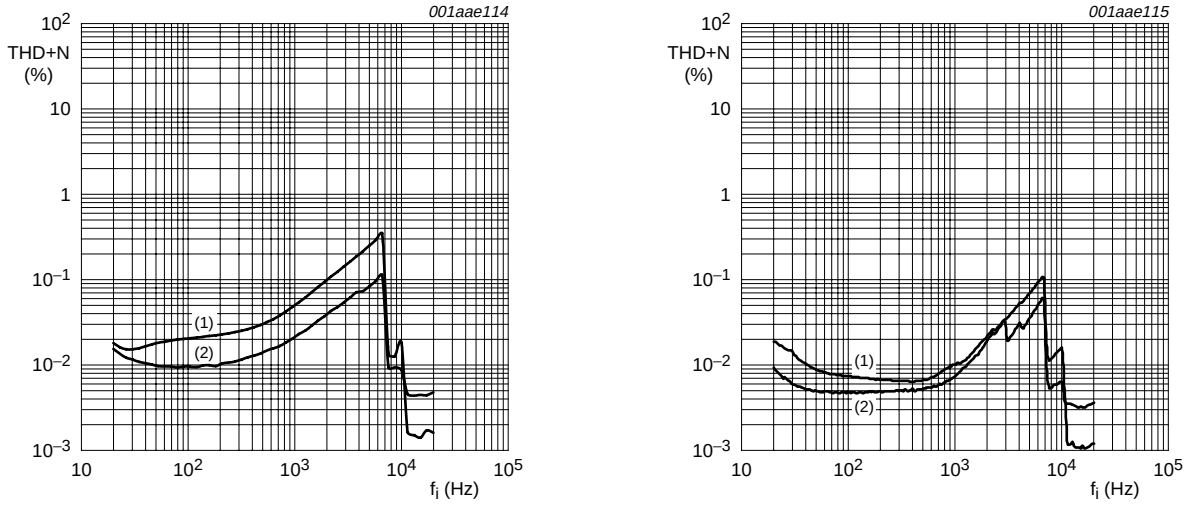
b. V_P = 24 V; R_L = 8 Ω

(1) f_i = 6 kHz

(2) f_i = 1 kHz

(3) f_i = 100 Hz

Fig 21. Total harmonic distortion-plus-noise as a function of output power



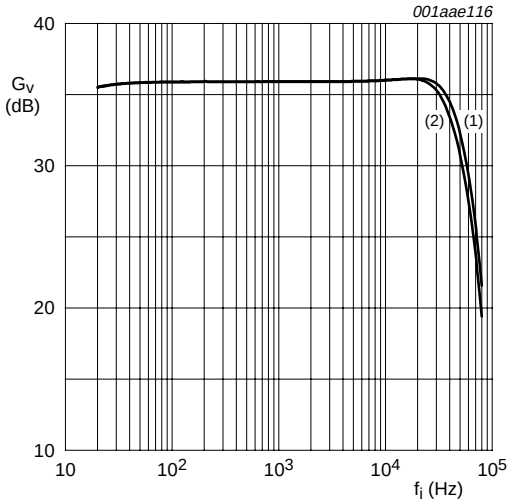
a. V_P = 22 V; R_L = 4 Ω

b. V_P = 22 V; R_L = 8 Ω

(1) P_o = 10 W

(2) P_o = 1 W

Fig 22. Total harmonic distortion-plus-noise as a function of frequency

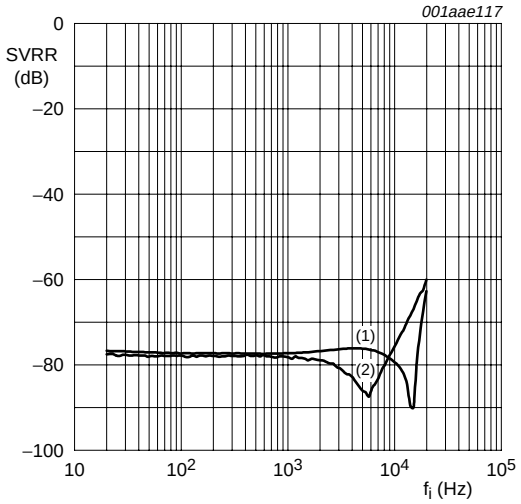


V_i = 100 mV (RMS); R_i = 0 Ω

(1) V_P = 12 V; R_L = 4 Ω

(2) V_P = 24 V; R_L = 8 Ω

Fig 23. Gain as a function of frequency

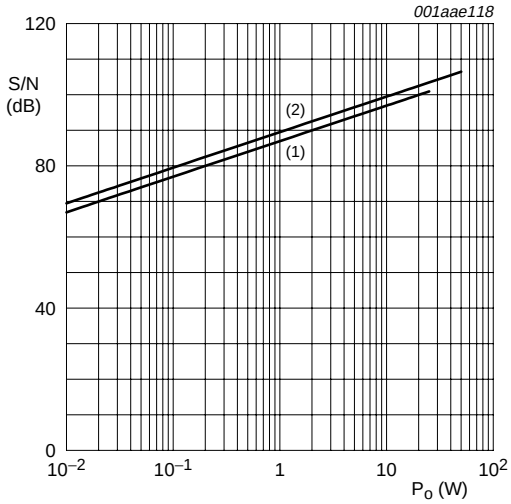


V_{ripple} = 500 mV (RMS) referenced to ground;
R_i = 0 Ω (shorted input)

(1) R_L = 4 Ω

(2) R_L = 8 Ω

Fig 24. Supply voltage ripple rejection as a function of frequency

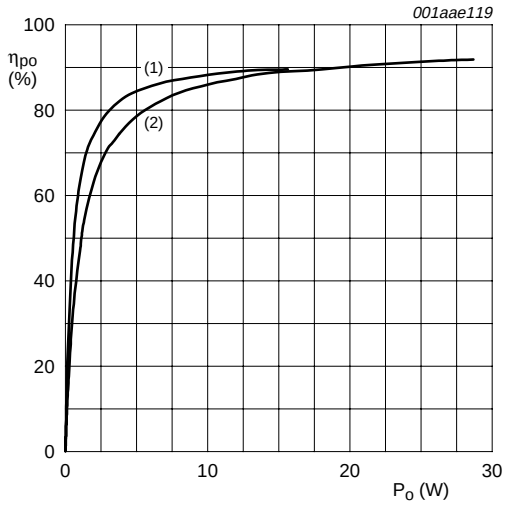


R_i = 0 Ω; 20 kHz brick-wall filter AES17

(1) R_L = 4 Ω; V_P = 15 V

(2) R_L = 8 Ω; V_P = 29 V

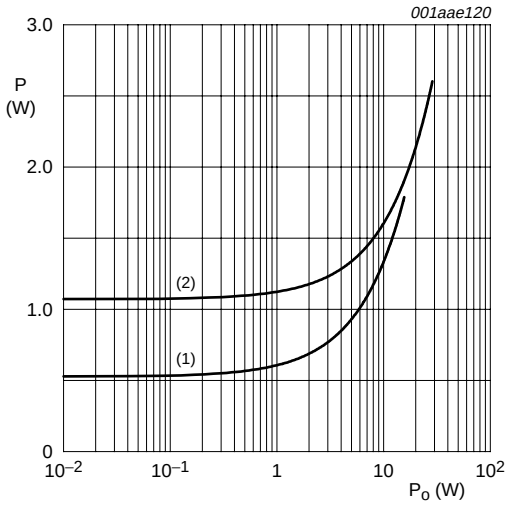
Fig 25. Signal-to-noise ratio as a function of output power



(1) V_P = 12 V; R_L = 2 × 4 Ω; f_i = 1 kHz

(2) V_P = 22 V; R_L = 2 × 8 Ω; f_i = 1 kHz

Fig 26. Output power efficiency as a function of output power



(1) V_P = 12 V; R_L = 2 × 4 Ω; f_i = 1 kHz

(2) V_P = 22 V; R_L = 2 × 8 Ω; f_i = 1 kHz

Fig 27. Power dissipation as a function of output power

14.11 Typical application schematics (simplified)

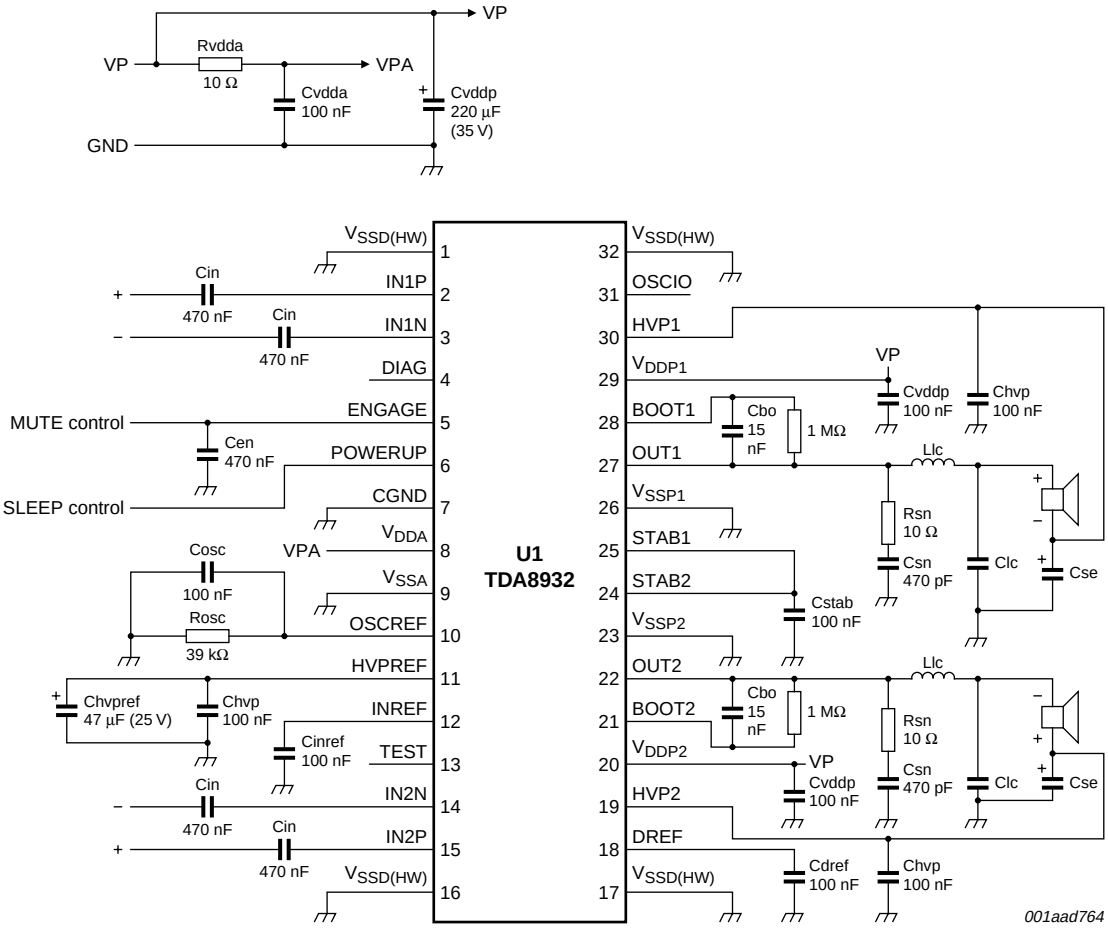


Fig 28. Typical simplified application diagram for 2 × SE (asymmetrical supply)

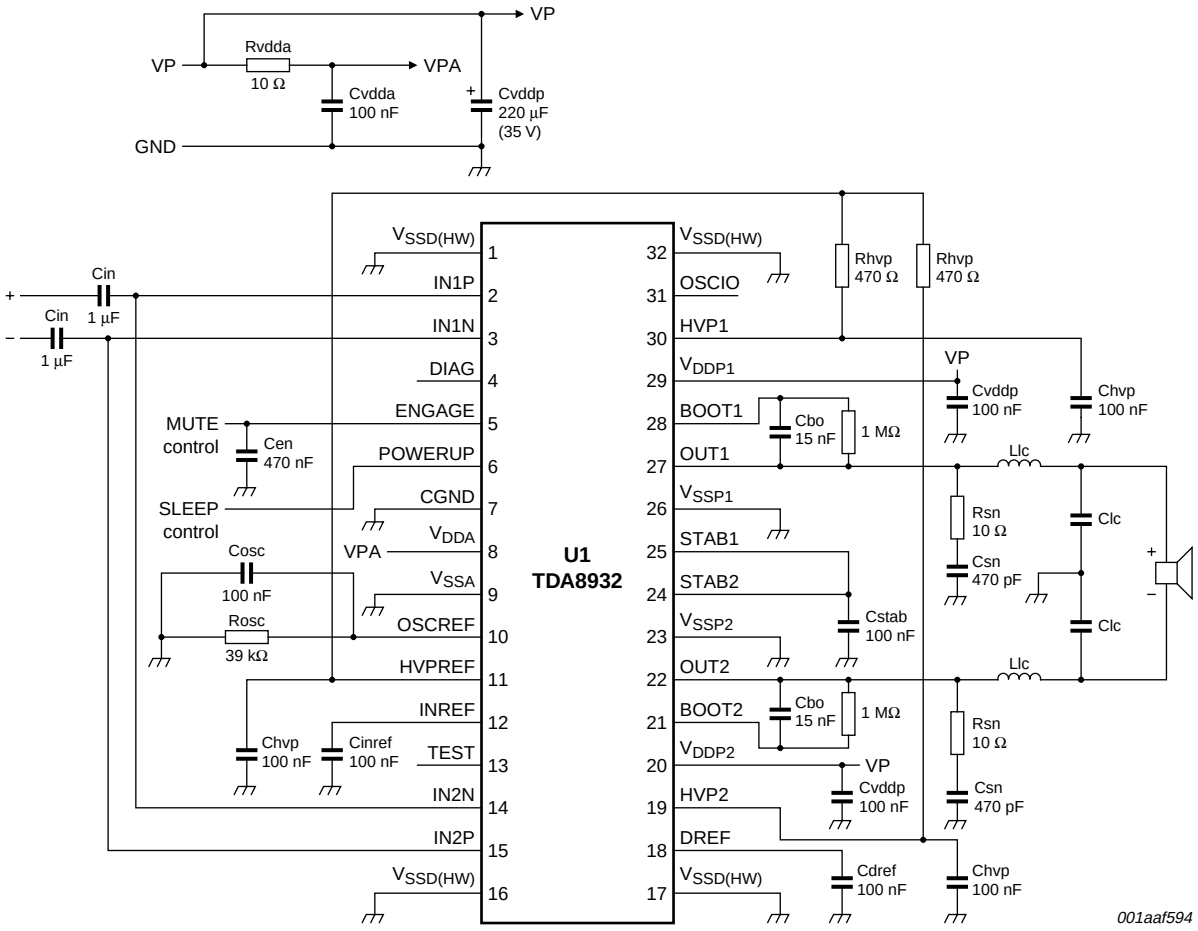


Fig 29. Typical simplified application diagram for 1 × BTL (asymmetrical supply)

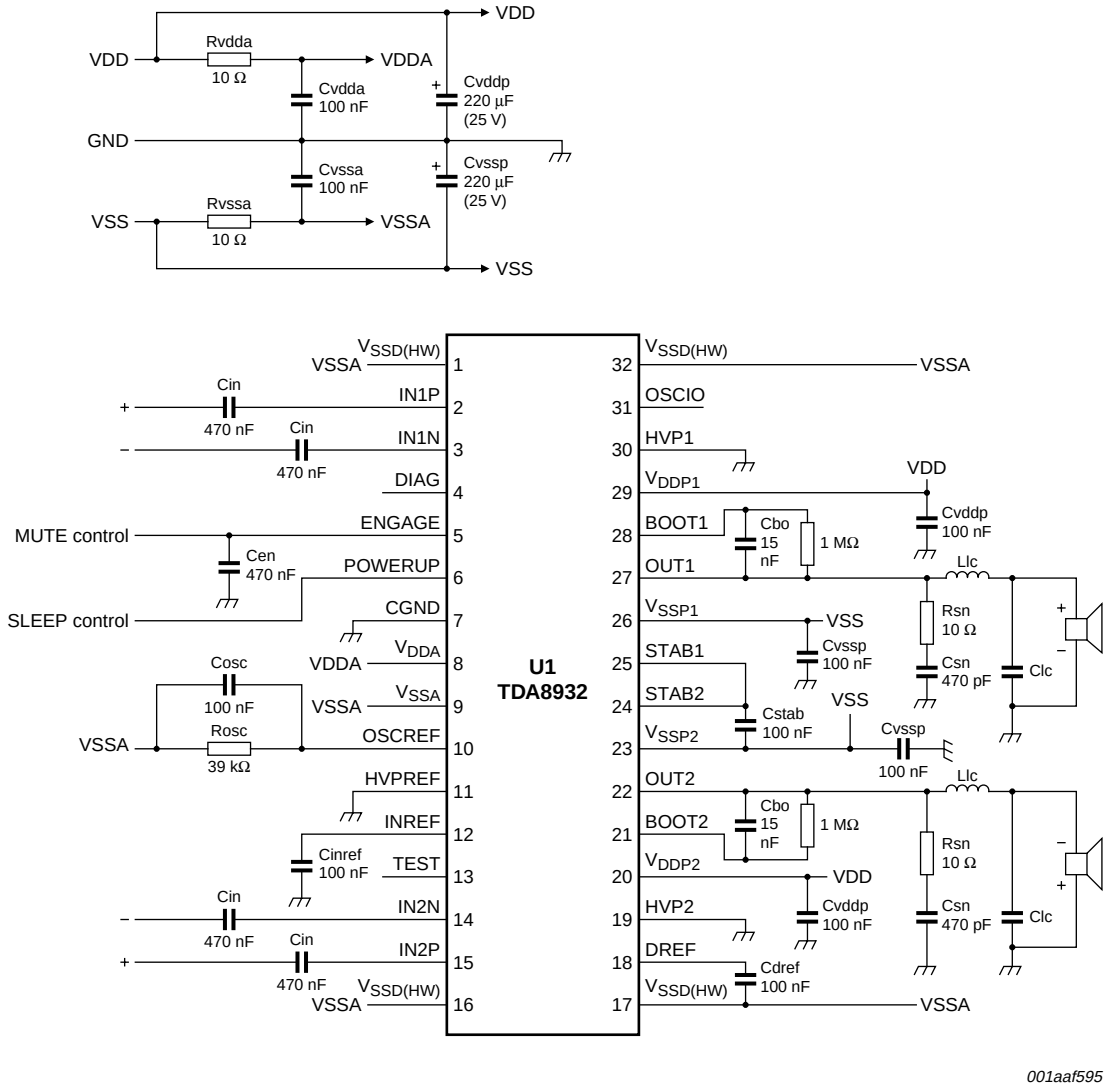


Fig 30. Typical simplified application diagram for 2 × SE (symmetrical supply)

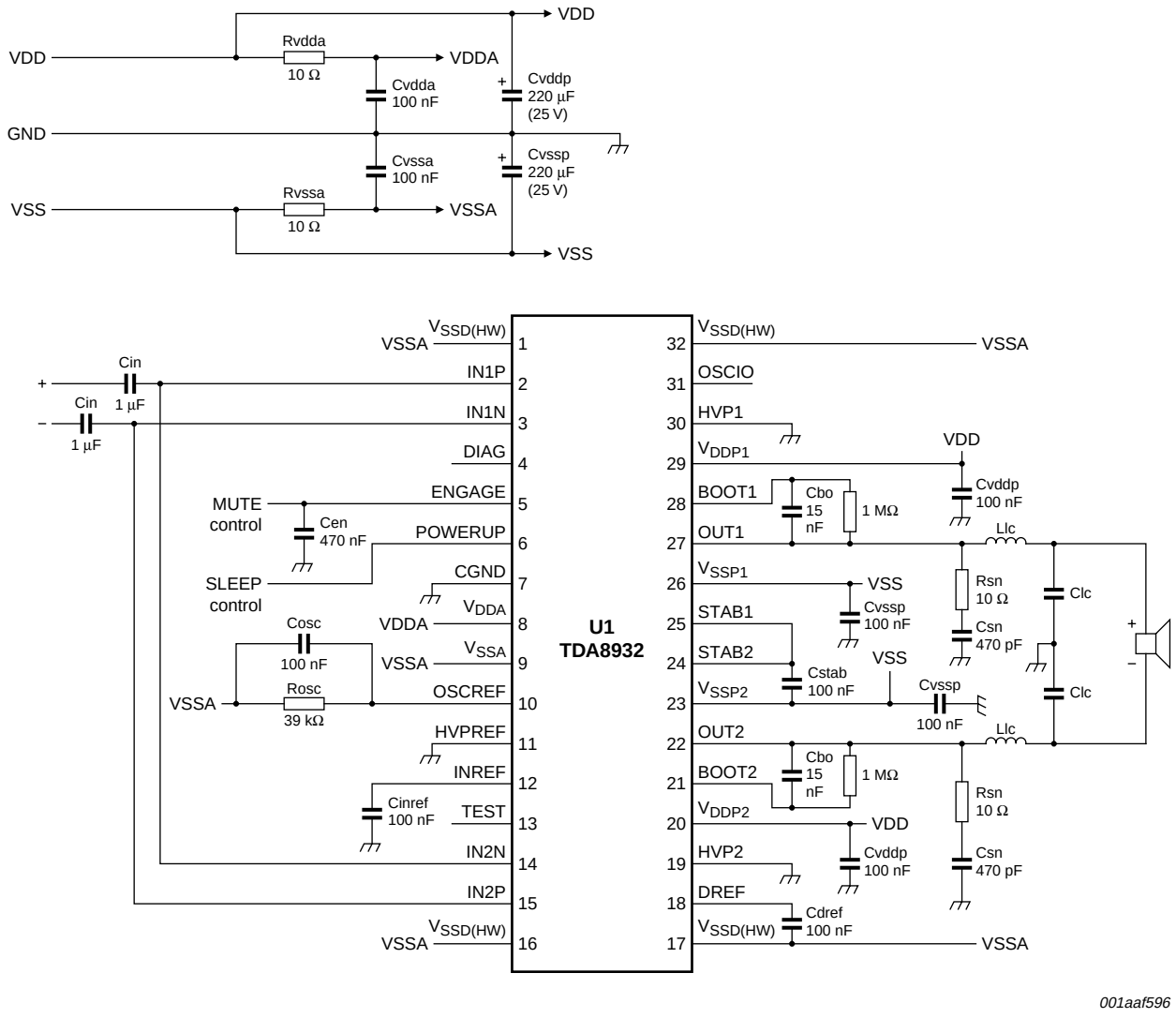


Fig 31. Typical simplified application diagram for 1 × BTL (symmetrical supply)

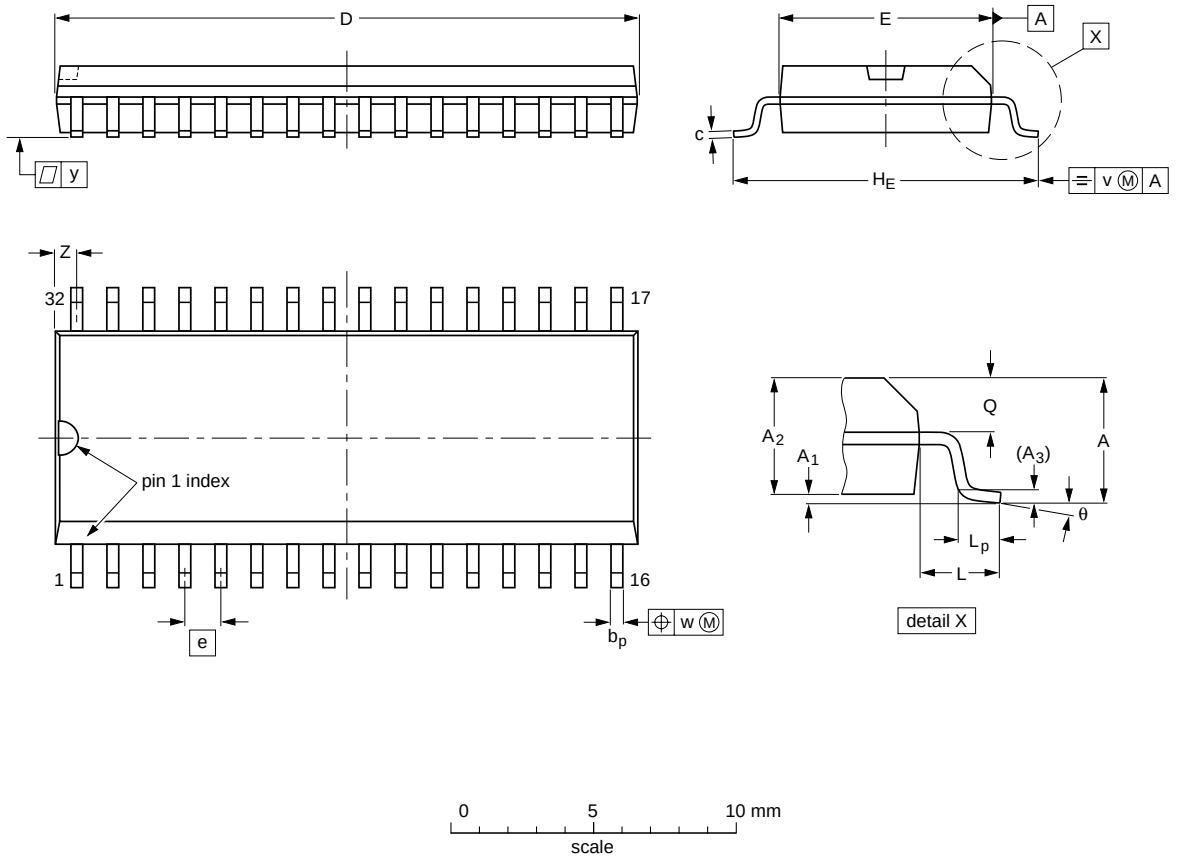
15. Test information

15.1 Quality information

The *General Quality Specification for Integrated Circuits, SNW-FQ-611* is applicable.

16. Package outline

SO32: plastic small outline package; 32 leads; body width 7.5 mm **SOT287-1**



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(1)}$	e	H_E	L	L_p	Q	v	w	y	$Z^{(1)}$	θ
mm	2.65	0.3 0.1	2.45 2.25	0.25	0.49 0.36	0.27 0.18	20.7 20.3	7.6 7.4	1.27	10.65 10.00	1.4	1.1 0.4	1.2 1.0	0.25	0.25	0.1	0.95 0.55	8^o 0^o
inches	0.1	0.012 0.004	0.096 0.089	0.01	0.02 0.01	0.011 0.007	0.81 0.80	0.30 0.29	0.05	0.419 0.394	0.055	0.043 0.016	0.047 0.039	0.01	0.01	0.004	0.037 0.022	

Note

1. Plastic or metal protrusions of 0.15 mm (0.006 inch) maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT287-1		MO-119				~~00-08-17~~ 03-02-19

Fig 32. Package outline SOT287-1 (SO32)

17. Soldering

This text provides a very brief insight into a complex technology. A more in-depth account of soldering ICs can be found in Application Note *AN10365 "Surface mount reflow soldering description"*.

17.1 Introduction to soldering

Soldering is one of the most common methods through which packages are attached to Printed Circuit Boards (PCBs), to form electrical circuits. The soldered joint provides both the mechanical and the electrical connection. There is no single soldering method that is ideal for all IC packages. Wave soldering is often preferred when through-hole and Surface Mount Devices (SMDs) are mixed on one printed wiring board; however, it is not suitable for fine pitch SMDs. Reflow soldering is ideal for the small pitches and high densities that come with increased miniaturization.

17.2 Wave and reflow soldering

Wave soldering is a joining technology in which the joints are made by solder coming from a standing wave of liquid solder. The wave soldering process is suitable for the following:

- Through-hole components
- Leaded or leadless SMDs, which are glued to the surface of the printed circuit board

Not all SMDs can be wave soldered. Packages with solder balls, and some leadless packages which have solder lands underneath the body, cannot be wave soldered. Also, leaded SMDs with leads having a pitch smaller than ~0.6 mm cannot be wave soldered, due to an increased probability of bridging.

The reflow soldering process involves applying solder paste to a board, followed by component placement and exposure to a temperature profile. Leaded packages, packages with solder balls, and leadless packages are all reflow solderable.

Key characteristics in both wave and reflow soldering are:

- Board specifications, including the board finish, solder masks and vias
- Package footprints, including solder thieves and orientation
- The moisture sensitivity level of the packages
- Package placement
- Inspection and repair
- Lead-free soldering versus PbSn soldering

17.3 Wave soldering

Key characteristics in wave soldering are:

- Process issues, such as application of adhesive and flux, clinching of leads, board transport, the solder wave parameters, and the time during which components are exposed to the wave
- Solder bath specifications, including temperature and impurities

17.4 Reflow soldering

Key characteristics in reflow soldering are:

- Lead-free versus SnPb soldering; note that a lead-free reflow process usually leads to higher minimum peak temperatures (see Figure 33) than a PbSn process, thus reducing the process window
- Solder paste printing issues including smearing, release, and adjusting the process window for a mix of large and small components on one board
- Reflow temperature profile; this profile includes preheat, reflow (in which the board is heated to the peak temperature) and cooling down. It is imperative that the peak temperature is high enough for the solder to make reliable solder joints (a solder paste characteristic). In addition, the peak temperature must be low enough that the packages and/or boards are not damaged. The peak temperature of the package depends on package thickness and volume and is classified in accordance with Table 16 and 17

Table 16. SnPb eutectic process (from J-STD-020C)

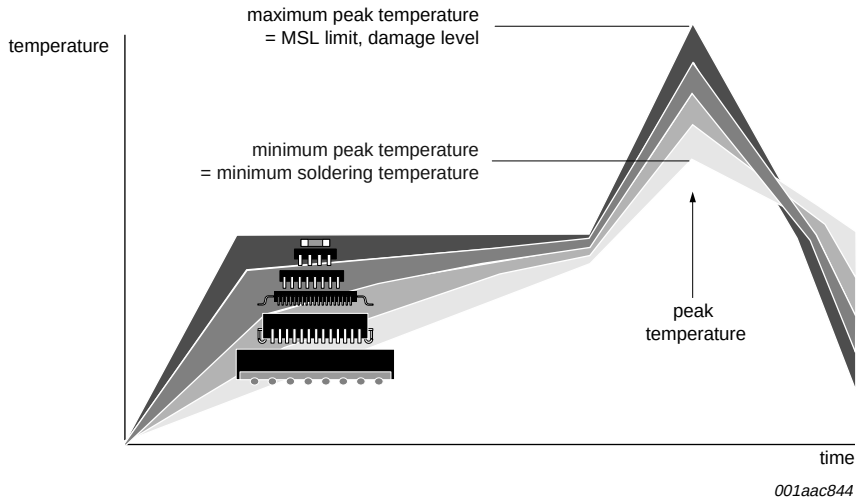
Package thickness (mm)	Package reflow temperature (°C)	
	Volume (mm^3)	
	< 350	≥ 350
< 2.5	235	220
≥ 2.5	220	220

Table 17. Lead-free process (from J-STD-020C)

Package thickness (mm)	Package reflow temperature (°C)		
	Volume (mm^3)		
	< 350	350 to 2000	> 2000
< 1.6	260	260	260
1.6 to 2.5	260	250	245
> 2.5	250	245	245

Moisture sensitivity precautions, as indicated on the packing, must be respected at all times.

Studies have shown that small packages reach higher temperatures during reflow soldering, see Figure 33.



MSL: Moisture Sensitivity Level

Fig 33. Temperature profiles for large and small components

For further information on temperature profiles, refer to Application Note *AN10365 "Surface mount reflow soldering description"*.

18. Abbreviations

Table 18. Abbreviations

Acronym	Description
BTL	Bridge Tied Load
DMOS	Double diffused Metal Oxide Semiconductor
ESD	ElectroStatic Discharge
PWM	Pulse Width Modulation
OCP	OverCurrent Protection
OTP	OverTemperature Protection
OVP	OverVoltage Protection
SE	Single Ended
UBP	UnBalance Protection
UVP	UnderVoltage Protection
TF	Thermal Foldback
WP	Window Protection

19. Revision history

Table 19. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
TDA8932_2	20061212	Preliminary data sheet	-	TDA8932_1
Modifications:	• The format of this data sheet has been redesigned to comply with the new identity guidelines of NXP Semiconductors. • Legal texts have been adapted to the new company name where appropriate. • Type number TDA8932TW has been deleted • Two new symbols and parameters in Table 9 “Thermal characteristics” • Minor adaptions in application diagrams Figure 29, Figure 30 and Figure 31			
TDA8932_1	20060511	Preliminary data sheet	-	-

20. Legal information

20.1 Data sheet status

Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL http://www.nxp.com.

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