RoHS compliant

N-CHANNEL MOSFET

Qualified per MIL-PRF-19500/556

Qualified Levels:
JAN, JANTX, and JANTXV

DESCRIPTION

This family of 2N6782U, 2N6784U and 2N6786U switching transistors are military qualified up to the JANTXV level for high-reliability applications. These devices are also available in thru hole TO-205AF package. Microsemi also offers numerous other transistor products to meet higher and lower power ratings with various switching speed requirements in both through-hole and surface-mount packages.

Important: For the latest information, visit our website http://www.microsemi.com.

U-18 LCC Package

Also available in:

TO-205AF (TO-39) package
(leaded)
2N6782 & 2N6786

FEATURES

- Surface mount equivalent of JEDEC registered 2N6782, 2N6784 and 2N6786 number series.
- JAN, JANTX, and JANTXV qualifications are available per MIL-PRF-19500/556. (See part nomenclature for all available options.)
- RoHS compliant by design.

APPLICATIONS / BENEFITS

- Lightweight surface mount design enables mounting in a crowded area.
- Military and other high-reliability applications.

MAXIMUM RATINGS @ T_A = +25 ºC unless otherwise stated

Parameters / Test Conditions		Symbol	Value	Unit
Operating & Storage Junction Temperature Range		T_J & T_{stg}	-55 to +150	°C
Thermal Resistance Junction-to-Case		$R_{\Theta JC}$	8.33	°C/W
Total Power Dissipation	@ T_A = +25 °C @ T_C = +25 °C (1)	P_T	0.8 15	W
Drain-Source Voltage, dc	2N6782U 2N6784U 2N6786U	V_{DS}	100 200 400	V
Gate-Source Voltage, dc		V_{GS}	± 20	V
Drain Current, dc @ T_C = +25 ºC (2)	2N6782U 2N6784U 2N6786U	I_{D1}	3.50 2.25 1.25	A
Drain Current, dc @ T_C = +100 ºC (2)	2N6782U 2N6784U 2N6786U	I_{D2}	2.25 1.50 0.80	A
Off-State Current (Peak Total Value) (3)	2N6782U 2N6784U 2N6786U	I_{DM}	14.0 9.0 5.5	A (pk)
Source Current	2N6782U 2N6784U 2N6786U	I_S	3.50 2.25 1.25	A

See notes on next page.

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Notes: 1. Derate linearly 0.12 W/°C for T_C > +25 °C.

2. The following formula derives the maximum theoretical I_D limit. I_D is also limited by package and internal wires and may be limited due to pin diameter.

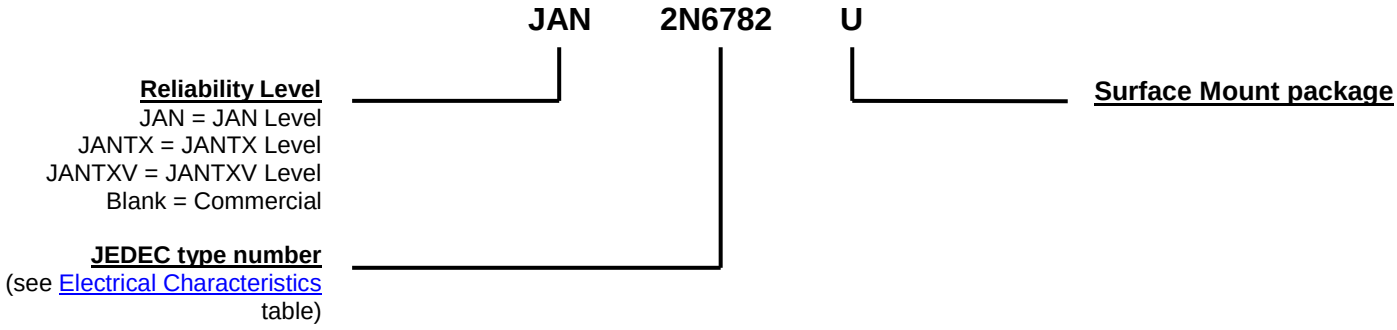
$$I_D = \sqrt{\frac{T_J(max) - T_C}{R_{\theta JC} \times R_{DS(on)} @ T_J(max)}}$$

3. I_{DM} = 4 x I_{D1} as calculated in note 1.

MECHANICAL and PACKAGING

- CASE: Ceramic LCC-18 with kovar gold plated lid.
- TERMINALS: Gold plating over nickel.
- MARKING: Manufacturer's ID, part number, date code, ESD symbol at Pin 1 location.
- TAPE & REEL option: Standard per EIA-481-D. Consult factory for quantities.
- See Package Dimensions on last page.

PART NOMENCLATURE



SYMBOLS & DEFINITIONS

Symbol	Definition
di/dt	Rate of change of diode current while in reverse-recovery mode, recorded as maximum value.
I_F	Forward current
R_G	Gate drive impedance
V_{DD}	Drain supply voltage
V_{DS}	Drain source voltage, dc
V_{GS}	Gate source voltage, dc

ELECTRICAL CHARACTERISTICS @ T_A = +25 °C, unless otherwise noted

Parameters / Test Conditions		Symbol	Min.	Max.	Unit
OFF CHARACTERISTICS					
Drain-Source Breakdown Voltage					
V_{GS} = 0 V, I_D = 1.0 mA	2N6782U 2N6784U 2N6786U	$V_{(BR)DSS}$	100 200 400		V
Gate-Source Voltage (Threshold)					
$V_{DS} \geq V_{GS}$, I_D = 0.25 mA		$V_{GS(th)1}$	2.0	4.0	V
$V_{DS} \geq V_{GS}$, I_D = 0.25 mA, T_J = +125 °C		$V_{GS(th)2}$	1.0		
$V_{DS} \geq V_{GS}$, I_D = 0.25 mA, T_J = -55 °C		$V_{GS(th)3}$		5.0	
Gate Current					
V_{GS} = ± 20 V, V_{DS} = 0 V		I_{GSS1}		±100	nA
V_{GS} = ± 20 V, V_{DS} = 0 V, T_J = +125 °C		I_{GSS2}		±200	
Drain Current					
V_{GS} = 0 V, V_{DS} = 80 V	2N6782U				
V_{GS} = 0 V, V_{DS} = 160 V	2N6784U	I_{DSS1}		25	µA
V_{GS} = 0 V, V_{DS} = 320 V	2N6786U				
Drain Current					
V_{GS} = 0 V, V_{DS} = 80 V, T_J = +125 °C	2N6782U				
V_{GS} = 0 V, V_{DS} = 160 V, T_J = +125 °C	2N6784U	I_{DSS2}		0.25	mA
V_{GS} = 0 V, V_{DS} = 320 V, T_J = +125 °C	2N6786U				
Static Drain-Source On-State Resistance					
V_{GS} = 10 V, I_D = 2.25 A pulsed	2N6782U			0.60	
V_{GS} = 10 V, I_D = 1.50 A pulsed	2N6784U	$r_{DS(on)1}$		1.50	Ω
V_{GS} = 10 V, I_D = 0.80 A pulsed	2N6786U			3.60	
Static Drain-Source On-State Resistance					
V_{GS} = 10 V, I_D = 3.50 A pulsed	2N6782U			0.61	
V_{GS} = 10 V, I_D = 2.25 A pulsed	2N6784U	$r_{DS(on)2}$		1.60	Ω
V_{GS} = 10 V, I_D = 1.25 A pulsed	2N6786U			3.70	
Static Drain-Source On-State Resistance					
T_J = +125 °C					
V_{GS} = 10 V, I_D = 2.25 A pulsed	2N6782U			1.08	
V_{GS} = 10 V, I_D = 1.50 A pulsed	2N6784U	$r_{DS(on)3}$		2.81	Ω
V_{GS} = 10 V, I_D = 0.80 A pulsed	2N6786U			7.92	
Diode Forward Voltage					
V_{GS} = 0 V, I_D = 3.50 A pulsed	2N6782U			1.5	
V_{GS} = 0 V, I_D = 2.25 A pulsed	2N6784U	V_{SD}		1.5	V
V_{GS} = 0 V, I_D = 1.25 A pulsed	2N6786U			1.4	

ELECTRICAL CHARACTERISTICS @ T_A = +25 °C, unless otherwise noted (continued)

DYNAMIC CHARACTERISTICS

Parameters / Test Conditions		Symbol	Min.	Max.	Unit
Gate Charge:					
On-State Gate Charge					
V_{GS} = 10 V, I_D = 3.50 A, V_{DS} = 50 V	2N6782U	$Q_{g(on)}$		8.1	nC
V_{GS} = 10 V, I_D = 2.25 A, V_{DS} = 100 V	2N6784U			8.6	
V_{GS} = 10 V, I_D = 1.25 A, V_{DS} = 200 V	2N6786U			12	
Gate to Source Charge					
V_{GS} = 10 V, I_D = 3.50 A, V_{DS} = 50 V	2N6782U	Q_{gs}		1.7	nC
V_{GS} = 10 V, I_D = 2.25 A, V_{DS} = 100 V	2N6784U			1.5	
V_{GS} = 10 V, I_D = 1.25 A, V_{DS} = 200 V	2N6786U			1.8	
Gate to Drain Charge					
V_{GS} = 10 V, I_D = 3.50 A, V_{DS} = 50 V	2N6782U	Q_{gd}		4.5	nC
V_{GS} = 10 V, I_D = 2.25 A, V_{DS} = 100 V	2N6784U			5.5	
V_{GS} = 10 V, I_D = 1.25 A, V_{DS} = 200 V	2N6786U			7.6	

SWITCHING CHARACTERISTICS

Parameters / Test Conditions		Symbol	Min.	Max.	Unit
Turn-on delay time					
I_D = 3.50 A, V_{GS} = 10 V, R_G = 7.5 Ω, V_{DD} = 50 V	2N6782U	$t_{d(on)}$		15	ns
I_D = 2.25 A, V_{GS} = 10 V, R_G = 7.5 Ω, V_{DD} = 100 V	2N6784U				
I_D = 1.25 A, V_{GS} = 10 V, R_G = 7.5 Ω, V_{DD} = 200 V	2N6786U				
Rinse time					
I_D = 3.50 A, V_{GS} = 10 V, R_G = 7.5 Ω, V_{DD} = 50 V	2N6782U	t_r		25	ns
I_D = 2.25 A, V_{GS} = 10 V, R_G = 7.5 Ω, V_{DD} = 100 V	2N6784U			20	
I_D = 1.25 A, V_{GS} = 10 V, R_G = 7.5 Ω, V_{DD} = 200 V	2N6786U			20	
Turn-off delay time					
I_D = 3.50 A, V_{GS} = 10 V, R_G = 7.5 Ω, V_{DD} = 50 V	2N6782U	$t_{d(off)}$		25	ns
I_D = 2.25 A, V_{GS} = 10 V, R_G = 7.5 Ω, V_{DD} = 100 V	2N6784U			30	
I_D = 1.25 A, V_{GS} = 10 V, R_G = 7.5 Ω, V_{DD} = 200 V	2N6786U			35	
Fall time					
I_D = 3.50 A, V_{GS} = 10 V, R_G = 7.5 Ω, V_{DD} = 50 V	2N6782U	t_f		20	ns
I_D = 2.25 A, V_{GS} = 10 V, R_G = 7.5 Ω, V_{DD} = 100 V	2N6784U			20	
I_D = 1.25 A, V_{GS} = 10 V, R_G = 7.5 Ω, V_{DD} = 200 V	2N6786U			30	
Diode Reverse Recovery Time					
di/dt ≤ 100 A/µs, V_{DD} ≤ 50 V, I_F = 3.50 A	2N6782U	t_{rr}		180	ns
di/dt ≤ 100 A/µs, V_{DD} ≤ 50 V, I_F = 2.25 A	2N6784U			350	
di/dt ≤ 100 A/µs, V_{DD} ≤ 50 V, I_F = 1.25 A	2N6786U			540	

GRAPHS

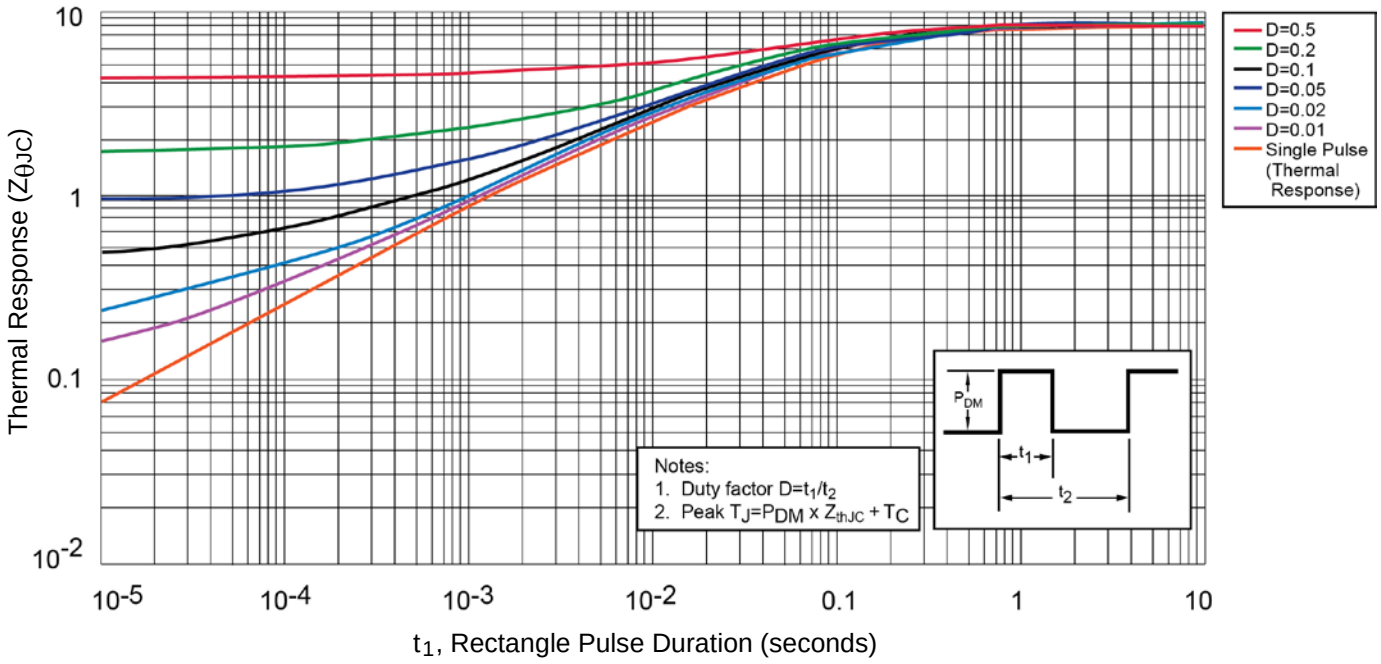
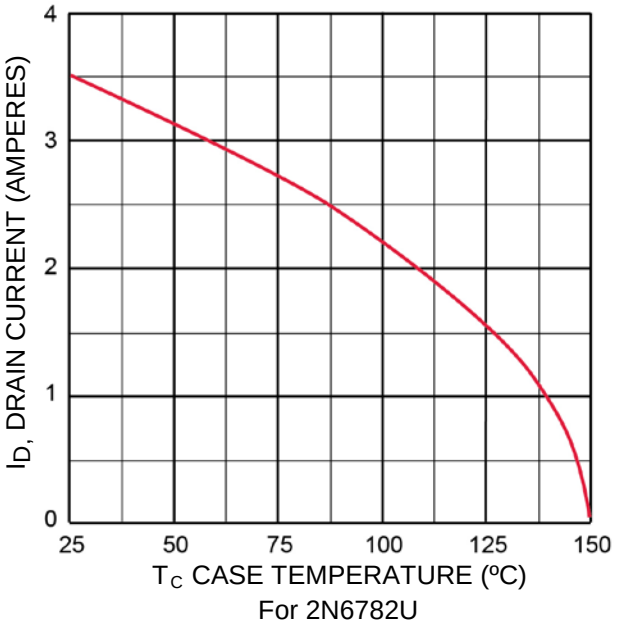


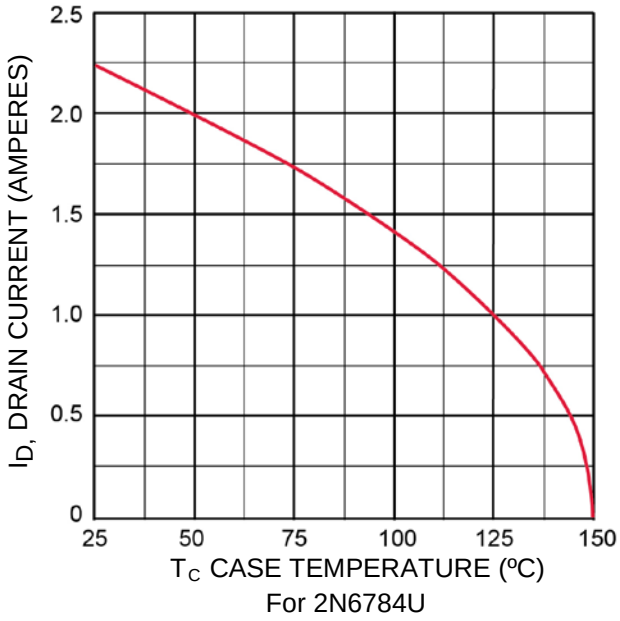
FIGURE 1
Thermal Response Curves

GRAPHS (continued)

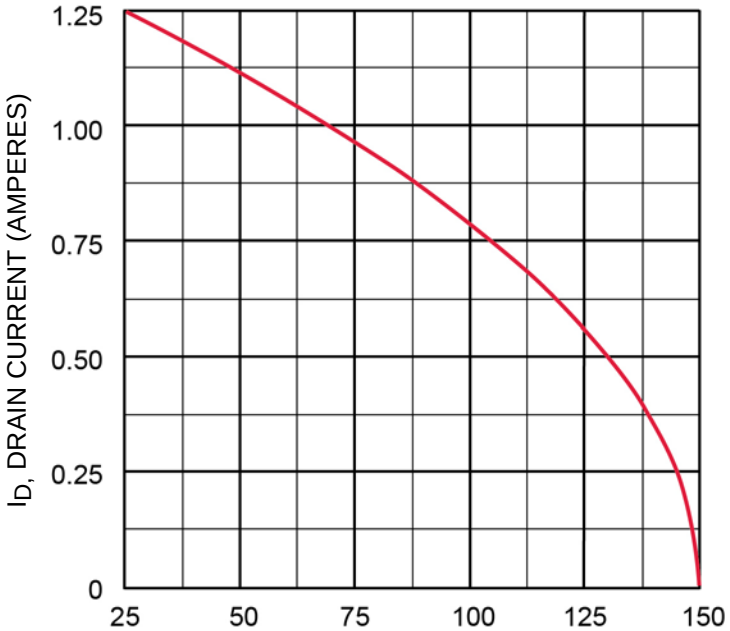
FIGURE 2 – Maximum Drain Current vs Case Temperature Graphs



For 2N6782U



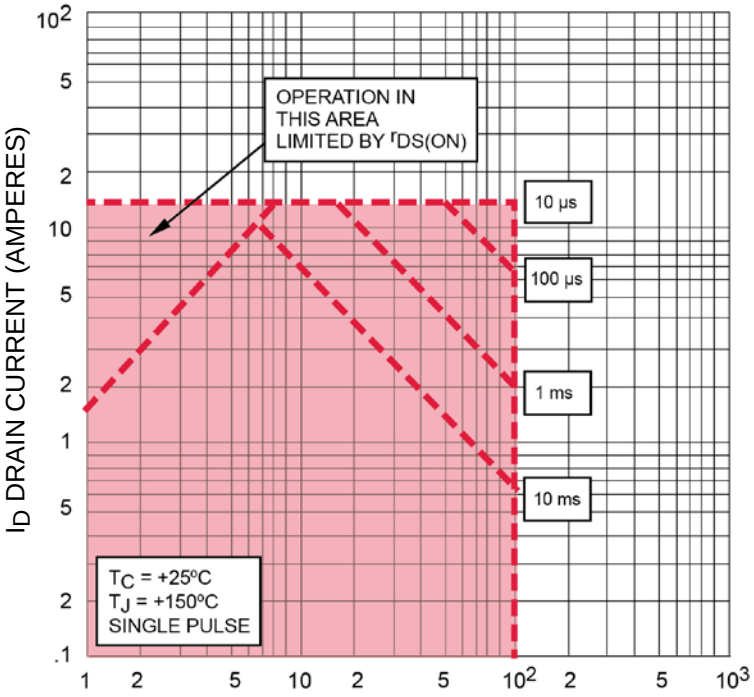
For 2N6784U

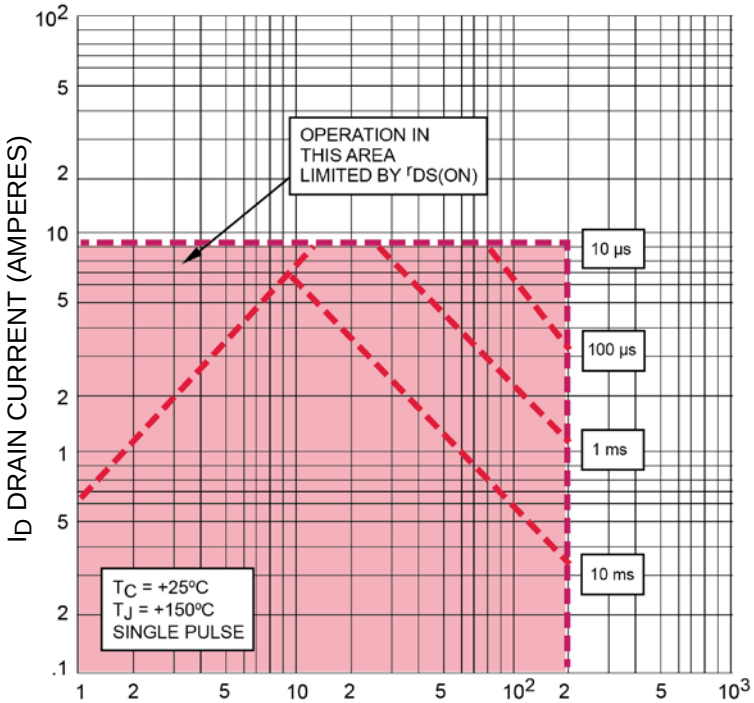


For 2N6786U

GRAPHS (continued)

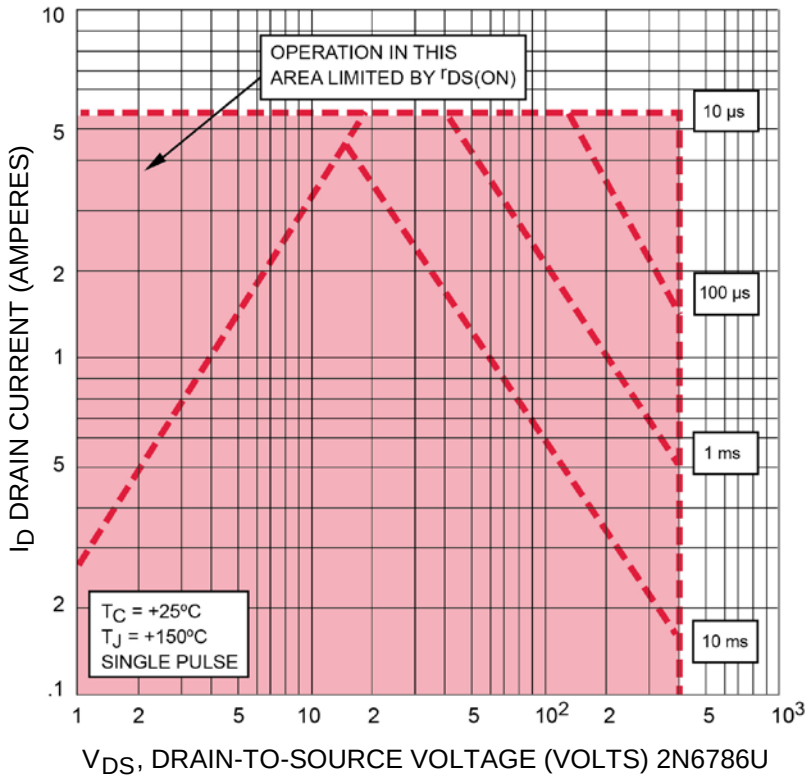
FIGURE 3 – Maximum Safe Operating Area



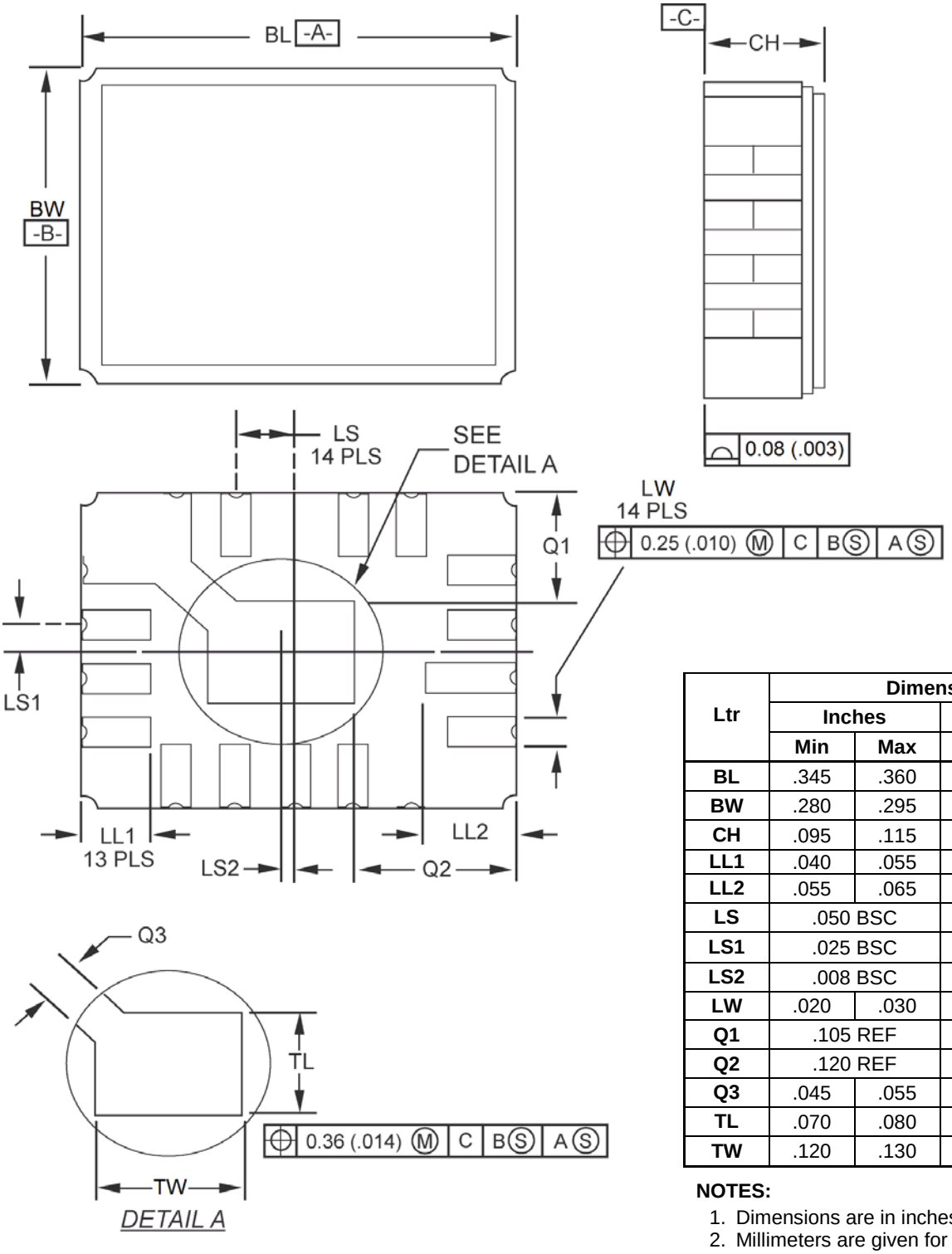


GRAPHS (continued)

FIGURE 3 – Maximum Safe Operating Area



PACKAGE DIMENSIONS

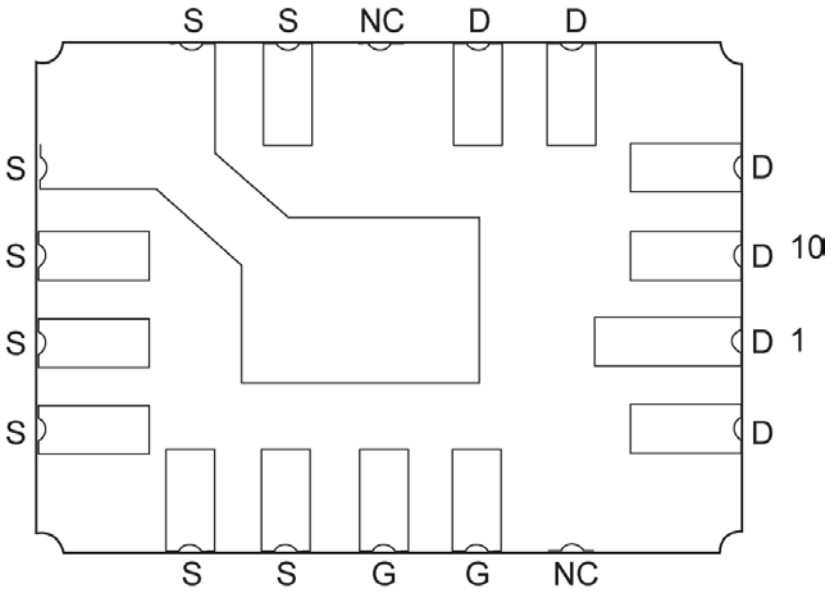


Ltr	Dimensions			
	Inches		Millimeters	
	Min	Max	Min	Max
BL	.345	.360	8.77	9.14
BW	.280	.295	7.12	7.49
CH	.095	.115	2.42	2.92
LL1	.040	.055	1.02	1.39
LL2	.055	.065	1.40	1.65
LS	.050 BSC		1.27 BSC	
LS1	.025 BSC		0.635 BSC	
LS2	.008 BSC		0.203 BSC	
LW	.020	.030	0.51	0.76
Q1	.105 REF		2.67 REF	
Q2	.120 REF		3.05 REF	
Q3	.045	.055	1.14	1.40
TL	.070	.080	1.78	2.03
TW	.120	.130	3.05	3.30

NOTES:

1. Dimensions are in inches.
2. Millimeters are given for general information only.
3. In accordance with ASME Y14.5M, diameters are equivalent to Φx symbology.
4. Ceramic package only.

PAD LAYOUT



PAD ASSIGNMENTS