UM2163
User manual

Getting started with the STEVAL-IME011V2 evaluation board based on the STHV748S ultrasound pulser

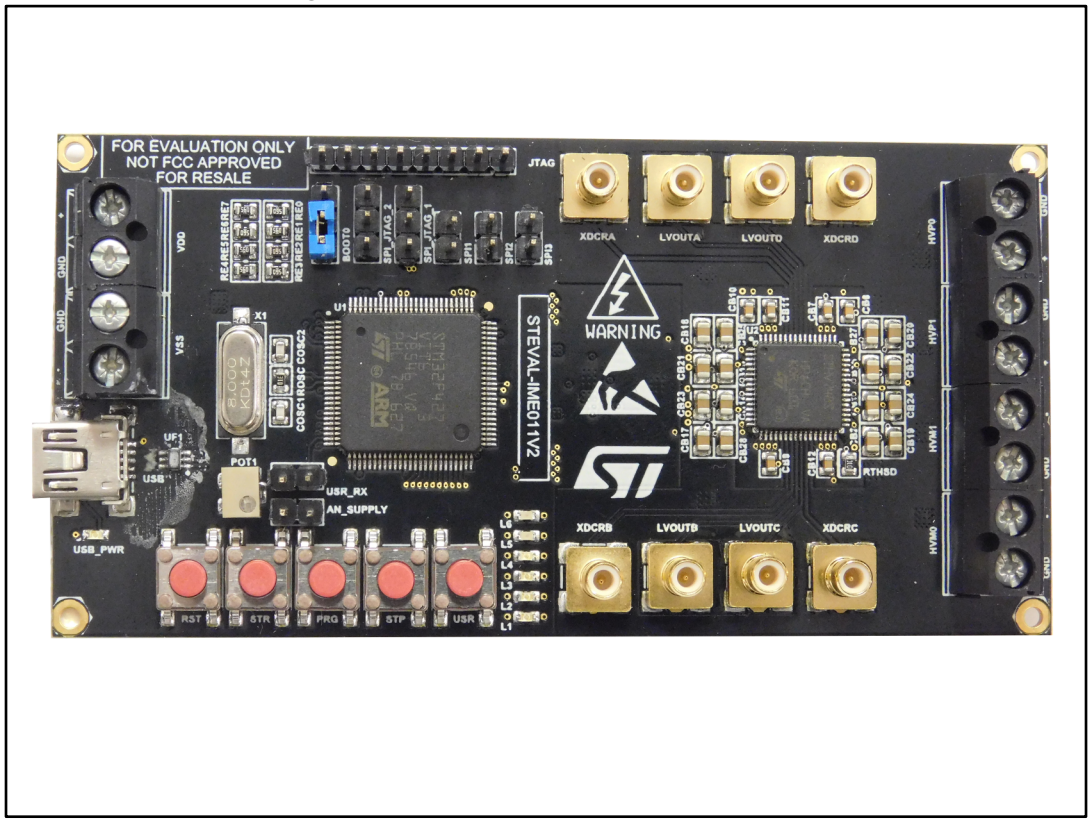
Introduction

The STEVAL-IME011V2 evaluation board is designed around the STHV748S 4-channel 5-level high voltage pulser, a state-of-the-art device designed for ultrasound imaging applications.

This board facilitates evaluation of the ultrasound pulser IC thanks also a new graphical user interface.

Once configured, the output waveforms can be displayed directly on an oscilloscope by connecting the probe to the relative BNCs.

Figure 1: STEVAL-IME011V2 evaluation board



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1 Board features

- 4-channel outputs: high voltage and low voltage BNC connectors
- Up to 4 memory locations to store own waveforms designs
- USB connector to load own waveforms onto the board
- Dedicated connectors to supply high voltage and low voltage to the STHV748S output stage
- 4-key button rapid preferred program selection
- RoHS compliant

2 Getting started

The STEVAL-IME011V2 is shipped by STMicroelectronics ready to use. The user only needs to:

1. Plug the power supply to the board
2. Connect the BNCs to the oscilloscope (see *Section 3.1: "Power supply"* for details)
3. Check LED PROGRAM 1 (LD1) turns on
4. Select the waveform with the PROGRAM button
   The corresponding PROGRAM LED (LD1-LD4) turns on
5. Press the START button to run the selected program
   The START LED (L5) turns on.
   When the program ends, L5 LED turns off
6. If a continuous wave program is selected, the STOP button must be pressed to stop program execution and the STOP LED (L5) turns off
7. To run the same program again, restart from step 5. To run another program, restart from step 4
   An overvoltage protection mechanism suspends pattern generation if the HV supply exceeds 90 V and the red LED (L6) switches on. Pattern generation restarts as soon as the HV supply voltage falls back into the allowed range.

3 Hardware layout and configuration

The STEVAL-IME011V2 evaluation board is designed around the STHV748S.

Figure 2: Connection between STM32F4 and STHV748S

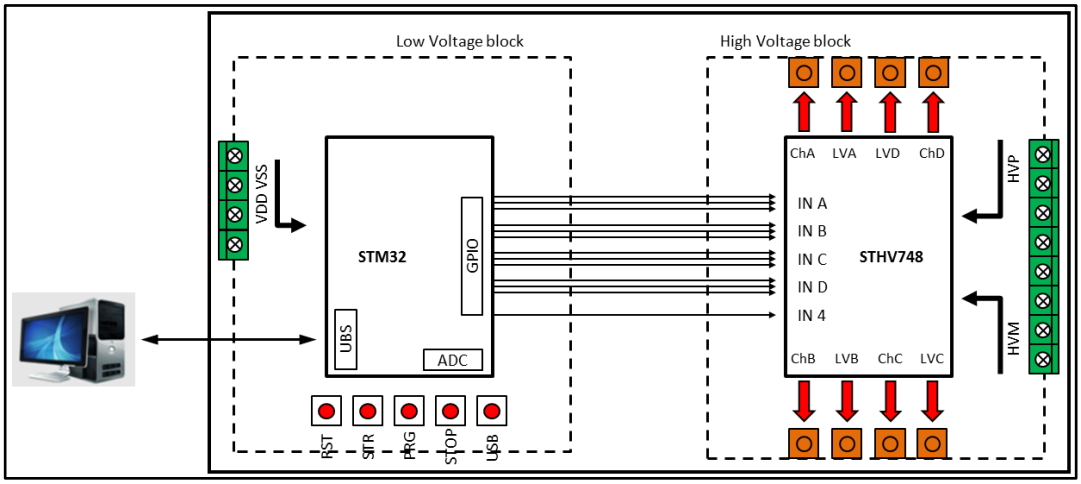
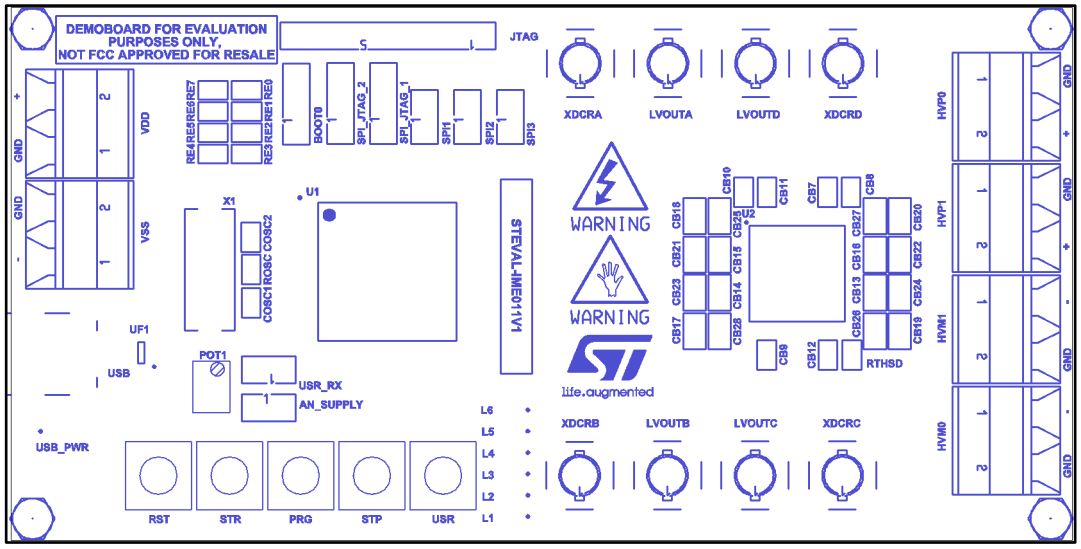


Figure 3: STEVAL-IME011V2 board layout



3.1 Power supply

The STEVAL-IME011V2 low voltage block is designed to be powered:

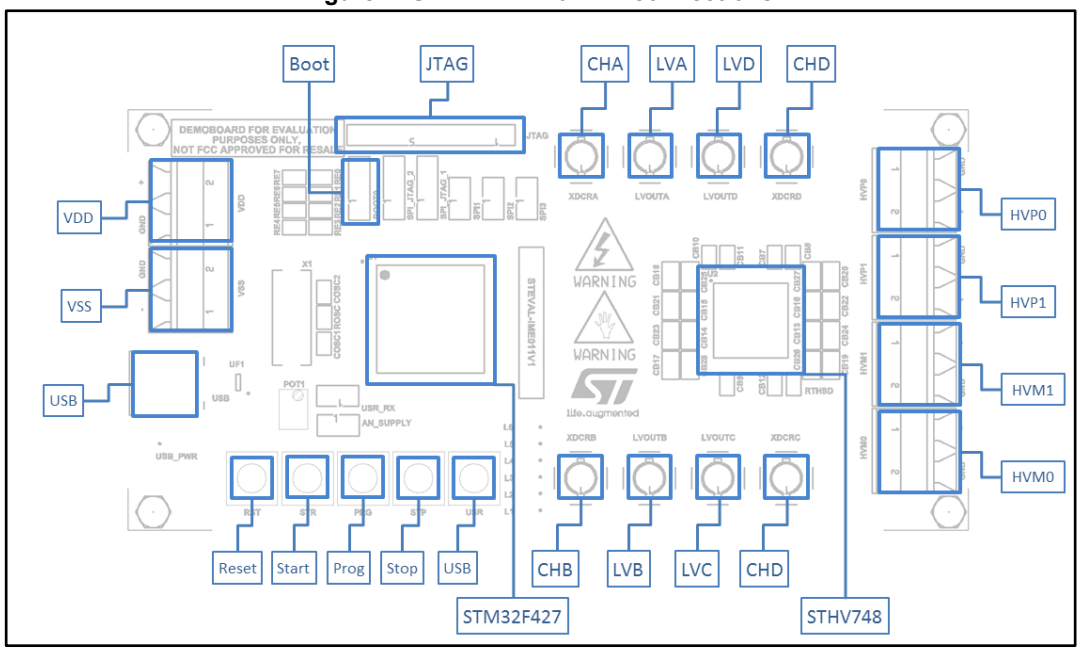
- during programming and when the board is connected to a PC:
  - 5 V DC through a USB Mini B connector to supply the STM32F4
- during pattern generation and when high voltage is powered on:
  - 5 V DC connected to VDD to supply STM32F4 and STHV748S through an LDO
  - -5 V DC connected to VSS to supply STHV748S through an LDO

The USB connector must be removed when high voltage is powered on.

The STEVAL-IME011V2 high voltage block is designed to be powered:

- VDD: positive supply voltage, 5 V (2 - VDD conn.)
- GND: ground (1 – VDD conn. And 2 – VSS conn.)
- VSS: negative supply voltage 5 V (1 - VSS conn.)
- GND: ground (1 – HVP0 conn.)
- HVP0: TX0 high voltage positive supply (2 - HVP0 conn.)
- GND: ground (1 – HVP1 conn.)
- HVP1: TX1 high voltage positive supply (2 - HVP1 conn.)
- HVM1: TX1 high voltage negative supply (1 - HVM1 conn.)
- GND: ground (2 - HVM1 conn.)
- HVM0: TX0 high voltage negative supply (1 - HVM0 conn.)
- GND: ground (2 – HVM0 conn.)

Figure 4: STEVAL-IME011V2 connections



3.2 MCU

The STM32F427 is fully dedicated to generate the bitstream on its GPIO pins to drive the pulser output channels. It is already pre-programmed as a DFU (device firmware upgrade) with the ability of upgrading internal Flash memory.

The STM32F427 manages all the DFU operations, such as the authentication of product identifier, vendor identifier and firmware version. The MCU drives the pulser channels through the use of different GPIO pins. You can simultaneously drive from 1 to 16 different pins by simply writing a 16-bit word into the GPIO output data register (ODR).

The board can be connected to a PC via USB. The required pattern is sent as a sequence of states for each pulser channel and for each state duration (expressed in units of MCU system clock cycle).

Once the information is received, the channel states are converted into 16-bit words for the GPIO peripheral and they are stored in the embedded Flash, with the timing information. After programming, the PC is no longer required, so the board becomes a stand-alone device.

Different patterns can be stored and you can select the one to use at run-time.

The same MCU can implement two different solutions for real-time execution.

The first solution involves the use of the STM32 direct memory access (DMA) peripheral, which can transfer data from memory to any peripheral register, GPIO included, without the intervention of the MCU core.

To trigger DMA transfer, a general purpose timer is used, that works at the system clock frequency and basically acts as a counter: the reload value (the value at which the counter returns to zero) is stored in the auto reload register (ARR).

The timer triggers two different DMA channels in two different moments:

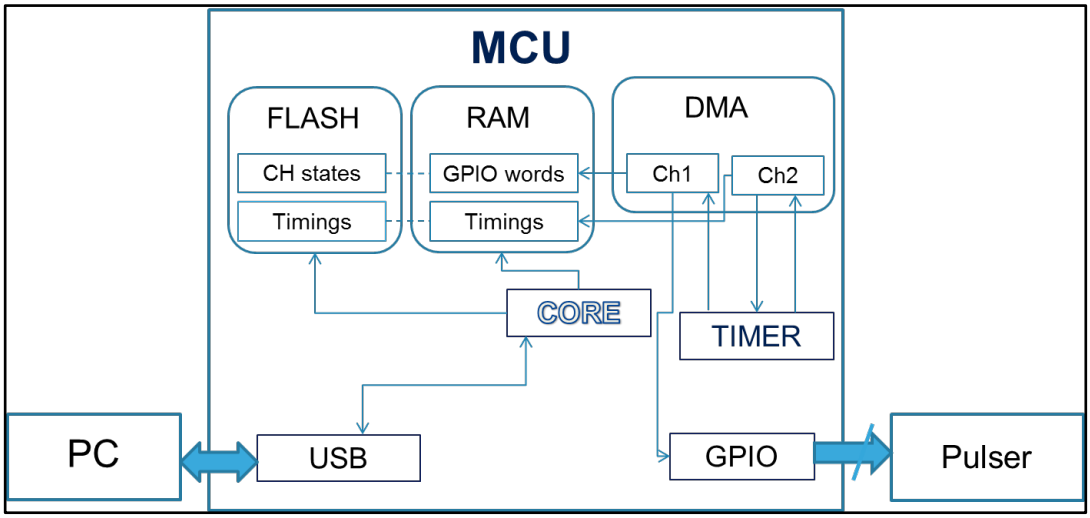
- the first channel is triggered at each reload event and transfers the new GPIO word to the ODR;
- the second is triggered at a constant time after reload and transfers the new duration information to the ARR

The timer preload feature is enabled, so that the new ARR value is effective only at the next reload. Since the time needed by the first DMA channel to update the ODR is a constant, considering the reload trigger as a starting point, the time between two different GPIO updates is simply given by the ARR value.

The DMA circular buffer feature can be enabled to allow automatic regeneration of the same pattern at each end. This solution has the advantage of being fully managed by hardware, thus, the MCU core is completely free for any user requirement.

The main drawback is that each timing value between two subsequent states cannot be lower than a minimum value to guarantee enough time for both DMA channels to perform their transfers.

Figure 5: Solution 1 with STM32 direct memory access (DMA) peripheral



The second solution is designed to overcome the DMA minimum duration requirement and directly involves the MCU core:

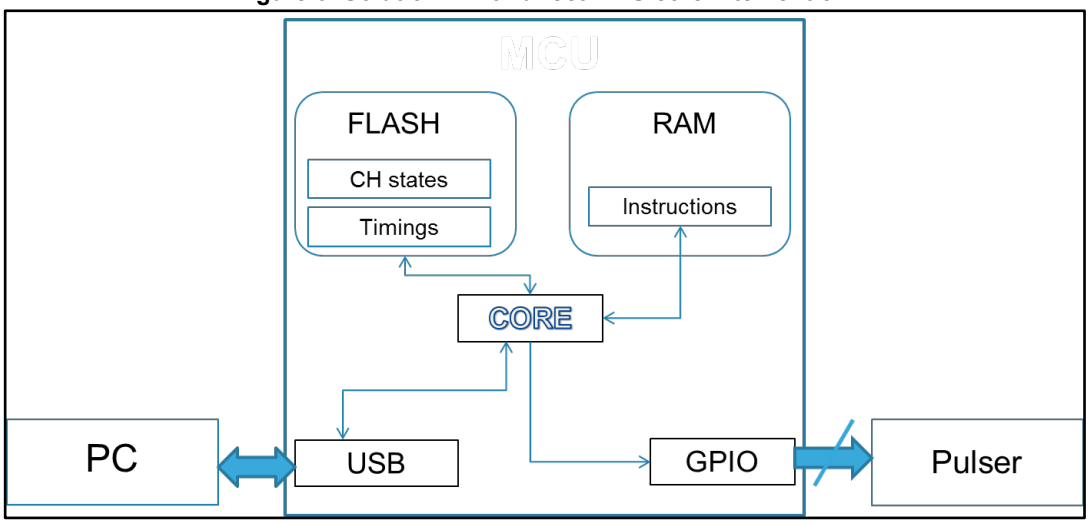
- during run-time, the core generates the binary assembly code it needs to load and store each word in the ODR. Any unnecessary instructions like control loops are avoided; the code is only a succession of simple load/store instructions;

- to adapt the timing to the pattern needs, dummy instructions are inserted in the assembly code. To avoid wasting time to load each word from memory, the word is inserted as a literal in the assembly instruction itself, which means that a 32-bit instruction is needed instead of an equivalent 16-bit;
- to avoid any latency due to the instruction fetch from Flash, the code is executed from the embedded RAM. Moreover, the RAM is configured to be accessed by the core through a different bus to the one used to access the ODR.

Thanks to this solution, it is possible to achieve a minimum time of two system clock cycles before two updates and maintain one system clock cycle resolution. For instance, if you consider a STM32F4 clocked at 168 MHz, the minimum timing you can achieve is 12 ns and you can set the duration of each state with a resolution of 6 ns. For a repetitive pattern, a branch instruction is added at the end of the routine to restart the pattern generation. In this case, the clock cycles needed for the branch instruction has to be considered for the last state.

The main drawback of this solution is that the MCU core is 100% involved in the pattern generation even though it can still be called by peripheral interrupts and stop pattern generation to perform other tasks.

Figure 6: Solution 2 with direct MCU core intervention



3.3 Stored patterns

The STEVAL-IME011V2 can store four different patterns in the MCU Flash memory to demonstrate the achievable performance at the pulser outputs.

Four selectable programs already stored in STM32 Flash memory form the default set which is available and ready to use (flagged by L1 to L4 LEDs).

Program 1:

- XDCR_A: pulse wave mode, TX0 switching, 5 pulses, time-period TP = 400 ns and PRF = 150 µs
- XDCR_B: pulse wave mode, TX0 switching, 5 pulses in counter phase respect to XDCR_A, time-period TP = 400 ns and PRF = 150 µs
- XDCR_C: pulse wave mode, TX1 switching, 5 pulses, time-period TP = 200 ns and PRF = 150 µs
- XDCR_D: pulse wave mode, TX1 switching, 5 pulses in counter phase with respect to XDCR_C, time-period TP = 200 ns and PRF = 150 µs

TX0 indicates that the H-bridge is supplied by HVP/M0, while TX1 indicates that the H-bridge is supplied by HVP/M1.

Figure 7: Program 1 scheme

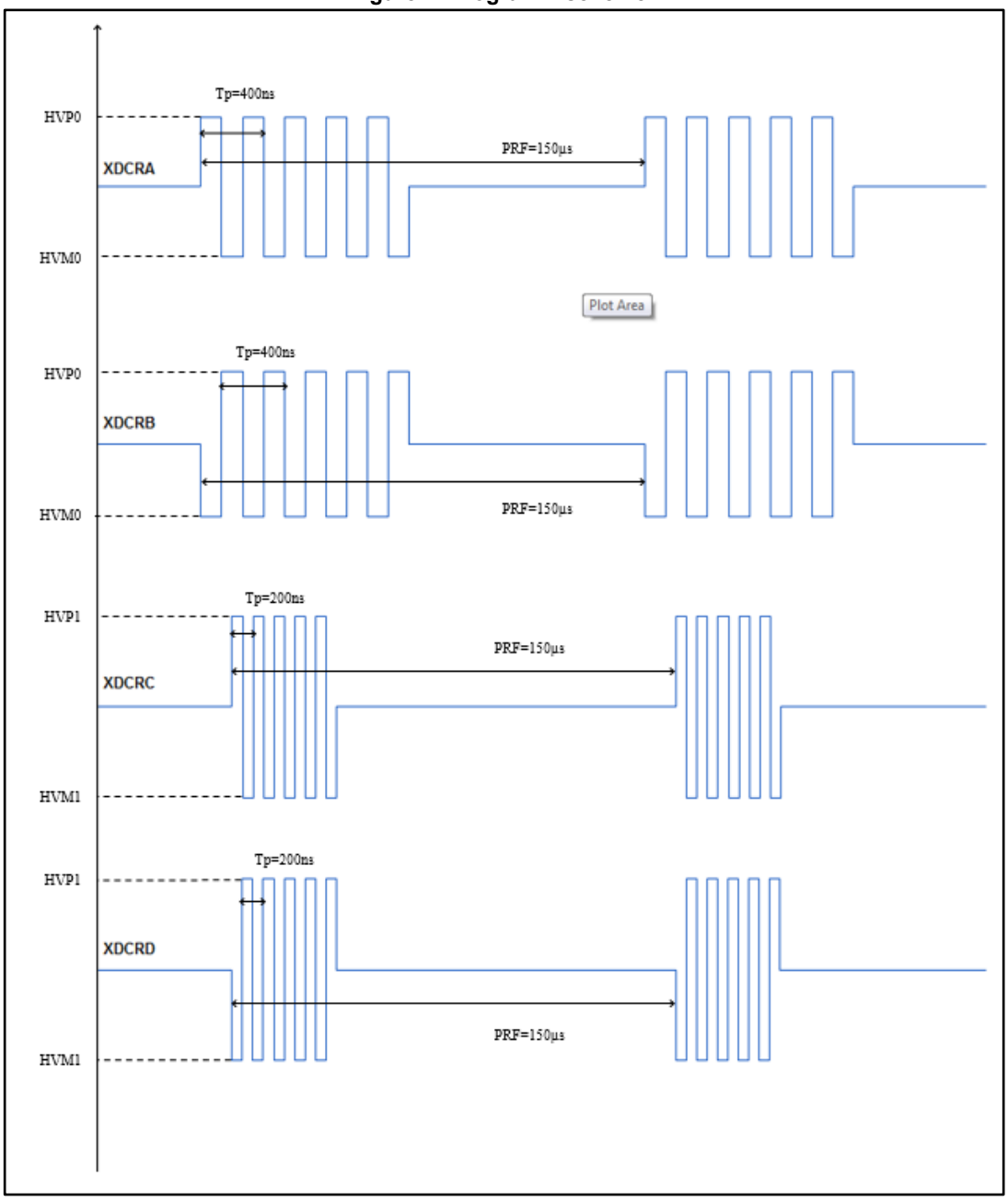
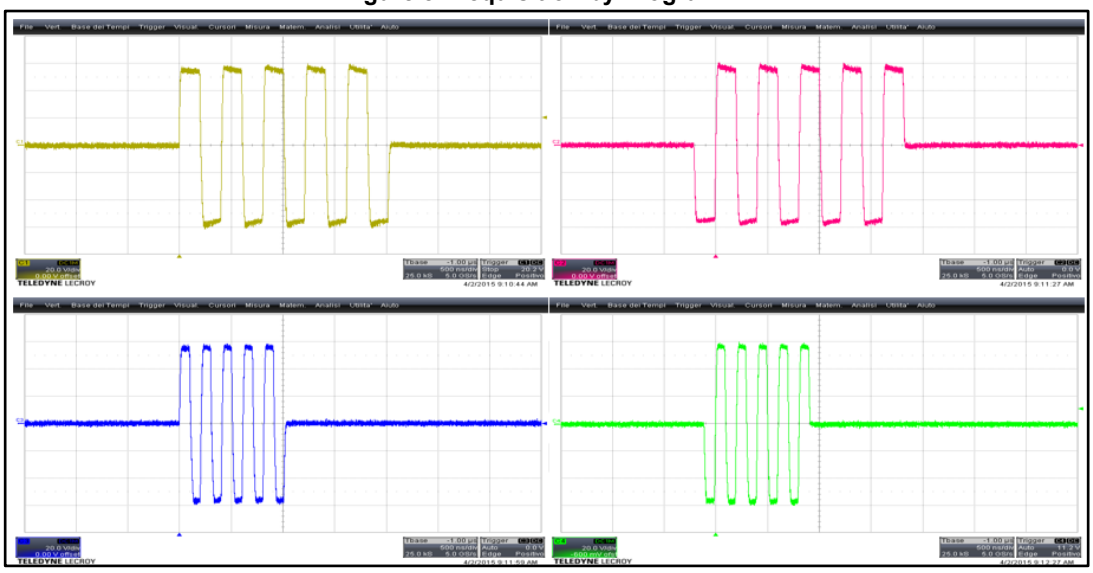


Table 1: Program 1

PW 5 pulses - HV0/1 = ± 60 V; LOAD: 270 pF//100 Ω						
	Mode	**Frequency (MHz)**	**Number of pulses**	**Initial pulse**	**H-bridge**	**PRF**
Ch A	PW	2.5	5	positive	TX0	150 µs
Ch B	PW	2.5	5	negative	TX0	150 µs
Ch C	PW	5	5	positive	TX1	150 µs
Ch D	PW	5	5	negative	TX1	150 µs

Figure 8: Acquisition by Program 1



Program 2:

- XDCR_A: pulse wave mode, TX0 switching, 5 pulses, time-period TP = 200 ns and PRF = 150 µs
- XDCR_B: pulse wave mode, TX0 switching, 5 pulses in counter phase with respect to XDCR_A, time-period TP = 200 ns and PRF =150 µs
- XDCR_C: pulse wave mode, TX1 switching, 5 pulses, time-period TP = 100 ns and PRF = 150 µs
- XDCR_D: pulse wave mode, TX1 switching, 5 pulses in counter phase with respect to XDCR_C, time-period TP = 100 ns and PRF = 150 µs

Figure 9: Program 2 scheme

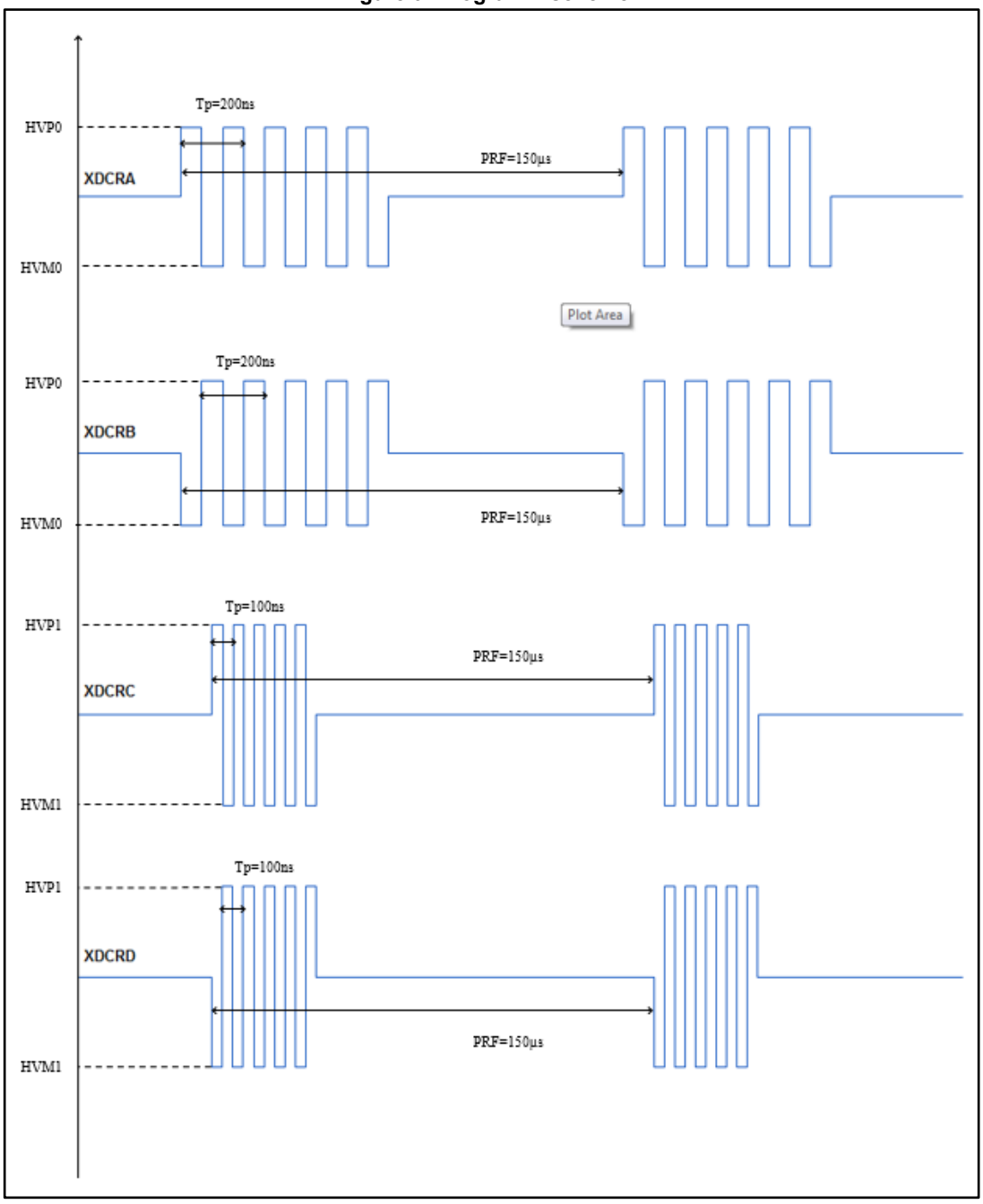
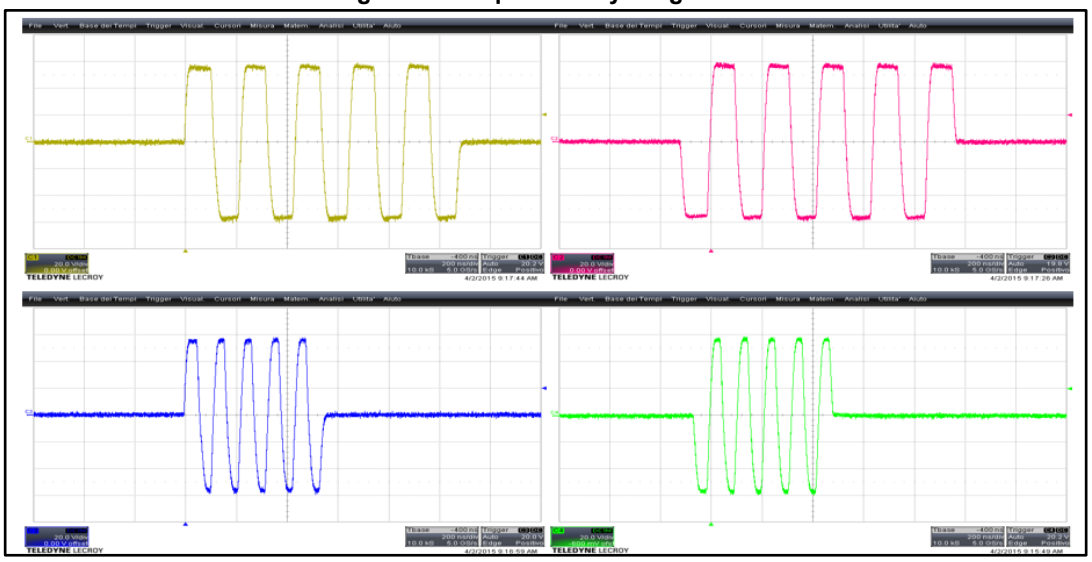


Table 2: Program 2

PW TX0 & TX1 5 pulses - HV0/1 = ± 60 V; LOAD: 270 pF//100 Ω						
	Mode	**Frequency (MHz)**	**Number of pulses**	**Initial pulse**	**H-bridge**	**PRF**
Ch A	PW	5	5	positive	TX0 & TX1	150 µs
Ch B	PW	5	5	negative	TX0 & TX1	150 µs
Ch C	PW	10	5	positive	TX0 & TX1	150 µs
Ch D	PW	10	5	negative	TX0 & TX1	150 µs

Figure 10: Acquisition by Program 2



Program 3:

- XDCR_A: continuous wave mode, TX-CW switching, time-period TP = 400 ns
- XDCR_B: continuous wave mode, TX-CW switching in counter-phase respect to XDCR_A, time-period TP = 400 ns
- XDCR_C: continuous wave mode, TX-CW switching, time-period TP =200 ns
- XDCR_D: continuous wave mode, TX-CW switching in counter-phase with respect to XDCR_C, time-period TP = 200 ns

Figure 11: Program 3 scheme

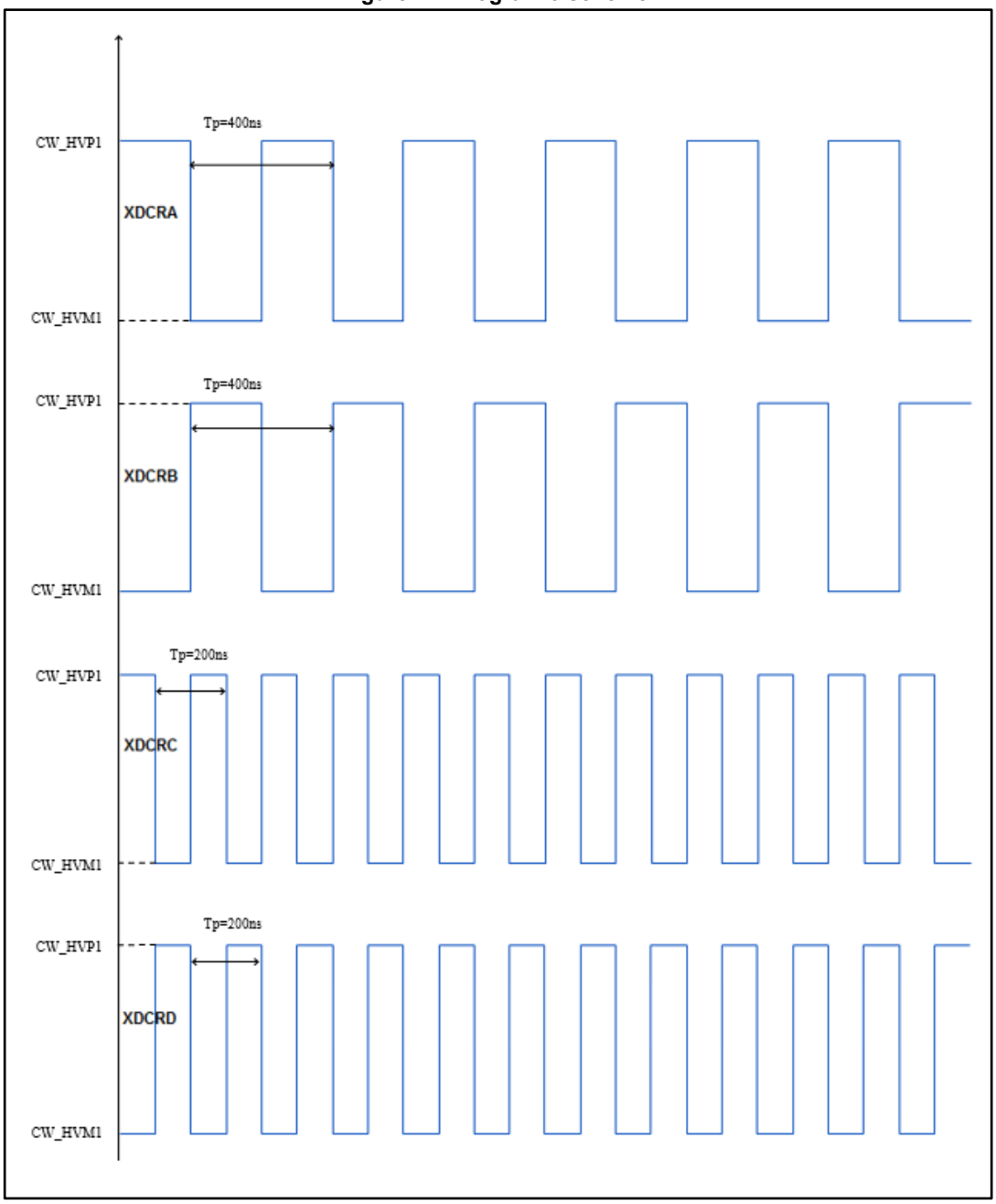
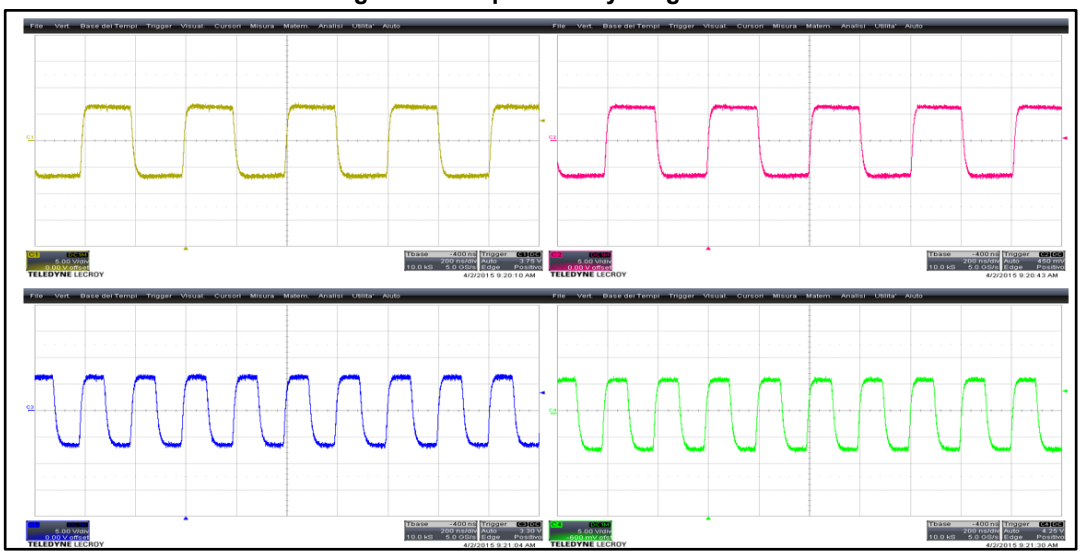


Table 3: Program 3

Continuous wave - HV1=±10V; LOAD: 270 pF//100 Ω					
	Mode	**Frequency (MHz)**	**Number of pulses**	**Initial pulse**	**H-bridge**
Ch A	CW	2.5	continuous wave	positive	TX-CW
Ch B	CW	2.5	continuous wave	negative	TX-CW
Ch C	CW	5	continuous wave	positive	TX-CW
Ch D	CW	5	continuous wave	negative	TX-CW

Figure 12: Acquisition by Program 3



Program 4:

- XDCR_A: pulse wave mode, TX0 switching, 1.5 pulses, time-period TP =400 ns and consequently TX1 switching, 5 pulses, time period TP = 200 ns and PRF = 150 µs
- XDCR_B: pulse wave mode, TX0 switching, 1.5 pulses, time-period TP = 400 ns and consequently TX1 switching, 5 pulses, time-period TP = 200 ns and PRF = 150 µs
- XDCR_C: pulse wave mode, TX0 switching, 1.5 pulses, time-period TP = 200 ns and consequently TX1 switching, 5 pulses, time-period TP =200 ns and PRF=150 µs
- XDCR_D: pulse wave mode, TX0 switching, 1.5 pulses, time-period TP = 200 ns and consequently TX1 switching, 5 pulses, time-period TP = 200 ns and PRF = 150 µs

Figure 13: Program 4

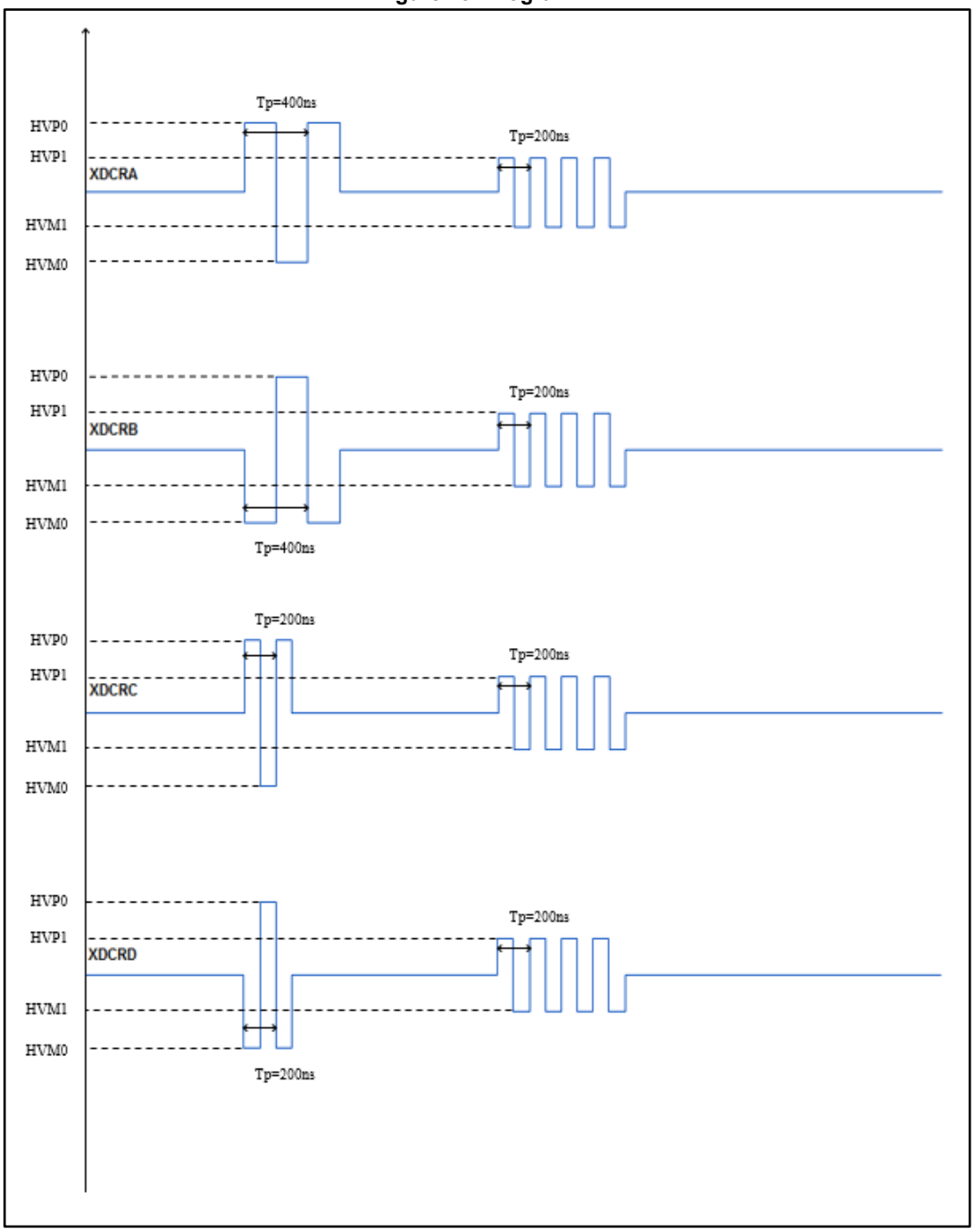
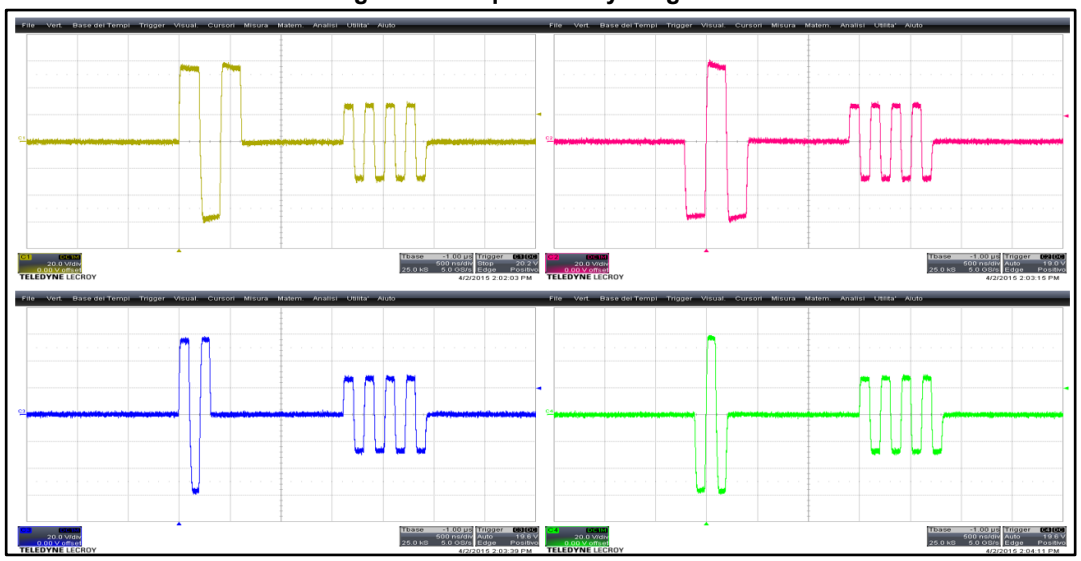


Table 4: Program 4

Pulse cancellation - HV0/1 = ±60 V; LOAD: 270 pF//100 Ω						
	Mode	**Frequency (MHz)**	**Number of pulses**	**Initial pulse**	**H-bridge**	**PRF**
Ch A	PW	2.5 - 5	3 half pulse then 4 pulse	positive	TX0 then TX1	150 µs
Ch B	PW	2.5 - 5	3 half pulse then 4 pulse	negative	TX0 then TX1	150 µs
Ch C	PW	5	3 half pulse then 4 pulse	positive	TX0 then TX1	150 µs
Ch D	PW	5	3 half pulse then 4 pulse	negative	TX0 then TX1	150 µs

Figure 14: Acquisition by Program 4



The board can be connected to a PC via a USB cable and patterns can be edited through a user interface.

The USB cable must be removed when a high voltage is connected to the board.

3.4 STHV748S stage

The STHV748S high-voltage, high-speed ultrasound pulser features four independent channels. It is designed for medical ultrasound applications, but can also be used for other piezoelectric, capacitive or MEMS transducers.

The device contains:

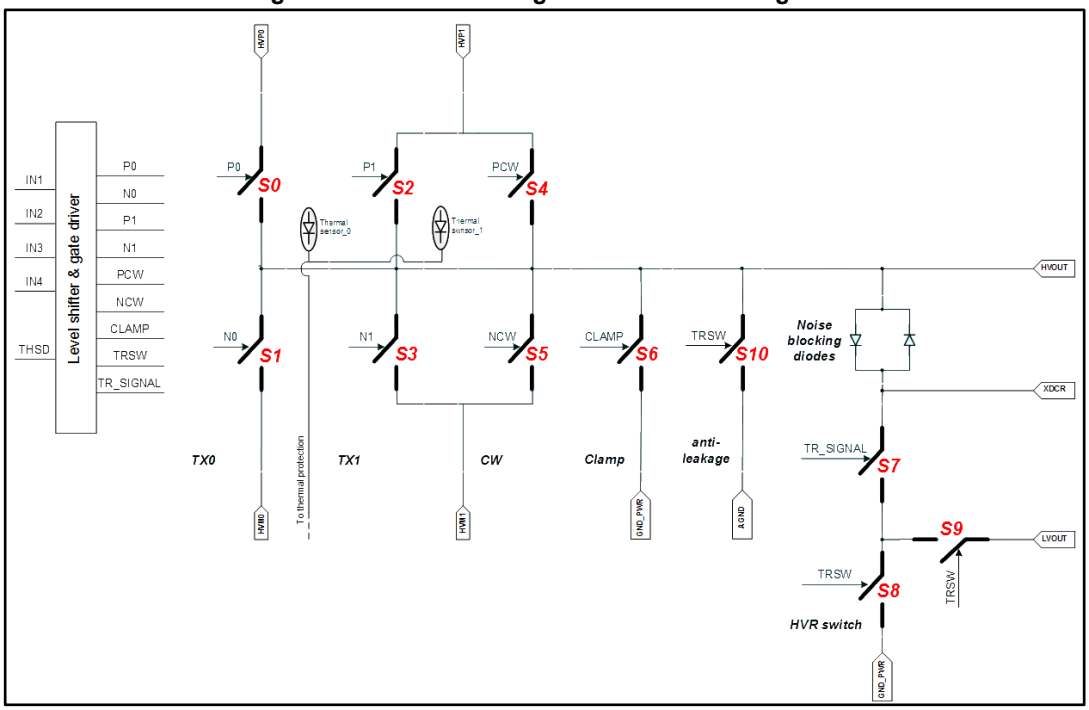
- a controller logic interface circuit
- level translators
- MOSFET gate drivers

- noise blocking diodes
- high-power P-channel and N-channel MOSFETs as output stages for each channel
- clamping-to-ground circuitry
- anti-leakage
- anti-memory effect block
- a thermal sensor
- an HV receiver switch (HVR_SW), which guarantees strong decoupling during the transmission phase
- self-biasing and thermal shutdown blocks (see *Figure 15: "STHV748S single channel block diagram"*)

Each channel can support up to five active output levels with two half bridges. Each channel output stage is able to provide a ±2 A peak output current; to reduce power dissipation during continuous wave mode, the peak current is limited to 0.6 A (a dedicated half bridge is used).

For further information, please refer to the STHV748S datasheet.

Figure 15: STHV748S single channel block diagram



STHV748S output waveforms can be directly displayed for each channel Ch A/B/C/D using an oscilloscope by connecting the scope probe to the XDCRA, XDCRB, XDCRC and XDCRD SMB connectors. Moreover, pulser outputs are connected to the onboard equivalent load, a 270 pF 200 V capacitor paralleled with a 100 Ω, 2 W resistor. A coaxial cable can also be used to easily connect the user transducer; in this case, the equivalent load should be removed from the board. Furthermore, four low voltage outputs are available to receive the echo signal coming from the piezo-element through HVR_SW (LVOUTA, LVOUTB, LVOUTC, LVOUTD).

The main issues in this PCB design are the capacitance values necessary to ensure good filtering and the effective decoupling between the low voltage inputs (IN1, IN2, IN3, IN4 and EN for each channel) and the HV switching signals (XDCR, HVOUT, etc.), which is ensured by the implemented layer separation.

3.5 Operating supply conditions

Table 5: DC working supply conditions

Operating supply voltages					
Symbol	**Parameter**	**Min.**	**Typ.**	**Max.**	**Value**
V_{DD}	Positive supply voltage	5	6	10	V
V_{SS}	Negative supply voltage	-5	6	-10	V
HVP0	TX0 high voltage positive supply			95	V
HVP1	TX1 high voltage positive supply			95	V
HVM0	TX0 high voltage negative supply	-95			V
HVM1	TX1 high voltage negative supply	-95			V

The high voltage pins must be HVP0 ≥ HVP1 and HVM1 ≥ HVM0

4 Connectors

4.1 Power supply

The STEVAL-IME011V2 evaluation board is powered through the screw connectors shown in the following figures.

Figure 16: Power supply connector VDD (+5V - GND)

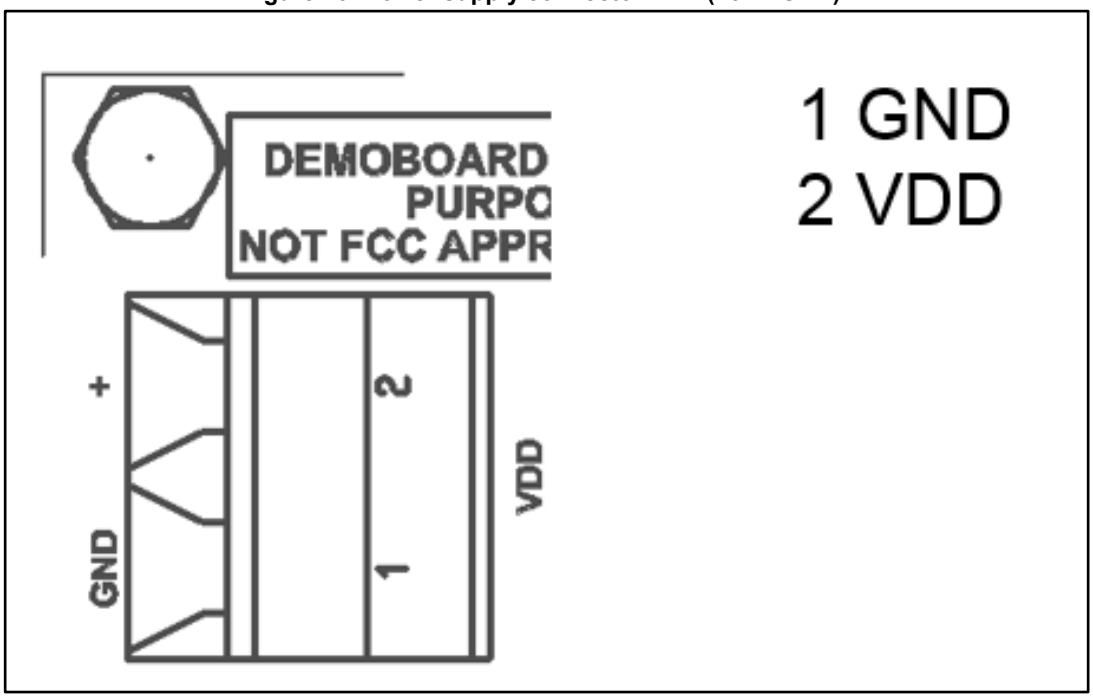


Figure 17: Power supply connector VSS (GND - -5V)

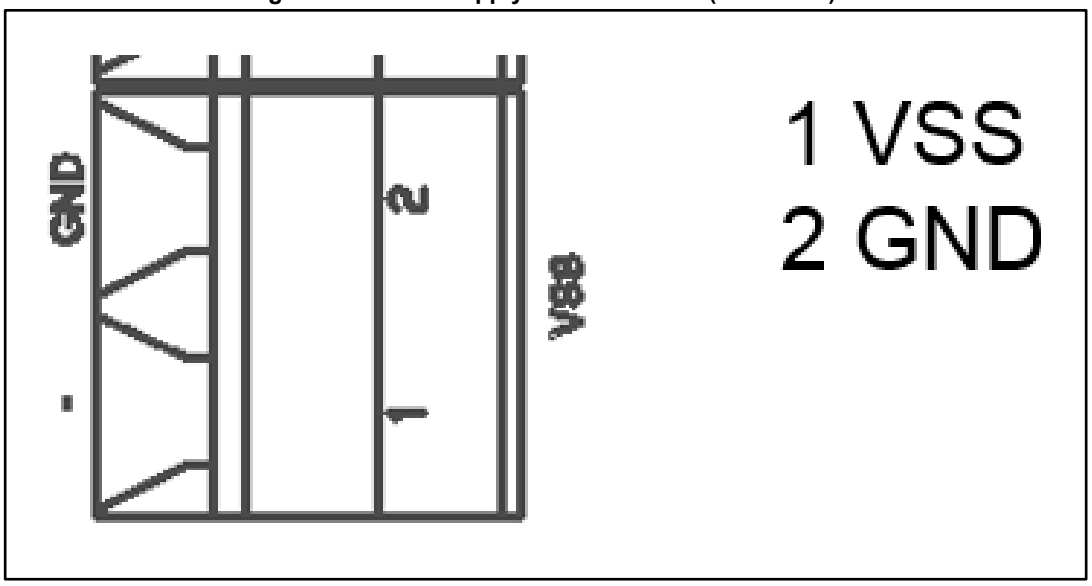
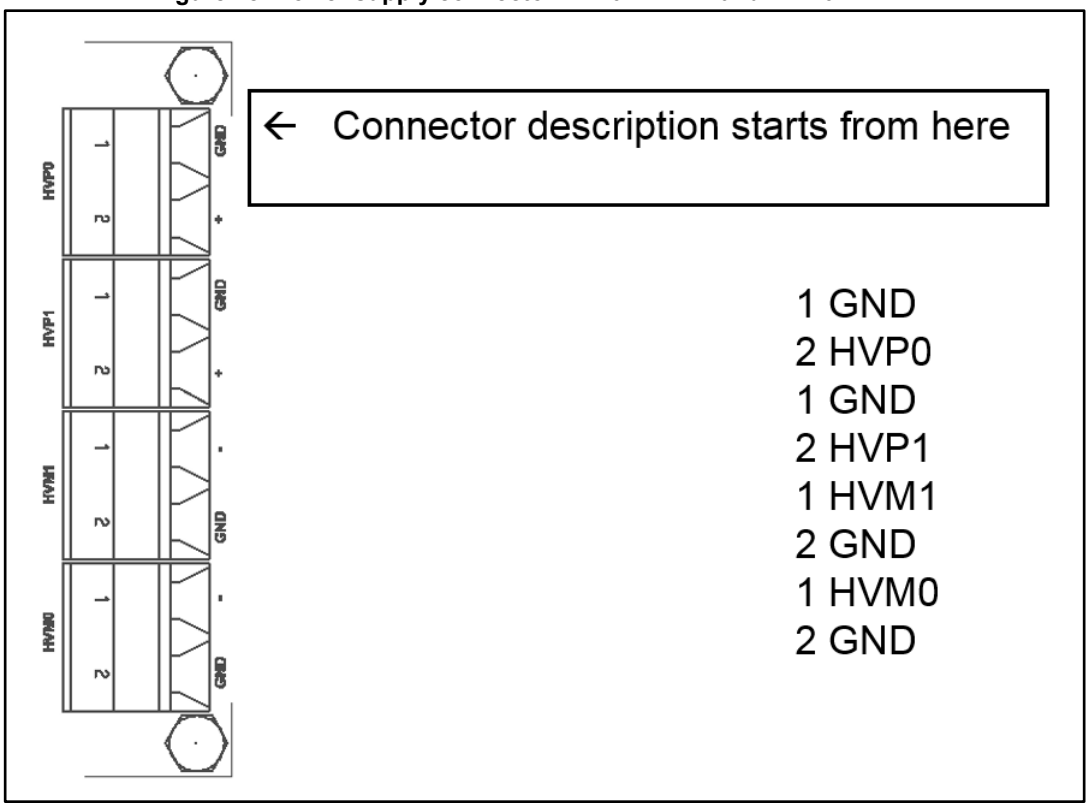


Figure 18: Power supply connector HVP0 – HVP1 and HVM0 – HVM1



4.2 MCU

Figure 19: USB mini-B connector (CN1)

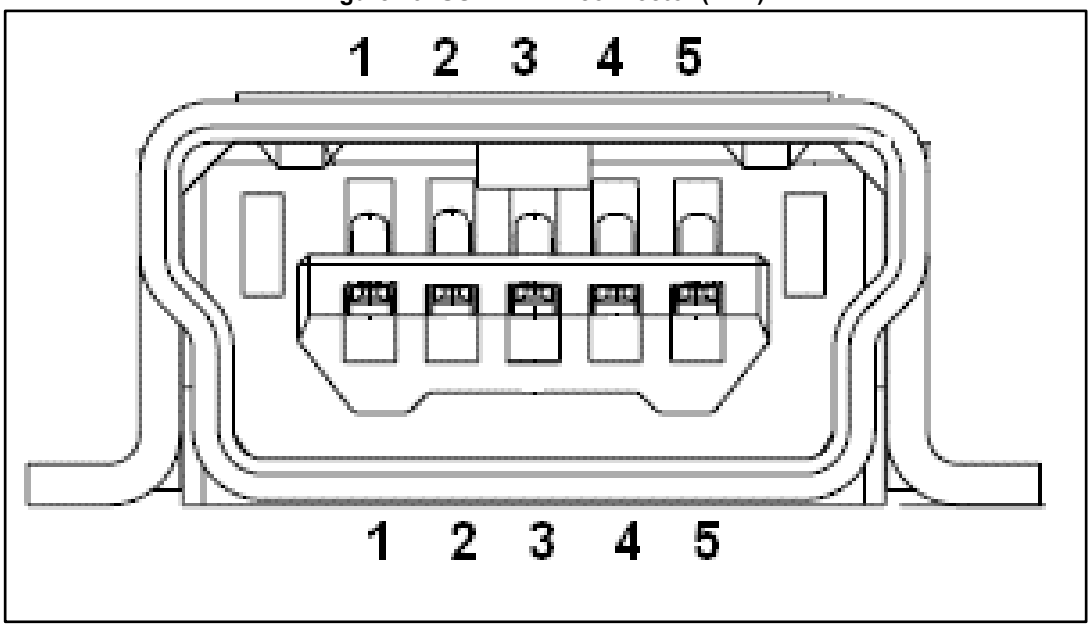


Table 6: USB mini B connector pinout

Pin number	Description
1	Vbus (power)
2	DM (STM32 PA11)
3	DP (STM32 PA12)
4	N.C.
5	Ground

Figure 20: JTAG connector

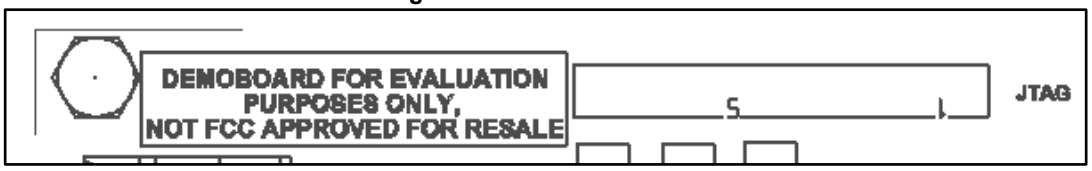


Table 7: JTAG connector pinout

Pin number	Description
1	DVDD
2	JTDI
3	JTMS
4	JTCK
5	JTDO
6	JRST
7	GND
8	NRST

Figure 21: Boot connector

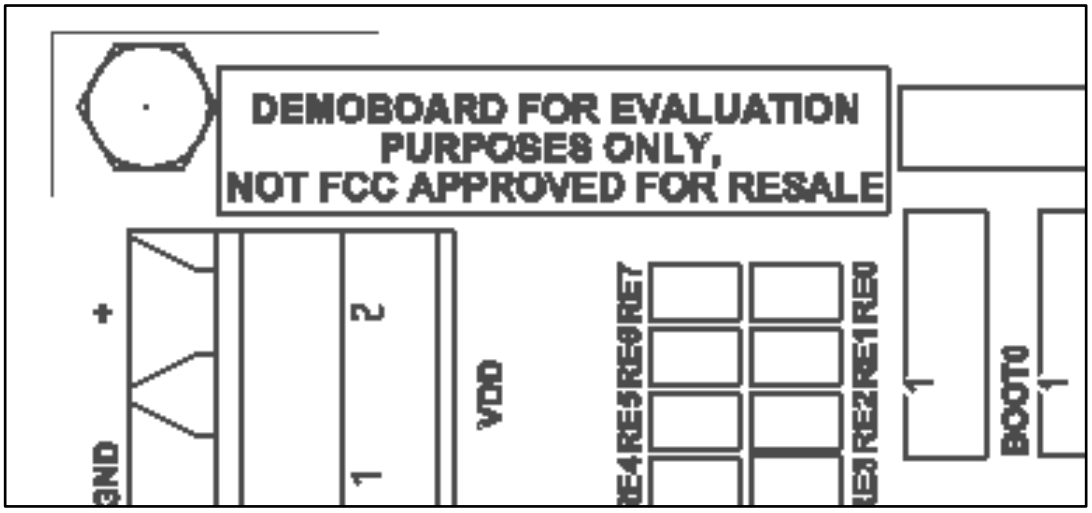
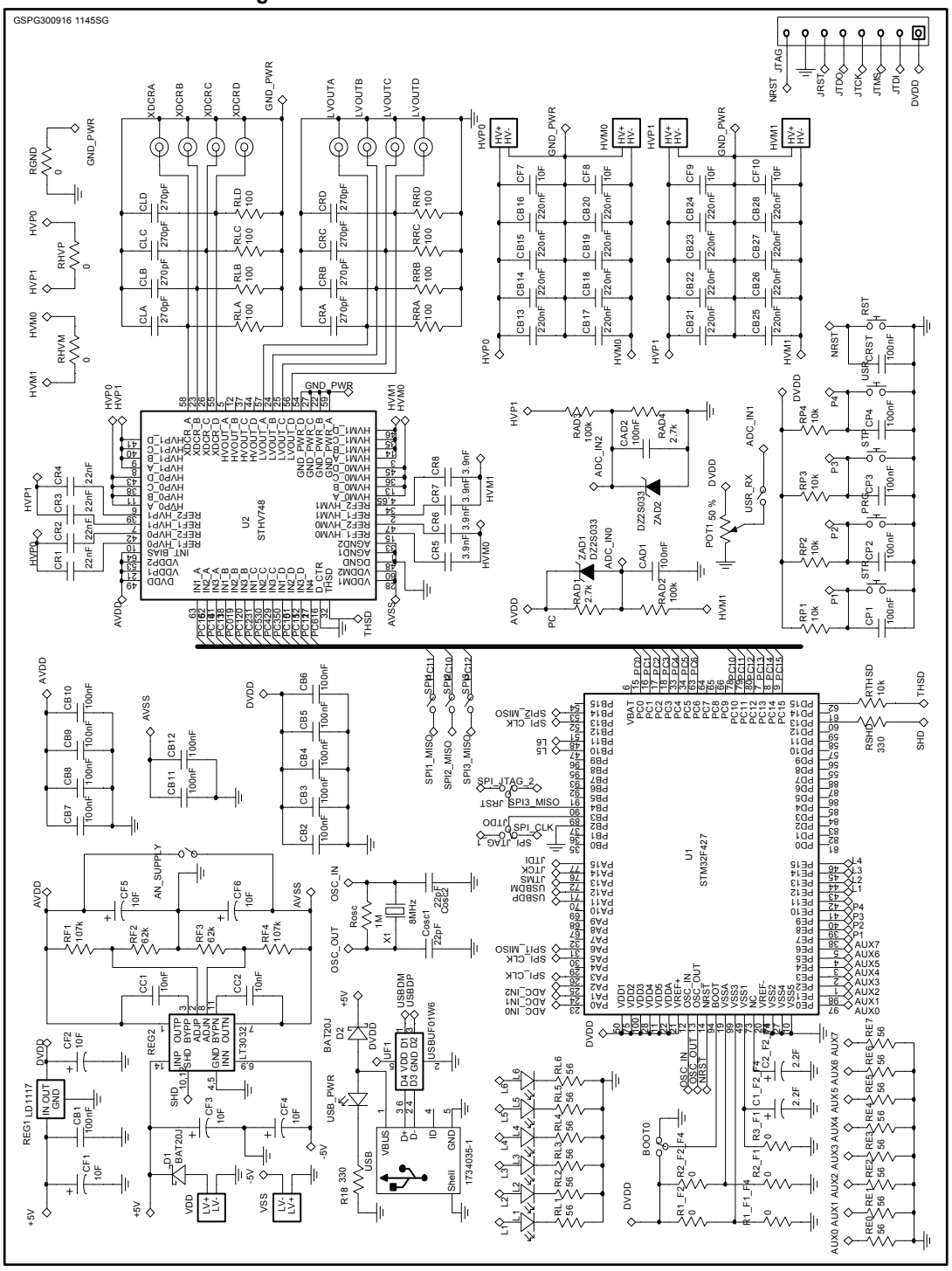


Table 8: Boot connector pinout

Pin number	Description
1	GND
2	BOOT0 (boot from flash memory)
3	DVDD (DFU mode)

5 Schematic diagrams

Figure 22: STEVAL-IME011V2 circuit schematic



6 PCB layout

Figure 23: Top layer

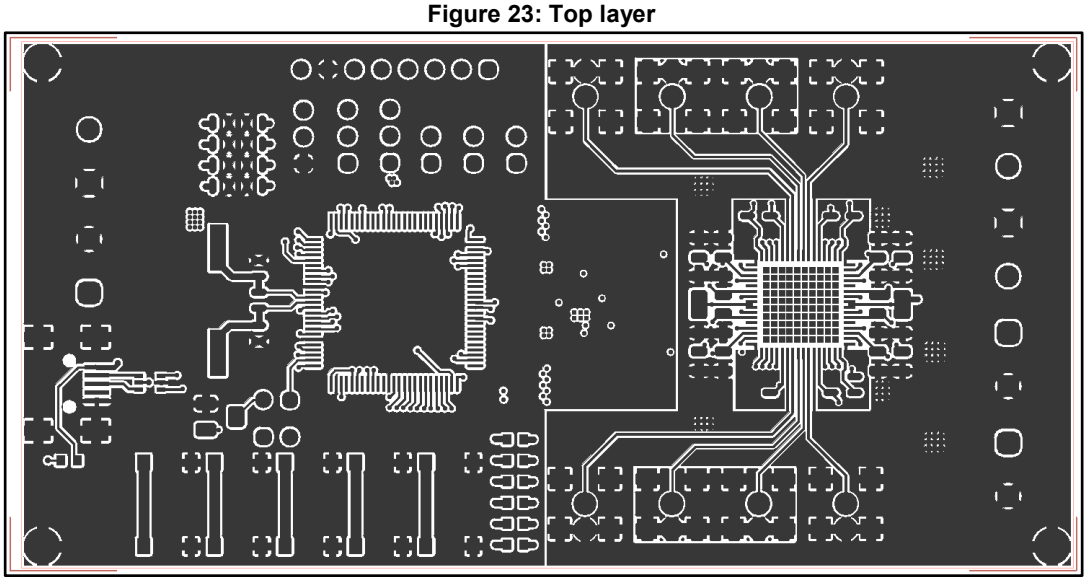


Figure 24: Inner layer 1

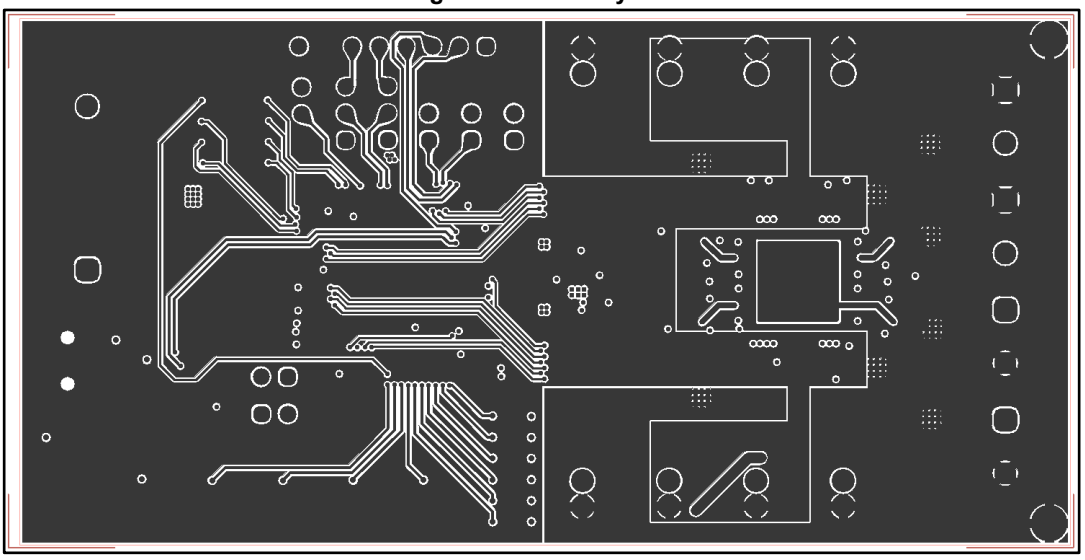


Figure 25: Inner layer 2

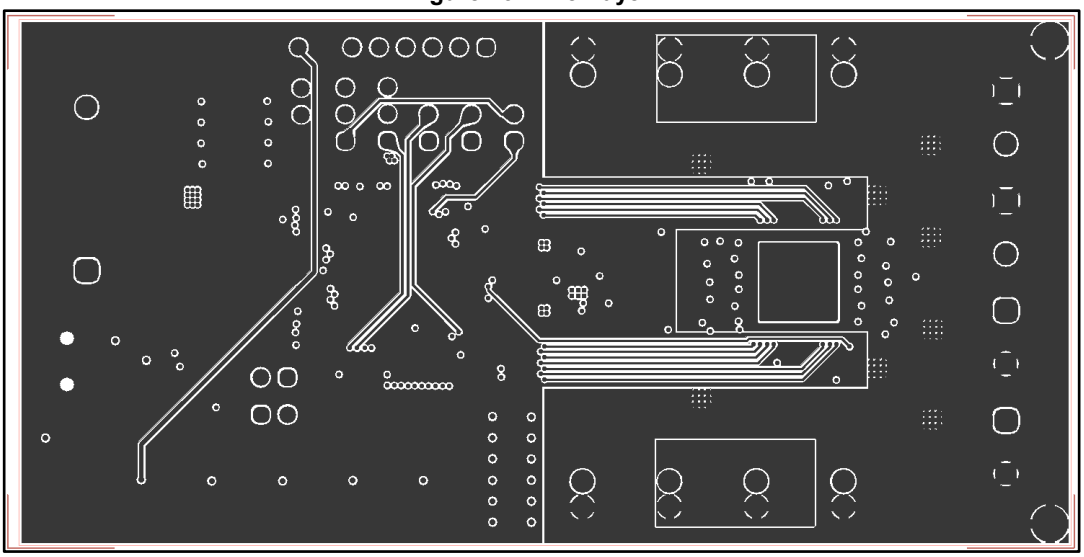


Figure 26: Inner layer 3

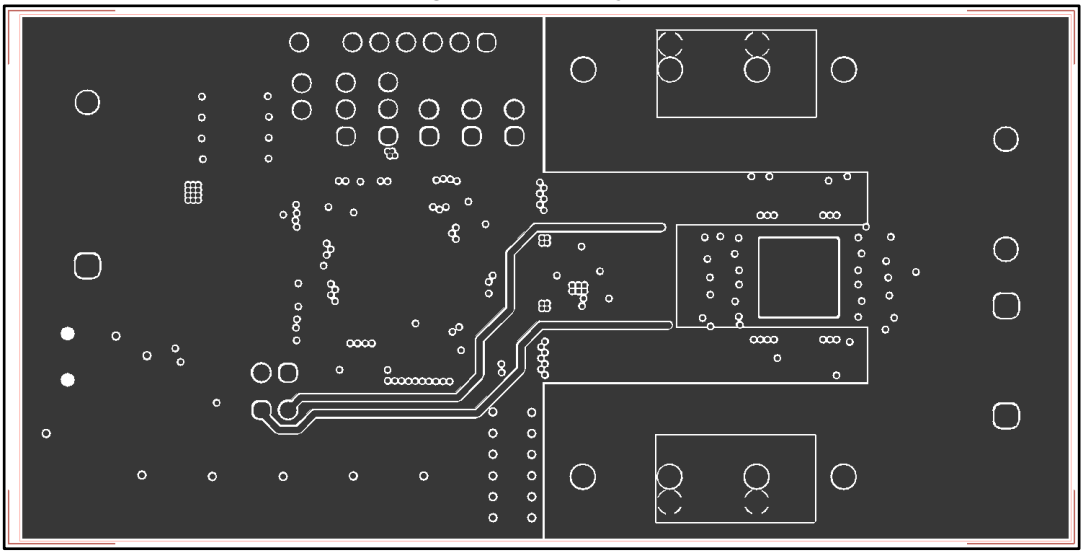


Figure 27: Inner layer 4

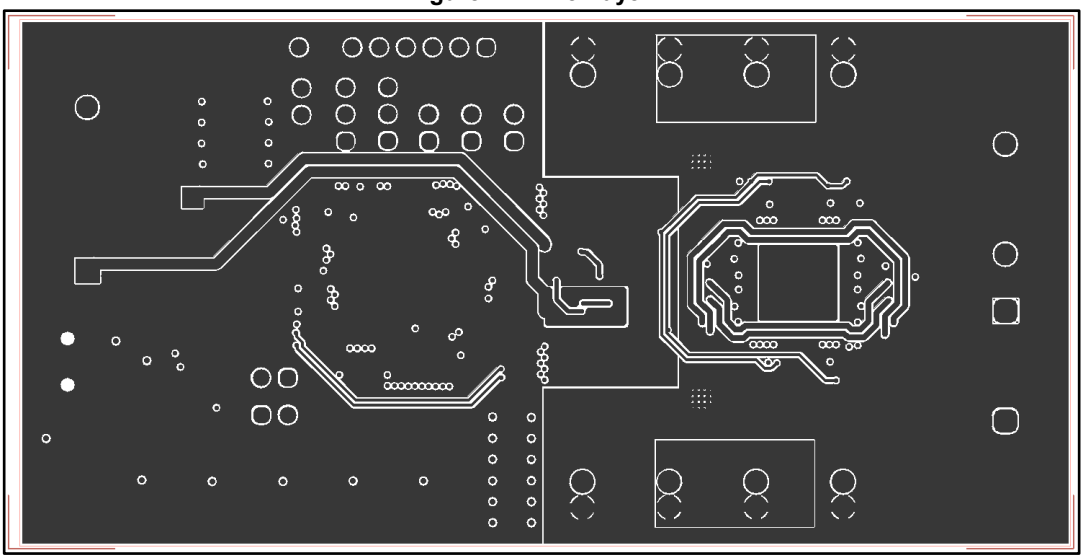
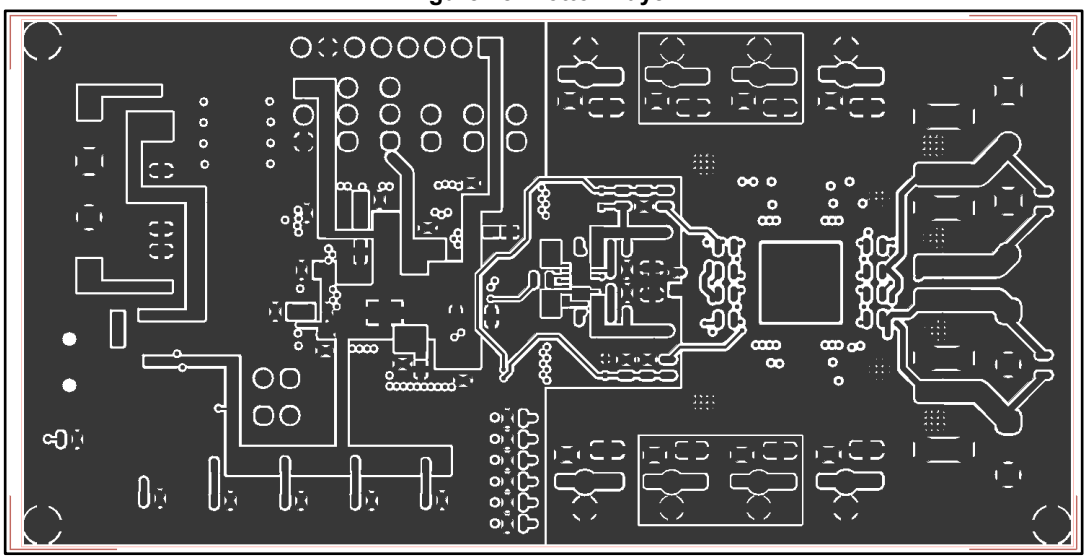


Figure 28: Bottom layer



7 Revision history

Table 9: Document revision history

Date	Version	Changes
17-Jan-2017	1	Initial release.

IMPORTANT NOTICE – PLEASE READ CAREFULLY

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