



# STW36NM60N

N-channel 600 V, 0.092  $\Omega$ , 29 A, MDmesh™ II Power MOSFET  
in TO-247

## Features

Order code	V <sub>DSS</sub> @ T <sub>Jmax</sub>	R <sub>DS(on)</sub> max	I <sub>D</sub>	P <sub>W</sub>
STW36NM60N	650 V	< 0.105 $\Omega$	29 A	210 W

- 100% avalanche tested
- Low input capacitance and gate charge
- Low gate input resistance

## Application

- Switching applications
  - Automotive

## Description

This device is made using the second generation of MDmesh™ technology. This revolutionary Power MOSFET associates a new vertical structure to the company's strip layout to yield one of the world's lowest on-resistance and gate charge. It is therefore suitable for the most demanding high efficiency converters.

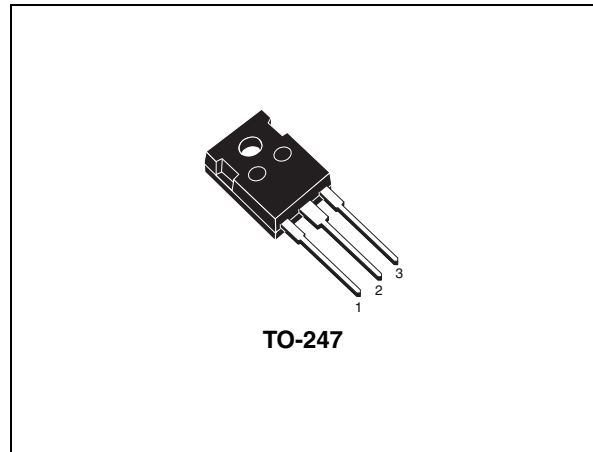


Figure 1. Internal schematic diagram

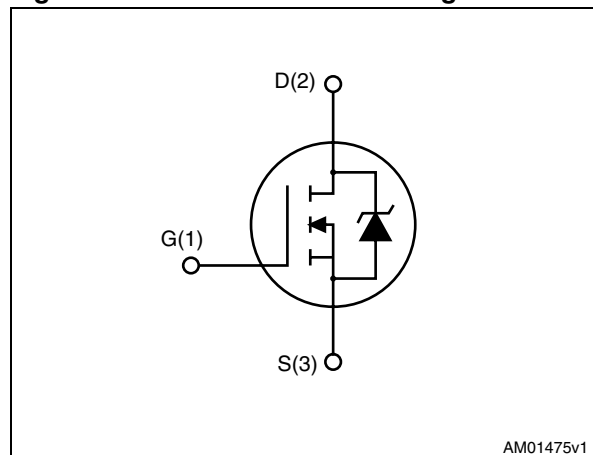


Table 1. Device summary

Order code	Marking	Package	Packaging
STW36NM60N	36NM60N	TO-247	Tape and reel

# Contents

<b>1</b>	<b>Electrical ratings</b> .....	<b>3</b>
<b>2</b>	<b>Electrical characteristics</b> .....	<b>4</b>
	2.1 Electrical characteristics (curves) .....	6
<b>3</b>	<b>Test circuits</b> .....	<b>8</b>
<b>4</b>	<b>Package mechanical data</b> .....	<b>9</b>
<b>5</b>	<b>Revision history</b> .....	<b>12</b>

# 1 Electrical ratings

**Table 2. Absolute maximum ratings**

Symbol	Parameter	Value	Unit
$V_{DS}$	Drain-source voltage ( $V_{GS}=0$ )	600	V
$V_{GS}$	Gate-source voltage	$\pm 25$	V
$I_D$	Drain current (continuous) at $T_C = 25\text{ }^\circ\text{C}$	29	A
$I_D$	Drain current (continuous) at $T_C = 100\text{ }^\circ\text{C}$	18	A
$I_{DM}^{(1)}$	Drain current (pulsed)	116	A
$P_{TOT}$	Total dissipation at $T_C = 25\text{ }^\circ\text{C}$	210	W
$I_{AR}$	Avalanche current, repetitive or not-repetitive (pulse width limited by $T_j$ max.)	10.5	A
$E_{AS}$	Single pulse avalanche energy (Starting $T_j = 25\text{ }^\circ\text{C}$ , $I_D = I_{AR}$ , $V_{DD} = 50\text{ V}$ .)	345	mJ
$dv/dt^{(2)}$	Peak diode recovery voltage slope	15	V/ns
$T_{stg}$	Storage temperature	-55 to 150	$^\circ\text{C}$
$T_j$	Max. operating junction temperature	150	$^\circ\text{C}$

1. Pulse width limited by safe operating area.
2.  $I_{SD} \leq 29\text{ A}$ ,  $di/dt \leq 400\text{ A}/\mu\text{s}$ ,  $V_{DS\text{ peak}} \leq V_{(BR)DSS}$ ,  $V_{DD} = 80\% V_{(BR)DSS}$

**Table 3. Thermal data**

Symbol	Parameter	Value	Unit
$R_{thj-case}$	Thermal resistance junction-case max	0.6	$^\circ\text{C}/\text{W}$
$R_{thj-pcb}^{(1)}$	Thermal resistance junction-pcb max	30	$^\circ\text{C}/\text{W}$
$T_l$	Maximum lead temperature for soldering purposes	300	$^\circ\text{C}$

1. When mounted on FR-4 board of 1inch<sup>2</sup>, 2oz Cu,  $t < 10\text{ sec}$

## 2 Electrical characteristics

(T<sub>case</sub> = 25°C unless otherwise specified)

**Table 4. On /off states**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
V <sub>(BR)DSS</sub>	Drain-source breakdown voltage	I <sub>D</sub> = 1 mA, V <sub>GS</sub> = 0	600			V
I <sub>DSS</sub>	Zero gate voltage drain current (V <sub>GS</sub> = 0)	V <sub>DS</sub> = Max rating V <sub>DS</sub> = Max rating, T <sub>C</sub> = 125 °C			10 100	μA μA
I <sub>GSS</sub>	Gate-body leakage current (V <sub>DS</sub> = 0)	V <sub>GS</sub> = ± 25 V			100	nA
V <sub>GS(th)</sub>	Gate threshold voltage	V <sub>DS</sub> = V <sub>GS</sub> , I <sub>D</sub> = 250 μA	2	3	4	V
R <sub>DS(on)</sub>	Static drain-source on resistance	V <sub>GS</sub> = 10 V, I <sub>D</sub> = 14.5 A		0.092	0.105	Ω

**Table 5. Dynamic**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
C <sub>iss</sub>	Input capacitance	V <sub>DS</sub> = 100 V, f = 1 MHz, V <sub>GS</sub> = 0	-	2722	-	pF
C <sub>oss</sub>	Output capacitance			173		pF
C <sub>rss</sub>	Reverse transfer capacitance			1.75		pF
C <sub>oss eq.</sub> <sup>(1)</sup>	Equivalent Output capacitance	V <sub>GS</sub> = 0, V <sub>DS</sub> = 0 to 480 V	-	458	-	pF
R <sub>g</sub>	Gate input resistance	f = 1MHz Gate DC Bias = 0 Test signal level = 20 mV open drain	-	2.9	-	Ω
Q <sub>g</sub>	Total gate charge	V <sub>DD</sub> = 480 V, I <sub>D</sub> = 29 A, V <sub>GS</sub> = 10 V <i>(see Figure 15)</i>	-	83.6	-	nC
Q <sub>gs</sub>	Gate-source charge			14		nC
Q <sub>gd</sub>	Gate-drain charge			45		nC

1. C<sub>oss eq.</sub> is defined as a constant equivalent capacitance giving the same charging time as C<sub>oss</sub> when V<sub>DS</sub> increases from 0 to 80% V<sub>DS</sub>

**Table 6. Switching times**

Symbol	Parameter	Test conditions	Min.	Typ.	Max	Unit	
$t_{d(on)}$	Turn-on delay time	$V_{DD} = 300\text{ V}$ , $I_D = 14.5\text{ A}$ , $R_G = 4.7\ \Omega$ , $V_{GS} = 10\text{ V}$ (see Figure 14)		17		ns	
$t_r$	Rise time			34		ns	
$t_{d(off)}$	Turn-off-delay time				106		ns
$t_f$	Fall time				67		ns

**Table 7. Source drain diode**

Symbol	Parameter	Test conditions	Min	Typ.	Max	Unit
$I_{SD}$	Source-drain current				29	A
$I_{SDM}^{(1)}$	Source-drain current (pulsed)		-		116	A
$V_{SD}^{(2)}$	Forward on voltage	$I_{SD} = 29\text{ A}$ , $V_{GS} = 0$	-		1.6	V
$t_{rr}$	Reverse recovery time	$I_{SD} = 29\text{ A}$ , $di/dt = 100\text{ A}/\mu\text{s}$ $V_{DD} = 60\text{ V}$ (see Figure 19)		408		ns
$Q_{rr}$	Reverse recovery charge			8		$\mu\text{C}$
$I_{RRM}$	Reverse recovery current			39		A
$t_{rr}$	Reverse recovery time	$I_{SD} = 29\text{ A}$ , $di/dt = 100\text{ A}/\mu\text{s}$ $V_{DD} = 60\text{ V}$ $T_j = 150\text{ }^\circ\text{C}$ (see Figure 19)		480		ns
$Q_{rr}$	Reverse recovery charge			10		$\mu\text{C}$
$I_{RRM}$	Reverse recovery current			42		A

1. Pulse width limited by safe operating area

2. Pulsed: pulse duration = 300 $\mu\text{s}$ , duty cycle 1.5%

## 2.1 Electrical characteristics (curves)

Figure 2. Safe operating area

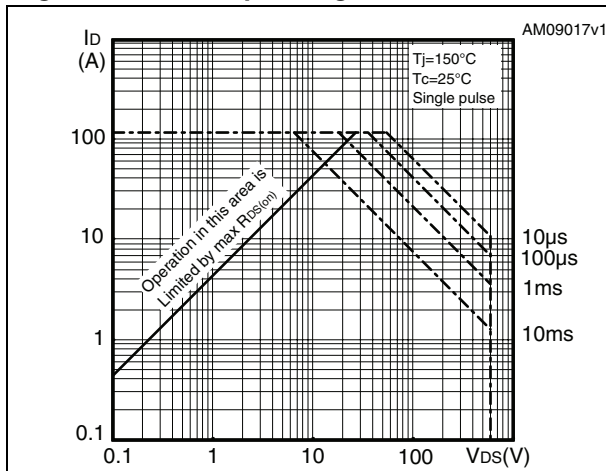


Figure 3. Thermal impedance

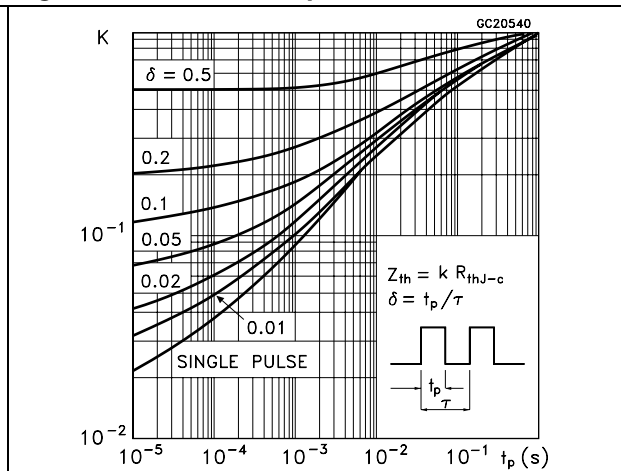


Figure 4. Output characteristics

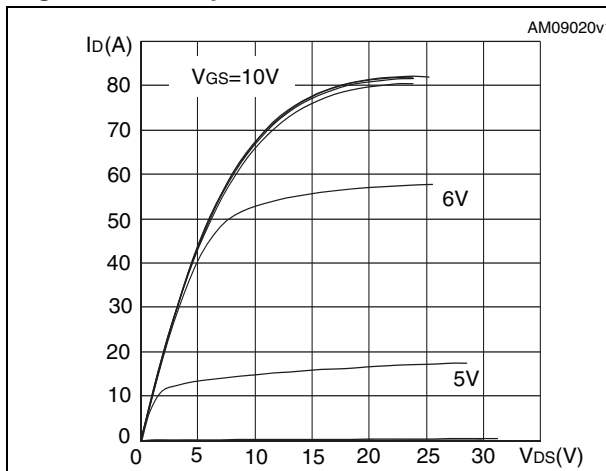


Figure 5. Transfer characteristics

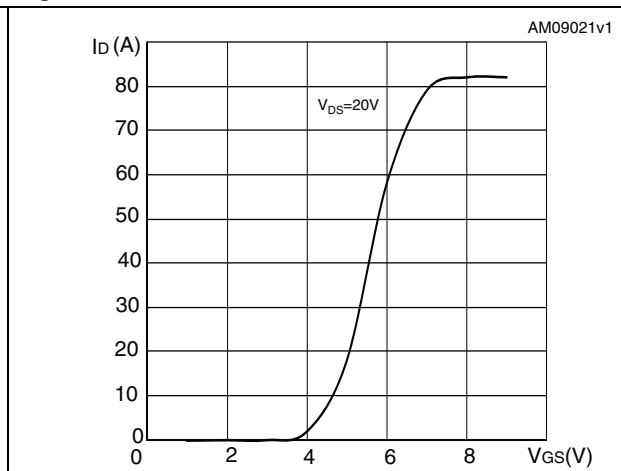


Figure 6. Gate charge vs gate-source voltage

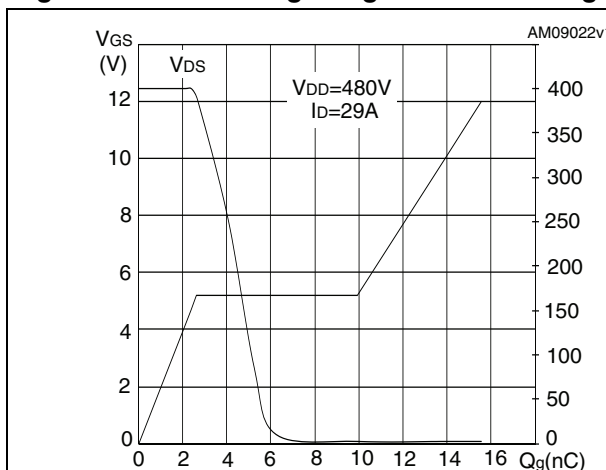


Figure 7. Static drain-source on resistance

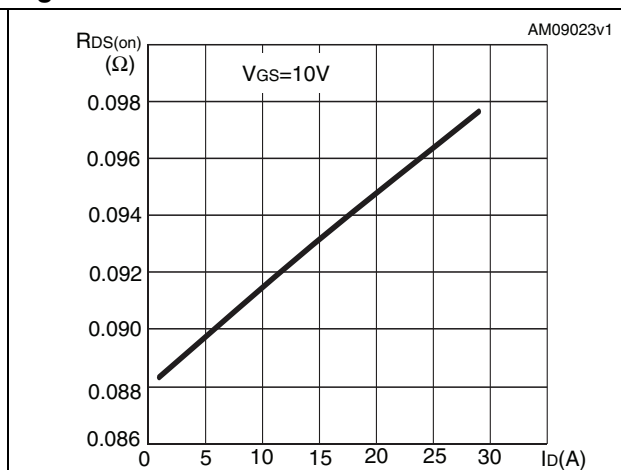


Figure 8. Capacitance variations

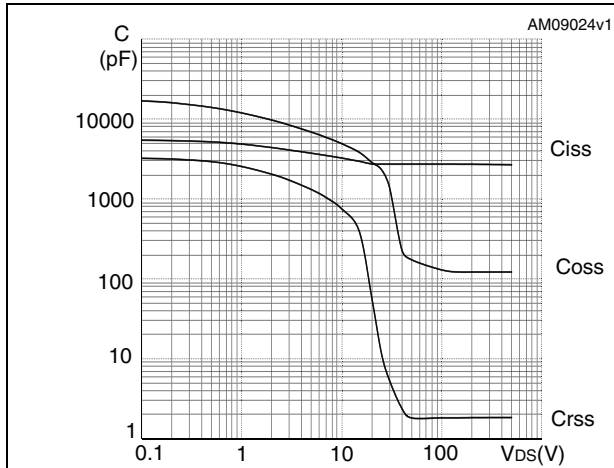


Figure 9. Output capacitance stored energy

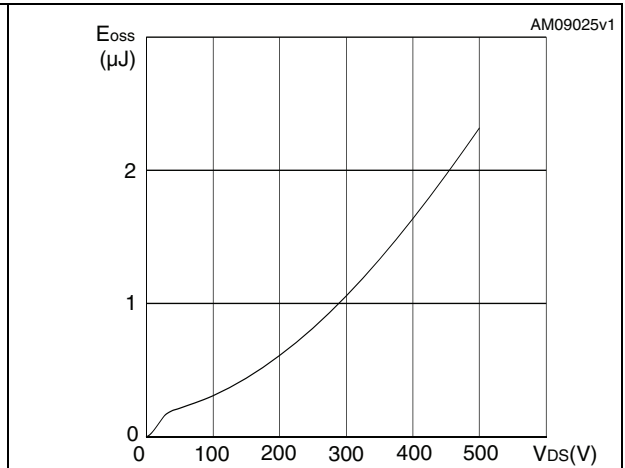


Figure 10. Normalized gate threshold voltage vs temperature

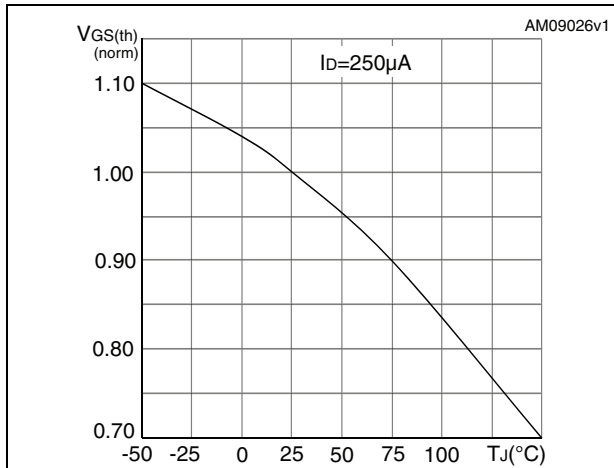


Figure 11. Normalized on resistance vs temperature

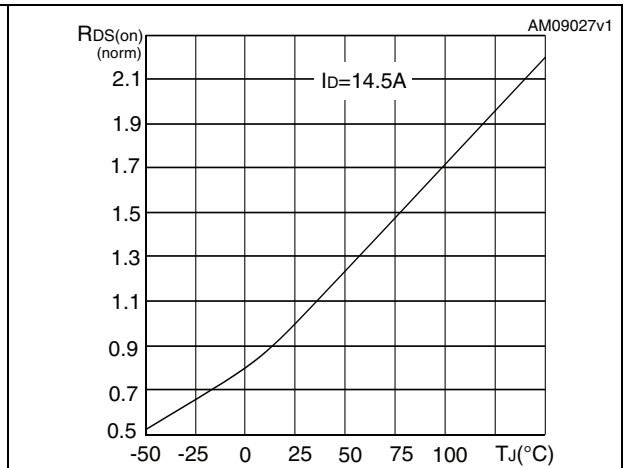


Figure 12. Normalized BVDS vs temperature

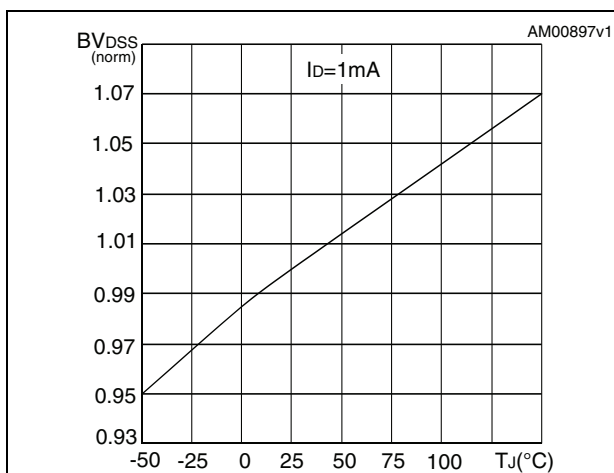
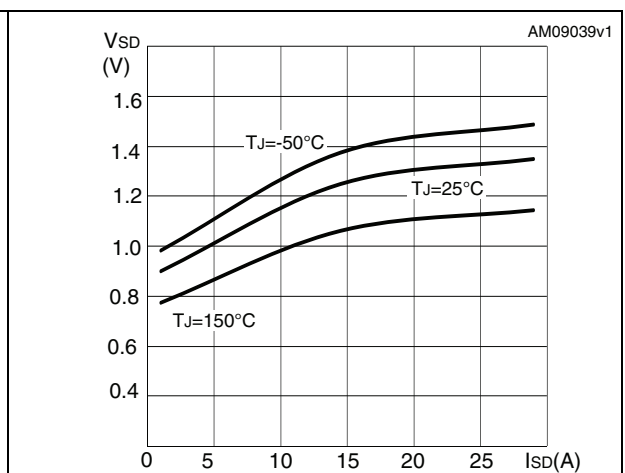
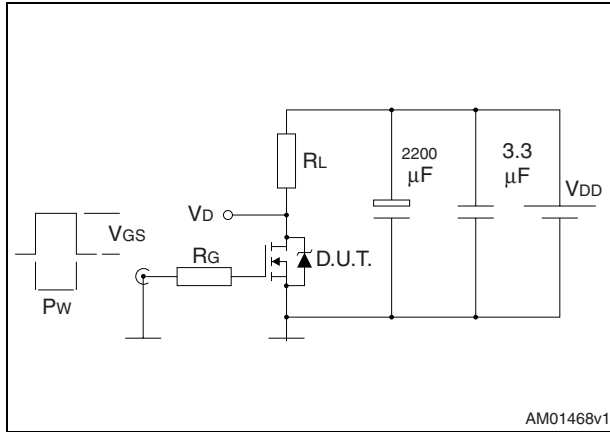


Figure 13. Source-drain diode forward characteristics

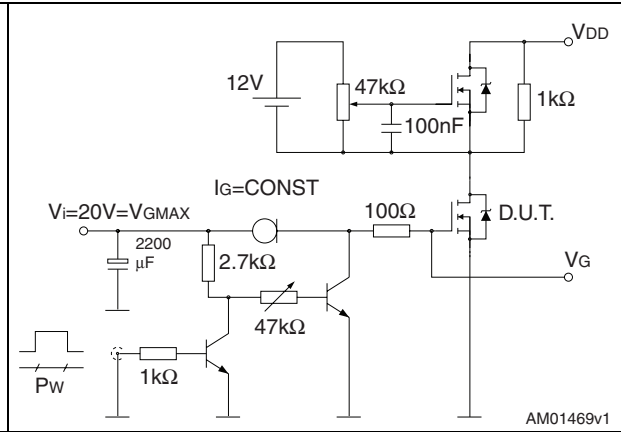


### 3 Test circuits

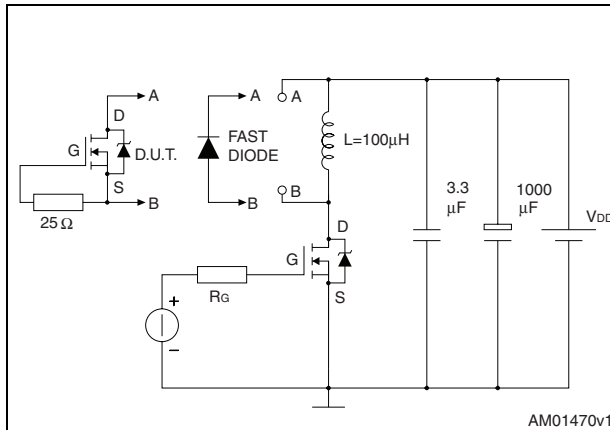
**Figure 14. Switching times test circuit for resistive load**



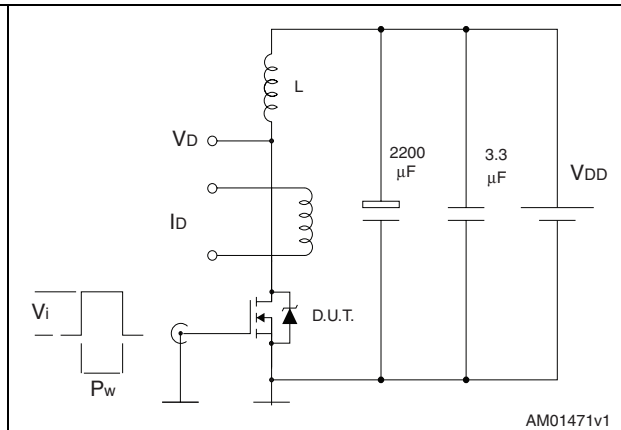
**Figure 15. Gate charge test circuit**



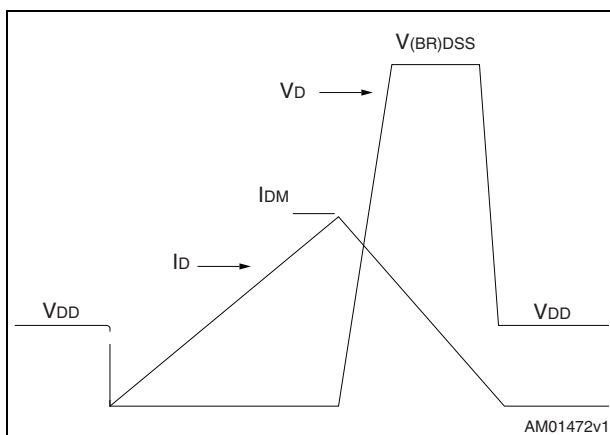
**Figure 16. Test circuit for inductive load switching and diode recovery times**



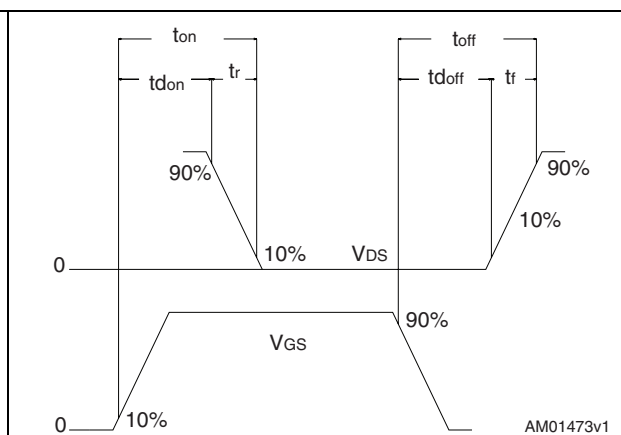
**Figure 17. Unclamped inductive load test circuit**



**Figure 18. Unclamped inductive waveform**



**Figure 19. Switching time waveform**





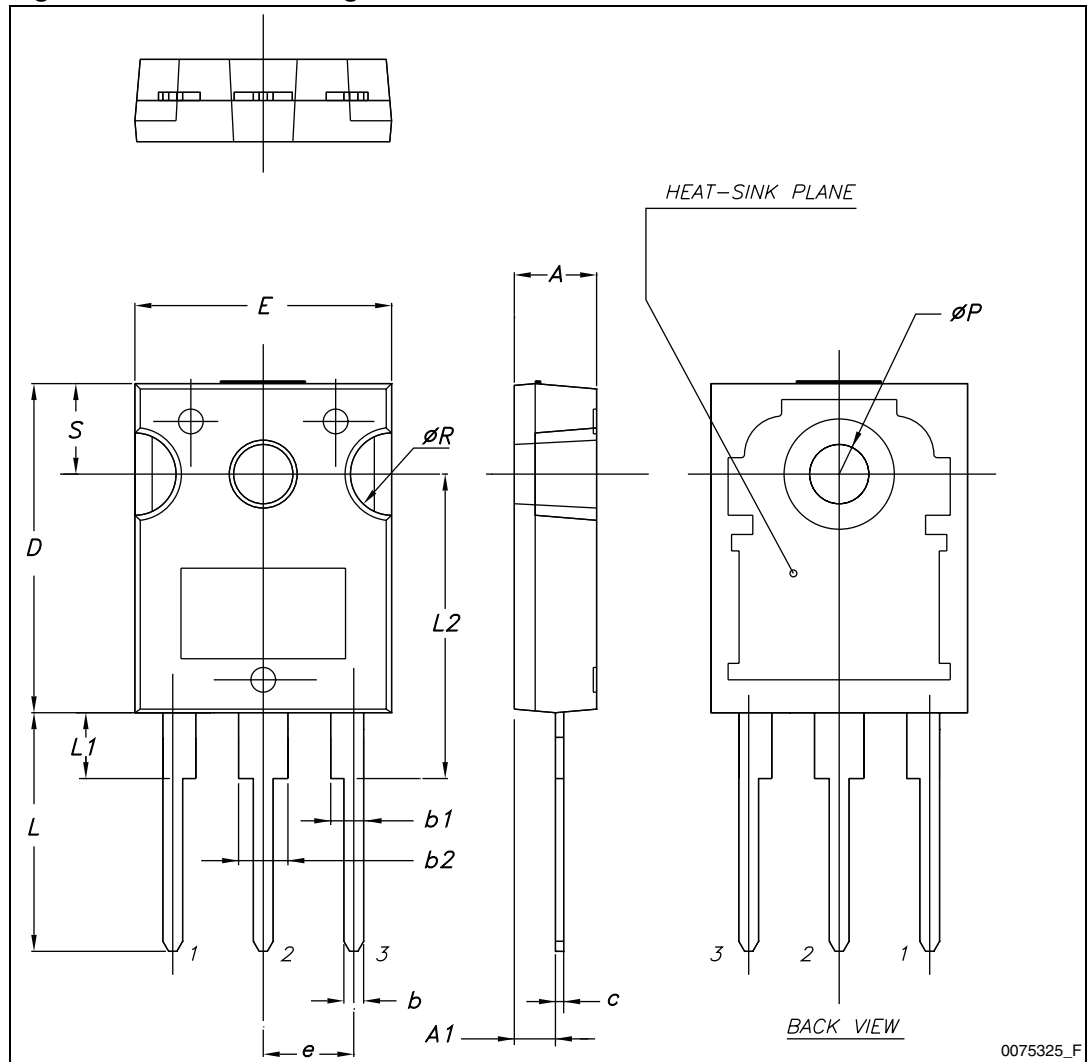
## 4 Package mechanical data

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: [www.st.com](http://www.st.com). ECOPACK is an ST trademark.

Table 8. TO-247 mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A	4.85		5.15
A1	2.20		2.60
b	1.0		1.40
b1	2.0		2.40
b2	3.0		3.40
c	0.40		0.80
D	19.85		20.15
E	15.45		15.75
e		5.45	
L	14.20		14.80
L1	3.70		4.30
L2		18.50	
ØP	3.55		3.65
ØR	4.50		5.50
S		5.50	

Figure 20. TO-247 drawing



0075325\_F

## 5 Revision history

**Table 9. Document revision history**

Date	Revision	Changes
21-Jun-2011	1	First release.

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