PIC18F87J11 Family
Silicon Errata and Data Sheet Clarification

The PIC18F87J11 family of devices that you have received conform functionally to the current Device Data Sheet (DS39778**E**), except for the anomalies described in this document.

The silicon issues discussed in the following pages are for silicon revisions with the Device and Revision IDs listed in Table 1. The silicon issues are summarized in Table 2.

The errata described in this document will be addressed in future revisions of the PIC18F87J11 family silicon.

Note:	This document summarizes all silicon errata issues from all revisions of silicon, previous as well as current. Only the issues indicated in the last column of Table 2 apply to the current silicon revision (**A6** or **C2**, respectively).

Data Sheet clarifications and corrections start on page 6, following the discussion of silicon issues.

The silicon revision level can be identified using the current version of MPLAB® IDE and Microchip's programmers, debuggers, and emulation tools, which are available at the Microchip corporate web site (www.microchip.com).

For example, to identify the silicon revision level using MPLAB IDE in conjunction with a hardware debugger:

1. Using the appropriate interface, connect the device to the hardware debugger.
2. Open an MPLAB IDE project.
3. Configure the MPLAB IDE project for the appropriate device and hardware debugger.
4. Based on the version of MPLAB IDE you are using, do one of the following:
   a) For MPLAB IDE 8, select *Programmer > Reconnect*.
   b) For MPLAB X IDE, select *Window > Dashboard* and click the **Refresh Debug Tool Status** icon ( ).
5. Depending on the development tool used, the part number *and* Device Revision ID value appear in the **Output** window.

Note:	If you are unable to extract the silicon revision level, please contact your local Microchip sales office for assistance.

The DEVREV values for the various PIC18F87J11 family silicon revisions are shown in Table 1.

TABLE 1: SILICON DEVREV VALUES

Part Number	Device ID(1)	Revision ID for Silicon Revision(2)						
		A1	A2	A4	A5	A6	C1	C2
PIC18F66J11	444h	1h	2h	4h	5h	6h	10h	13h
PIC18F66J16	446h							
PIC18F67J11	448h							
PIC18F86J11	44Eh							
PIC18F86J16	450h							
PIC18F87J11	452h							

Note 1: The Device IDs (DEVID and DEVREV) are located at the last two implemented addresses of configuration memory space. They are shown in hexadecimal in the format "DEVID DEVREV".

2: Refer to the *"PIC18F6XJXX/8XJXX Flash Microcontroller Programming Specification"* (DS39644) for detailed information on Device and Revision IDs for your specific device.

TABLE 2: SILICON ISSUE SUMMARY

Module	Feature	Item Num	Issue Summary	Affected Revisions(1)						
				A1	A2	A4	A5	A6	C1	C2
Master Synchronous Serial Port (MSSPx)	I^2C Slave Reception	1.	When configured for I^2C slave reception, the MSSPx module may not receive the correct data if the SSPxBUF register is not read within a window after an SSPxIF interrupt occurs.	X	X	X	X	X	X	X
Oscillator Configurations (PLL)	PLL	2.	When Phase Lock Loop (PLL) is enabled, if the PLL input frequency is higher than 8 MHz, there may be problems accessing the RAM.	X	X					
Voltage Regulator	V_{DDCORE}	3.	If V_{DDCORE} drops below approximately 2.45V, while the on-chip core voltage regulator is enabled and operating in Voltage Tracking mode, the REGSLP bit (WDTCON <7>) will be automatically cleared.	X						
SRAM	Read/Write	4.	Any read or write access to SRAM will increase the current consumption of the device – varying with how often the SRAM is accessed.	X						
Low-Voltage Detect	LVDSTAT	5.	The LVDSTAT V_{DDCORE} Status bit is not implemented in the cited revision of silicon.	X						
MSSPx (I2C Master)	I^2C Master mode	6.	In Master mode, the first clock may become narrower than the configuration width if the slave performs a clock stretch and release.	X	X	X	X	X	X	
Enhanced Universal Synchronous Asynchronous Receiver Transmitter (EUSART)	Synchronous Mode	7.	The TRMT bit may not indicate when the TSR register is empty.	X	X	X	X	X	X	X
Timer1/3	Interrupt	8.	When the timer is operated in Asynchronous External Input mode, unexpected interrupt flag generation may occur.	X	X	X	X	X	X	X

Note 1: Only those issues indicated in the last column apply to the current silicon revision.

Silicon Errata Issues

Note: This document summarizes all silicon errata issues from all revisions of silicon, previous as well as current. Only the issues indicated by the shaded column in the following tables apply to the current silicon revision (**A6** or **C2**, respectively).

1. Module: Master Synchronous Serial Port (MSSPx)

When configured for I^2C slave reception, the MSSPx module may not receive the correct data, in extremely rare cases. This occurs only if the Serial Receive/Transmit Buffer Register (SSPxBUF) is not read within a window after the SSPxIF interrupt (PIRx<3>) has occurred.

Work around

The issue can be resolved in either of these ways:

- Prior to the I^2C slave reception, enable the clock stretching feature.

  This is done by setting the SEN bit (SSPxCON2<0>).
- Each time the SSPxIF is set, read the SSPxBUF before the first rising clock edge of the next byte being received.

Affected Silicon Revisions

A1	A2	A4	A5	A6	C1	C2	
X	X	X	X	X	X	X	

2. Module: Oscillator Configurations (PLL)

When Phase Lock Loop (PLL) is enabled, if the PLL input frequency is higher than 8 MHz, there may be problems accessing the RAM.

Work around

Limit the PLL input frequency from 4 MHz to 8 MHz. This will cause the system clock to operate from 16 MHz to 32 MHz.

If it is necessary to run the device above 32 MHz, do not enable PLL and use the EC mode.

Affected Silicon Revisions

A1	A2	A4	A5	A6	C1	C2	
X	X						

3. Module: Voltage Regulator

If V_{DDCORE} drops below approximately 2.45V while the on-chip core voltage regulator is enabled, and operating in Voltage Tracking mode, the REGSLP bit (WDTCON <7>) will be automatically cleared. The REGSLP bit cannot be set again by firmware until V_{DDCORE} rises back above the 2.45V approximate threshold.

Additionally, the REGSLP bit retains its previous state upon all Resets except POR.

Work around

None.

Affected Silicon Revisions

A1	A2	A4	A5	A6	C1	C2	
X							

4. Module: SRAM

Any access to SRAM, either in the form of read or write operations, will increase the current consumption of the device, depending on how often the SRAM is accessed. A small current increase is normal, but in this cited silicon revision, the difference may be significant and of particular concern for low-power applications.

For further details, see Table 3.

TABLE 3: TYPICAL CURRENT CONSUMPTION

Case 1:			
Voltage Regulator Enabled Temperature = +25°C SEC_RUN mode using 32 kHz Timer1 Crystal			
Condition	**IDD (μA)**	**VDD (V)**	
No RAM access(1)	59	3.3	
Typ RAM access(2)	201	3.3	
Extreme RAM access(3)	906	3.3	
Case 2:			
Voltage Regulator Disabled VDDCORE is tied to VDD Temperature = +25°C SEC_RUN mode using 32 kHz Timer1 Crystal			
Condition	**IDD (μA)**	**VDD (V)**	**VDDCORE (V)**
No RAM access(1)	20	2.5	2.5
Typ RAM access(2)	132	2.5	2.5
Extreme RAM access(3)	723	2.5	2.5

Note 1: Code execution patterns where no instructions access SRAM.
2: Code execution that accesses SRAM, once every seven instruction cycles.
3: Code execution where every instruction cycle executes an instruction that accesses SRAM.

Work around

None.

Affected Silicon Revisions

A1	A2	A4	A5	A6	C1	C2	
X							

5. Module: Low-Voltage Detect

The LVDSTAT, VDDCORE Status bit (WDTCON<6>), is not implemented in this revision of silicon.

Work around

None.

Affected Silicon Revisions

A1	A2	A4	A5	A6	C1	C2	
X							

6. Module: MSSPx (I^2C Master)

If the module is in I^2C Master mode, and the slave performs clock stretching, the first clock pulse after the slave releases the SCLx line may be narrower than the configured clock width. This may result in the slave missing the first clock in the next transmission/reception.

Work around

If the module is in I^2C Master mode, do not allow the slave to perform clock stretching. Alternately, the master can slow down the SCLx clock frequency to a level where the slave can detect the narrowed clock pulse.

Affected Silicon Revisions

A1	A2	A4	A5	A6	C1	C2	
X	X	X	X	X	X		

7. Module: Enhanced Universal Synchronous Asynchronous Receiver Transmitter (EUSART)

In Synchronous Slave Transmission mode, the TRMT bit (TXSTA<1>) may not indicate when the TSR register is empty.

Work around

Instead of polling the TRMT bit to determine the status of the EUSART, poll the TXIF flag (PIR1<4>) to determine when new data can be written to the TXREG register.

Affected Silicon Revisions

A1	A2	A4	A5	A6	C1	C2	
X	X	X	X	X	X	X	

8. Module: Timer1/3

When Timer1 or Timer3 is operated in Asynchronous External Input mode, unexpected interrupt flag generation may occur if an external clock edge arrives too soon following a firmware write to the TMRxH:TMRxL registers. An unexpected interrupt flag event may also occur when enabling the module or switching from Synchronous to Asynchronous mode.

Work around

This issue only applies when operating the timer in Asynchronous mode. Whenever possible, operate the timer module in Synchronous mode to avoid spurious timer interrupts.

If Asynchronous mode must be used in the application, potential strategies to mitigate the issue may include any of the following:

- Design the firmware so it does not rely on the TMRxIF flag or keep the respective interrupt disabled. The timer still counts normally and does not reset to `0x0000` when the spurious interrupt flag event is generated.
- Design the firmware so that it does not write to the TMRxH:TMRxL registers or does not periodically disable/enable the timer, or switch modes. Reading from the timer does not trigger the spurious interrupt flag events.
- If the firmware must use the timer interrupts and must write to the timer (or disable/enable, or mode switch the timer), implement code to suppress the spurious interrupt event, should it occur. This can be achieved by following the process shown in Example 1.

EXAMPLE 1: ASYNCHRONOUS TIMER MODE WORK AROUND TO AVOID SPURIOUS INTERRUPT

```
//Timer1 update procedure in asynchronous mode
//The code below uses Timer1 as example

T1CONbits.TMR1ON = 0;          //Stop timer from incrementing
PIE1bits.TMR1IE = 0;           //Temporarily disable Timer1 interrupt vectoring
TMR1H = 0x00;                  //Update timer value
TMR1L = 0x00;
T1CONbits.TMR1ON = 1;          //Turn on timer

//Now wait at least two full T1CKI periods + 2TCY before re-enabling Timer1 interrupts.
//Depending upon clock edge timing relative to TMR1H/TMR1L firmware write operation,
//a spurious TMR1IF flag event may sometimes assert. If this happens, to suppress
//the actual interrupt vectoring, the TMR1IE bit should be kept clear until
//after the "window of opportunity" (for the spurious interrupt flag event has passed).
//After the window is passed, no further spurious interrupts occur, at least
//until the next timer write (or mode switch/enable event).

while(TMR1L < 0x02);           //Wait for 2 timer increments more than the Updated Timer
                               //value (indicating more than 2 full T1CKI clock periods elapsed)
NOP();                         //Wait two more instruction cycles
NOP();
PIR1bits.TMR1IF = 0;           //Clear TMR1IF flag, in case it was spuriously set
PIE1bits.TMR1IE = 1;           //Now re-enable interrupt vectoring for timer 1
```

Affected Silicon Revisions

A1	A2	A4	A5	A6	C1	C2	
X	X	X	X	X	X	X	

Data Sheet Clarifications

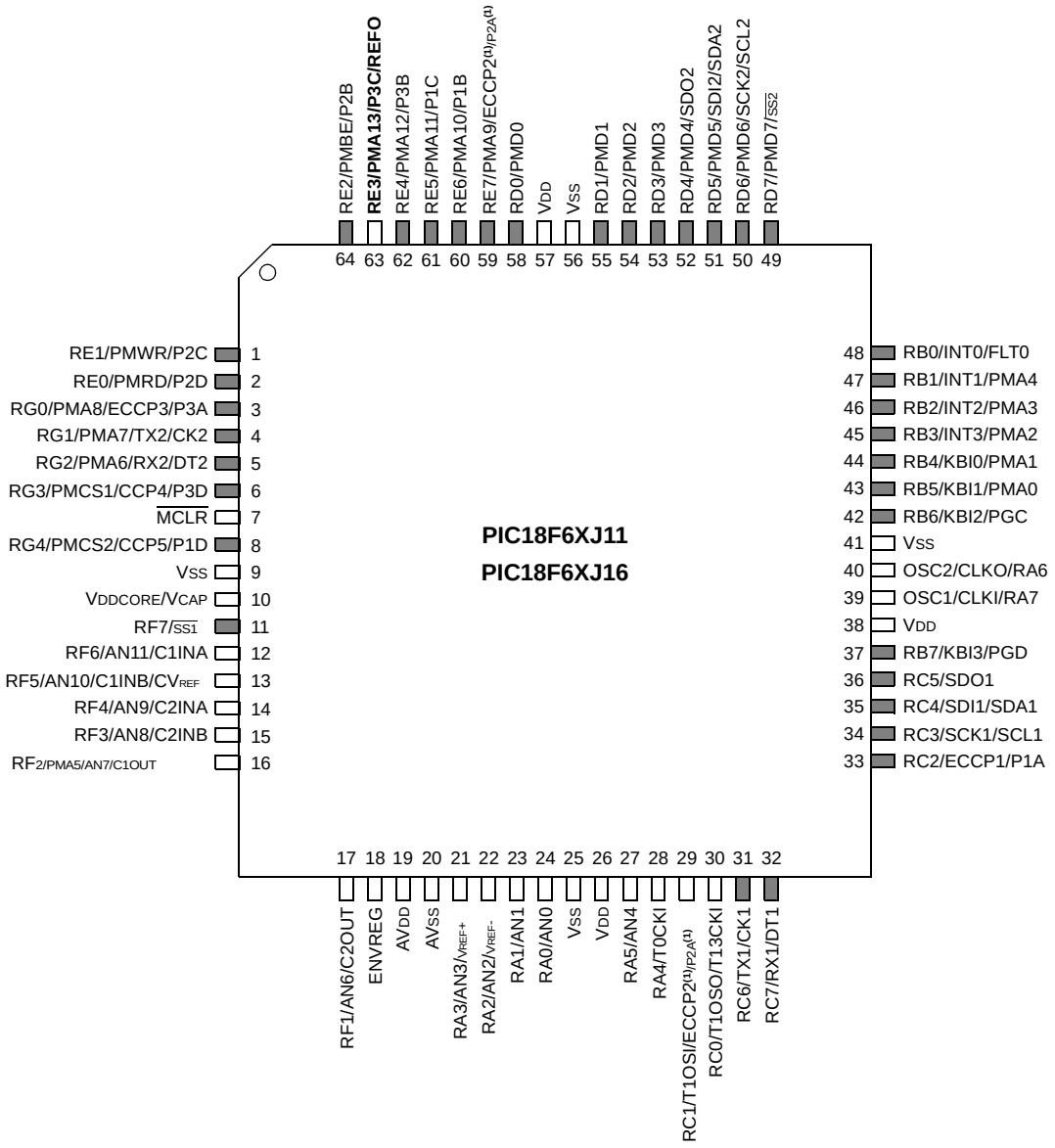
The following typographic corrections and clarifications are to be noted for the latest version of the device data sheet (DS39778**E**):

Note:	Corrections are shown in **bold**. Where possible, the original bold text formatting has been removed for clarity.

1. Module: I/O Ports

PORTE pin RE3 is not +5.5V tolerant as indicated in the data sheet. The pin diagrams should be corrected to read as follows:

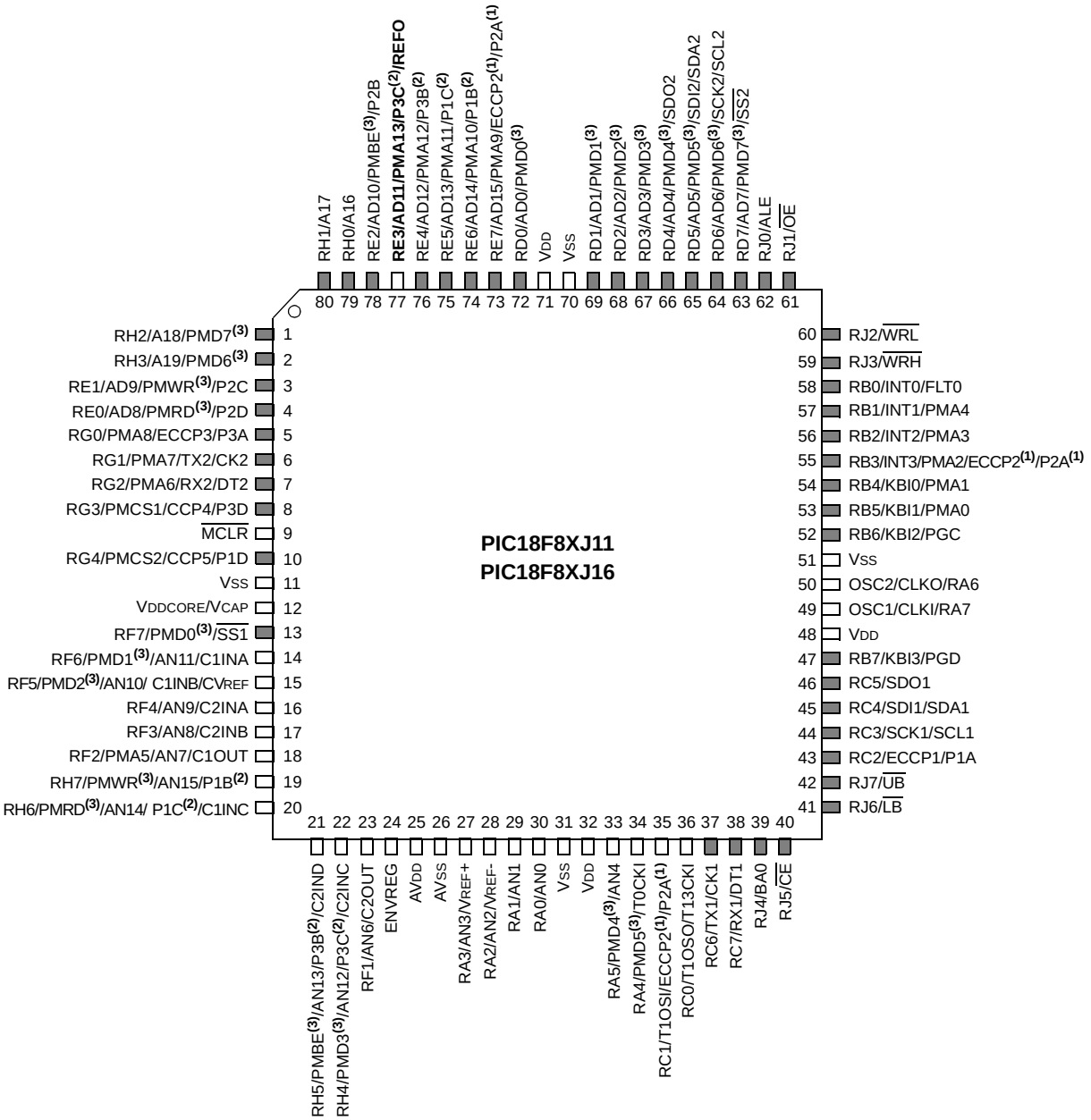
64-Pin TQFP



Legend: Shaded pins indicate pins that are tolerant up to +5.5V.

Note 1: The ECCP2/P2A pin placement depends on the CCP2MX Configuration bit setting.

80-Pin TQFP



Legend: Shaded pins indicate pins that are tolerant up to +5.5V.

Note 1: The ECCP2/P2A pin placement depends on the CCP2MX Configuration bit and Processor mode settings.

2: P1B, P1C, P3B, and P3C pin placement depends on the ECCPMX Configuration bit setting.

3: PMP pin placement depends on the PMPMX Configuration bit setting.

2. Module: Input Voltage Levels

Table 11-1 in Section 11.1.1 should be corrected to read as follows:

TABLE 11-1: INPUT VOLTAGE LEVELS

Port or Pin	Tolerated Input	Description
PORTA<7:0>	VDD	Only VDD input levels are tolerated.
PORTC<1:0>		
PORTE<3>		
PORTF<6:1>		
PORTH<7:4>(1)		
PORTB<7:0>	5.5V	Tolerates input levels above VDD, useful for most standard logic.
PORTC<7:2>		
PORTD<7:0>		
PORTE<7:4>		
PORTE<2:0>		
PORTF<7>		
PORTG<4:0>		
PORTH<3:0>(1)		
PORTJ<7:0>(1)		

Note 1: These ports are not available on PIC18F6XJ1X devices.

APPENDIX A: DOCUMENT REVISION HISTORY

Rev A Document (2/2010)

Combined existing silicon and data sheet errata documents into the new, single document format. Added the A6 silicon revision, but no issues or clarifications.

This document replaces these errata documents:

- DS80418A, *"PIC18F87J11 Family Rev. A5 Silicon Errata"*
- DS80417A, *"PIC18F87J11 Family Rev. A4 Silicon Errata"*
- DS80344A, *"PIC18F87J11 Family Rev. A2 Silicon Errata"*
- DS80305B, *"PIC18F87J11 Family Rev. A1 Silicon Errata"*
- DS80408B, *"PIC18F87J11 Family Data Sheet Errata"*

Rev B Document (7/2010)

Added silicon issue 6 (MSSPx I^2C™ Master).

Added data sheet clarifications 10 and 11 (Memory Organization).

Rev C Document (8/2010)

Added silicon revision B0; includes existing silicon issues 1 (Master Synchronous Serial Port – MSSPx) and 6 (MSSPx – I^2C Master).

No new data sheet clarifications added.

Rev D Document (2/2011)

Replaced silicon revision B0 with revision C1 for lower pin count devices. Added silicon issue 12 (Enhanced Universal Synchronous Asynchronous Receiver Transmitter (EUSART). Removed data sheet clarification 12 (Electrical Characteristics).

Rev E Document (9/2011)

Removed data sheet clarification 12 (Guidelines for Getting Started). Added new data sheet clarification 12 (Electrical Specification). Added new silicon revision (**C2**).

Rev F Document (7/2014)

Added MPLAB X IDE; Added Module 8, Timer1/3 to Silicon Errata Issues.

Data Sheet Clarifications: Removed Modules 1 through 12.

Rev G Document (9/2015)

Data Sheet Clarifications: Added Modules 1 and 2.

Note the following details of the code protection feature on Microchip devices:

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