TOSHIBA Field Effect Transistor Silicon N Channel MOS Type

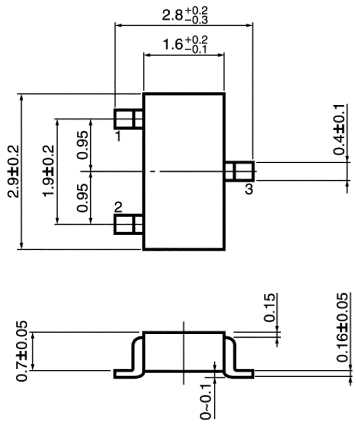
SSM3K316T

Power Management Switch Applications

High-Speed Switching Applications

- 1.8-V drive
- Low ON-resistance: R_{on} = 131 mΩ (max) (@V_{GS} = 1.8 V)
  R_{on} = 87 mΩ (max) (@V_{GS} = 2.5 V)
  R_{on} = 65 mΩ (max) (@V_{GS} = 4.5 V)
  R_{on} = 53 mΩ (max) (@V_{GS} = 10 V)

Unit: mm



1. GATE
2. SOURCE
3. DRAIN

TSM

JEDEC	—
JEITA	—
TOSHIBA	2-3S1A

Weight: 10 mg (typ.)

Absolute Maximum Ratings (Ta = 25°C)

Characteristics		Symbol	Rating	Unit
Drain–source voltage		V_{DSS}	30	V
Gate–source voltage		V_{GSS}	± 12	V
Drain current	DC	I_D (Note 1)	4.0	A
	Pulse	I_{DP} (Note 1)	8.0	
Drain power dissipation		P_D (Note 2)	700	mW
		t = 10s	1250	
Channel temperature		T_{ch}	150	°C
Storage temperature range		T_{stg}	−55 to 150	°C

Note: Using continuously under heavy loads (e.g. the application of high temperature/current/voltage and the significant change in temperature, etc.) may cause this product to decrease in the reliability significantly even if the operating conditions (i.e. operating temperature/current/voltage, etc.) are within the absolute maximum ratings.
Please design the appropriate reliability upon reviewing the Toshiba Semiconductor Reliability Handbook (“Handling Precautions”/“Derating Concept and Methods”) and individual reliability data (i.e. reliability test report and estimated failure rate, etc).

Note 1: The Junction temperature should not exceed 150°C during use.

Note 2: Mounted on an FR4 board. (25.4 mm × 25.4 mm × 1.6 mm, Cu Pad: 645 mm^2)

Electrical Characteristics (Ta = 25°C)

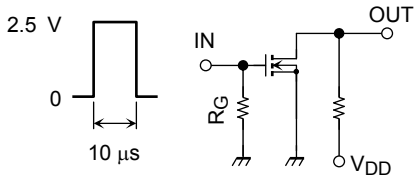
Characteristics		Symbol	Test Condition		Min	Typ.	Max	Unit
Drain–source breakdown voltage		$V_{(BR)\ DSS}$	I_D = 1 mA, V_{GS} = 0 V		30	—	—	V
		$V_{(BR)\ DSX}$	I_D = 1 mA, V_{GS} = –12 V		18	—	—	V
Drain cutoff current		I_{DSS}	V_{DS} = 30 V, V_{GS} = 0 V		—	—	1	μA
Gate leakage current		I_{GSS}	V_{GS} = ± 12 V, V_{DS} = 0 V		—	—	±1	μA
Gate threshold voltage		V_{th}	V_{DS} = 3 V, I_D = 1 mA		0.4	—	1.0	V
Forward transfer admittance		$\|Y_{fs}\|$	V_{DS} = 3 V, I_D = 2 A	(Note3)	3.8	7.7	—	S
Drain–source ON-resistance		$R_{DS\ (ON)}$	I_D = 3.0 A, V_{GS} = 10V	(Note3)	—	42	53	mΩ
			I_D = 2.0 A, V_{GS} = 4.5 V	(Note3)	—	51	65	
			I_D = 1.0 A, V_{GS} = 2.5 V	(Note3)	—	64	87	
			I_D = 0.5 A, V_{GS} = 1.8 V	(Note3)	—	81	131	
Input capacitance		C_{iss}	V_{DS} = 10 V, V_{GS} = 0 V, f = 1 MHz		—	270	—	pF
Output capacitance		C_{oss}			—	56	—	
Reverse transfer capacitance		C_{rss}			—	47	—	
Total Gate Charge		Q_g	V_{DS} = 15 V, I_{DS}= 3.0 A, V_{GS} = 4 V		—	4.3	—	nC
Gate-Source Charge		Q_{gs}			—	2.8	—	
Gate-Drain Charge		Q_{gd}			—	1.5	—	
Switching time	Turn-on time	t_{on}	V_{DD} = 10 V, I_D = 2 A, V_{GS} = 0 to 2.5 V, R_G = 4.7 Ω		—	20	—	ns
	Turn-off time	t_{off}			—	31	—	
Drain–source forward voltage		V_{DSF}	I_D = – 4.0 A, V_{GS} = 0 V	(Note3)	—	– 0.9	– 1.2	V

Note3: Pulse test

Start of commercial production
2008-04

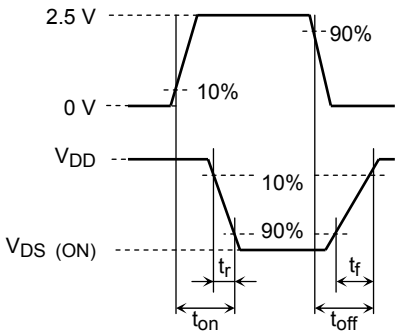
Switching Time Test Circuit

(a) Test Circuit



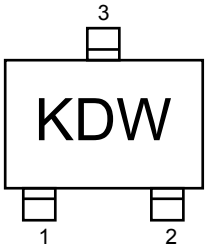
V_{DD} = 10 V
R_G = 4.7 Ω
Duty ≤ 1%
V_{IN}: t_r, t_f < 5 ns
Common Source
Ta = 25°C

(b) V_{IN}

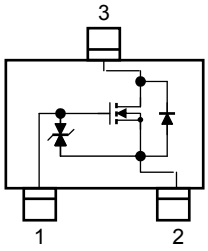


(c) V_{OUT}

Marking



Equivalent Circuit (top view)



Usage Considerations

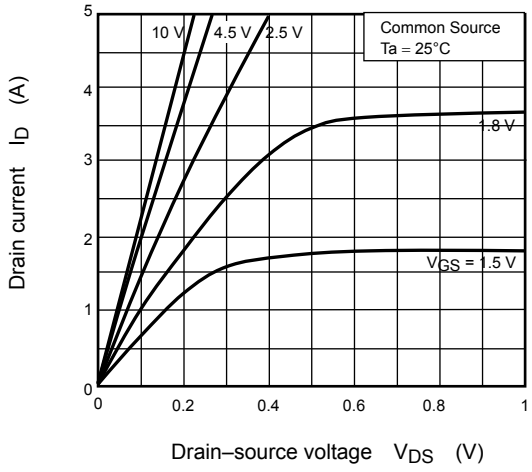
Let V_{th} be the voltage applied between gate and source that causes the drain current (I_D) to below 1 mA for the SSM3K316T). Then, for normal switching operation, $V_{GS(on)}$ must be higher than V_{th}, and $V_{GS(off)}$ must be lower than V_{th}. This relationship can be expressed as: $V_{GS(off)} < V_{th} < V_{GS(on)}$.

Take this into consideration when using the device.

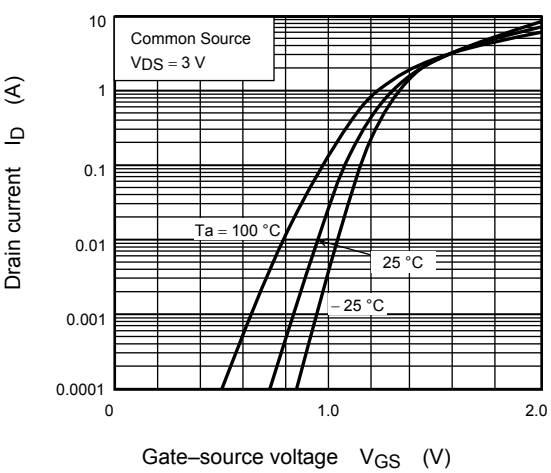
Handling Precaution

When handling individual devices that are not yet mounted on a circuit board, make sure that the environment is protected against electrostatic discharge. Operators should wear antistatic clothing, and containers and other objects that come into direct contact with devices should be made of antistatic materials.

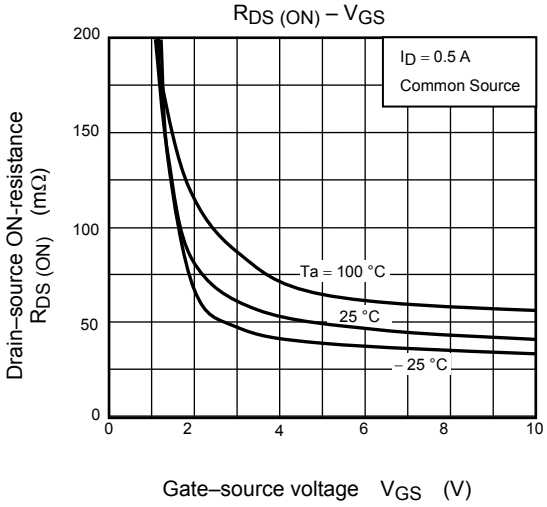
$I_D - V_{DS}$



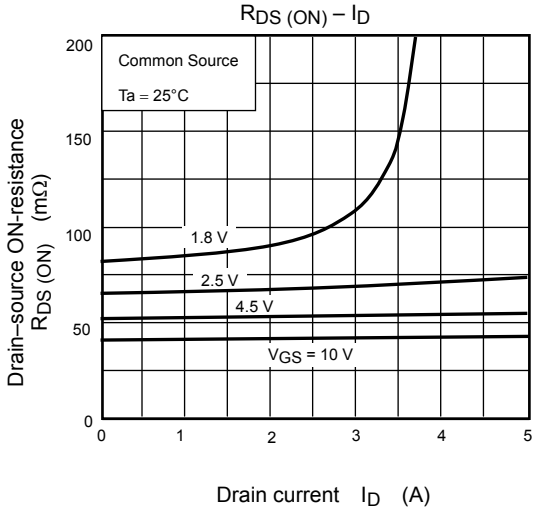
$I_D - V_{GS}$



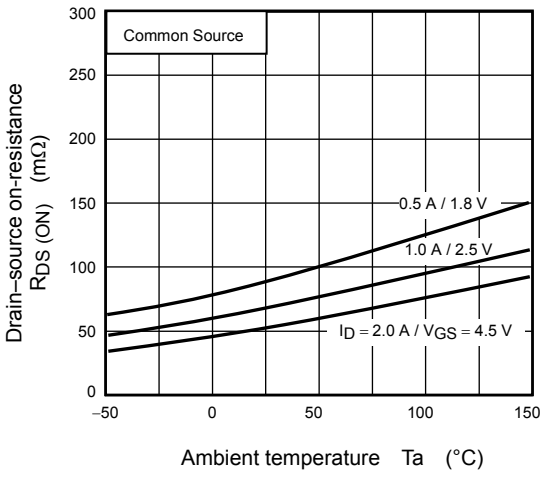
$R_{DS\ (ON)} - V_{GS}$



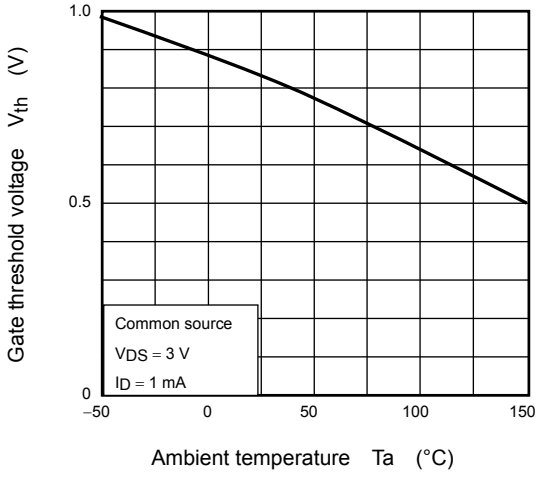
$R_{DS\ (ON)} - I_D$

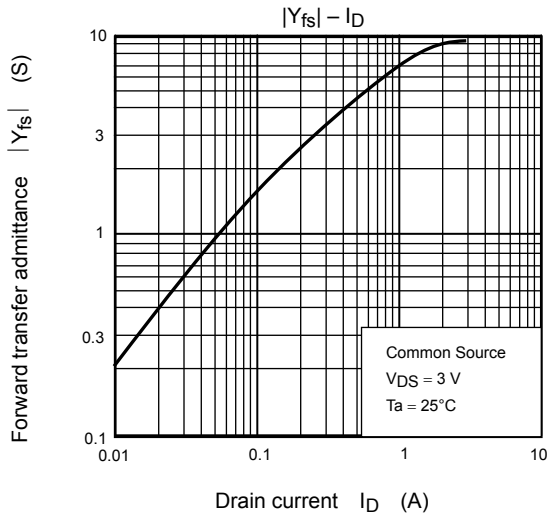


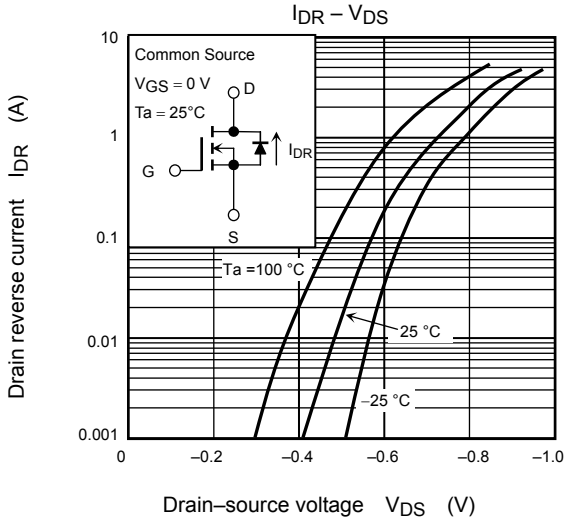
$R_{DS\ (ON)} - Ta$

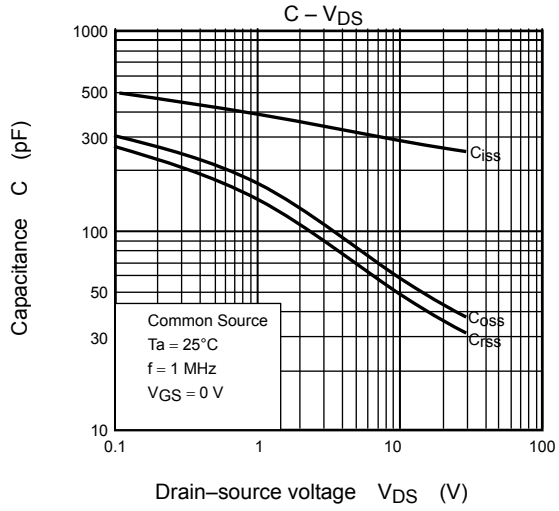


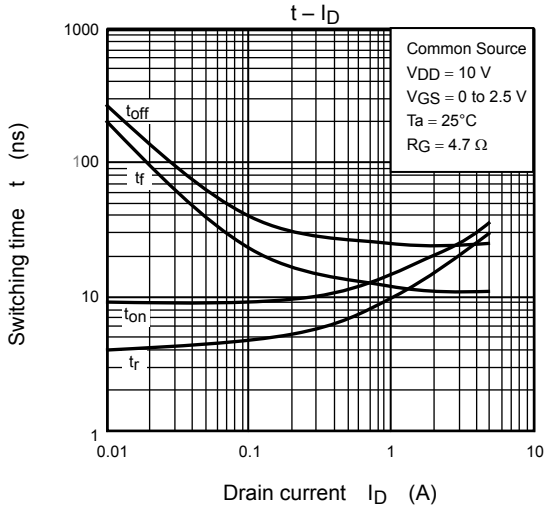
$V_{th} - Ta$

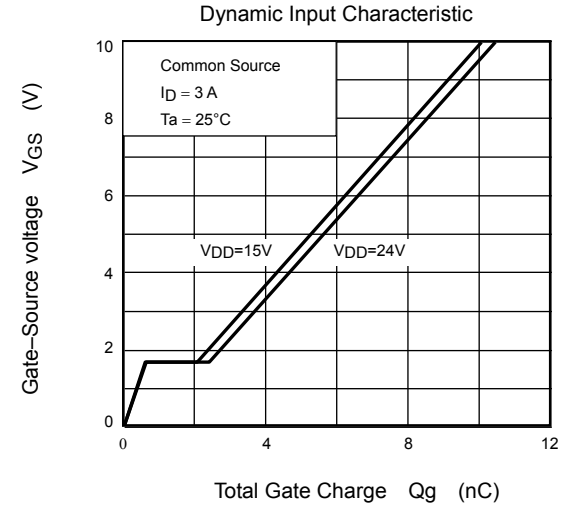



|Yfs| – ID
Forward transfer admittance |Yfs| (S)
10
3
1
0.3
0.1
0.01
0.1
1
10
Common Source
VDS = 3 V
Ta = 25°C
Drain current ID (A)

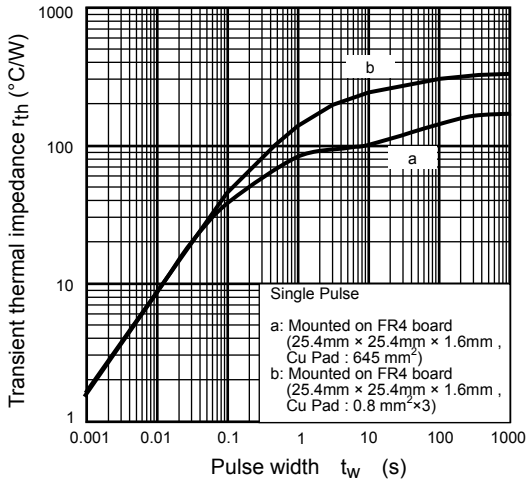

IDR – VDS
Drain reverse current IDR (A)
Common Source
VGS = 0 V
Ta = 25°C
D
G
S
IDR
10
1
0.1
0.01
0.001
Ta =100 °C
25 °C
−25 °C
0
−0.2
−0.4
−0.6
−0.8
−1.0
Drain–source voltage VDS (V)


C – VDS
Capacitance C (pF)
1000
500
300
100
50
30
10
0.1
1
10
100
Ciss
Coss
Crss
Common Source
Ta = 25°C
f = 1 MHz
VGS = 0 V
Drain–source voltage VDS (V)

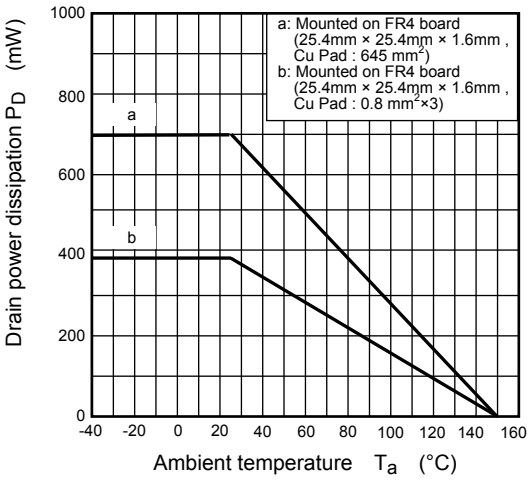

t – ID
Switching time t (ns)
1000
100
10
1
0.01
0.1
1
10
toff
tf
ton
tr
Common Source
VDD = 10 V
VGS = 0 to 2.5 V
Ta = 25°C
RG = 4.7 Ω
Drain current ID (A)


Dynamic Input Characteristic
Gate–Source voltage VGS (V)
10
8
6
4
2
0
0
4
8
12
Common Source
ID = 3 A
Ta = 25°C
VDD=15V
VDD=24V
Total Gate Charge Qg (nC)

$r_{th} - t_w$


Transient thermal impedance r_{th} (°C/W)
1000
100
10
1
0.001
0.01
0.1
1
10
100
1000
Pulse width t_w (s)
b
a
Single Pulse
a: Mounted on FR4 board
(25.4mm × 25.4mm × 1.6mm ,
Cu Pad : 645 mm²)
b: Mounted on FR4 board
(25.4mm × 25.4mm × 1.6mm ,
Cu Pad : 0.8 mm²×3)

$P_D - T_a$


Drain power dissipation P_D (mW)
1000
800
600
400
200
0
-40
-20
0
20
40
60
80
100
120
140
160
Ambient temperature T_a (°C)
a
b
a: Mounted on FR4 board
(25.4mm × 25.4mm × 1.6mm ,
Cu Pad : 645 mm²)
b: Mounted on FR4 board
(25.4mm × 25.4mm × 1.6mm ,
Cu Pad : 0.8 mm²×3)

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