

NPIC6C4894

Power logic 12-bit shift register; open-drain outputs

Rev. 1 — 17 April 2014

Product data sheet

1. General description

The NPIC6C4894 is a 12-stage serial shift register. It has a storage latch associated with each stage for strobing data from the serial input (D) to the parallel open-drain outputs (QP0 to QP11). Data is shifted on positive-going clock (CP) transitions. The data in each shift register stage is transferred to the storage register when the latch enable (LE) input is HIGH. Data in the storage register drives the gate of the output extended-drain NMOS transistor whenever the output enable input (OE) is HIGH. A LOW on OE causes the outputs to assume a high-impedance OFF-state. Operation of the OE input does not affect the state of the registers. Two serial outputs (QS1 and QS2) are available for cascading a number of NPIC6C4894 devices. Serial data is available at QS1 on positive-going clock edges to allow high-speed operation in cascaded systems with a fast clock rise time. The same serial data is available at QS2 on the next negative going clock edge. It is used for cascading NPIC6C4894 devices when the clock has a slow rise time. The open-drain outputs are 33 V/100 mA continuous current extended-drain NMOS transistors designed for use in systems that require moderate load power such as LEDs. Integrated voltage clamps in the outputs, provide protection against inductive transients. This protection makes the device suitable for power driver applications such as relays, solenoids and other low-current or medium-voltage loads.

2. Features and benefits

- Specified from $-40\text{ }^{\circ}\text{C}$ to $+125\text{ }^{\circ}\text{C}$
- Low R_{DSon}
- 12 Power EDNMOS transistor outputs of 100 mA continuous current
- 250 mA current limit capability
- Output clamping voltage 33 V
- 30 mJ avalanche energy capability
- Low power consumption
- Latch-up performance exceeds 100 mA per JESD 78 Class II level A
- ESD protection:
 - ◆ HBM JS-2011 Class 2 exceeds 2500 V
 - ◆ CDM JESD22-C101E exceeds 1000 V

3. Applications

- LED sign
- Graphic status panel
- Fault status indicator

4. Ordering information

Table 1. Ordering information

Type number	Package			Version
	Temperature range	Name	Description	
NPIC6C4894D	-40 °C to +125 °C	SO20	plastic small outline package; 20 leads; body width 7.5 mm	SOT163-1
NPIC6C4894PW	-40 °C to +125 °C	TSSOP20	plastic thin shrink small outline package; 20 leads; body width 4.4 mm	SOT360-1

5. Functional diagram

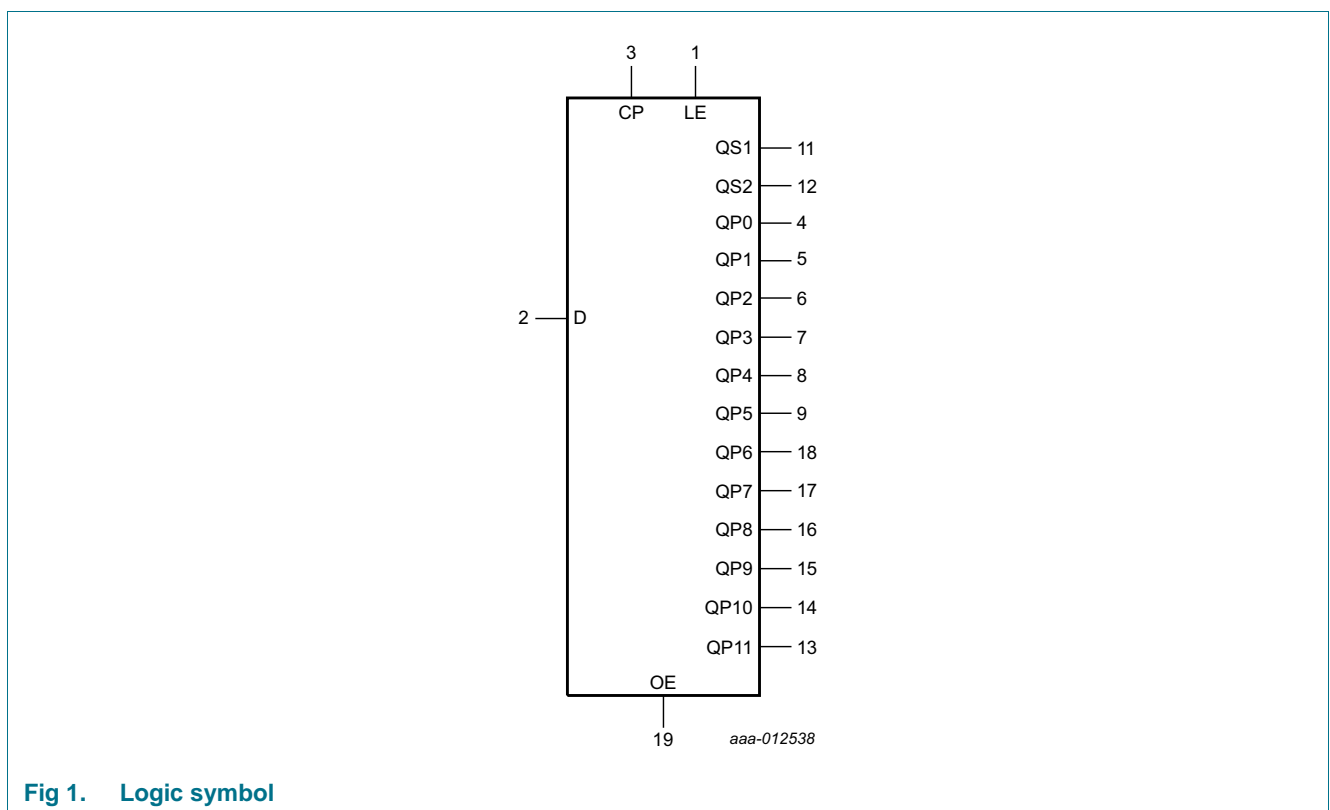
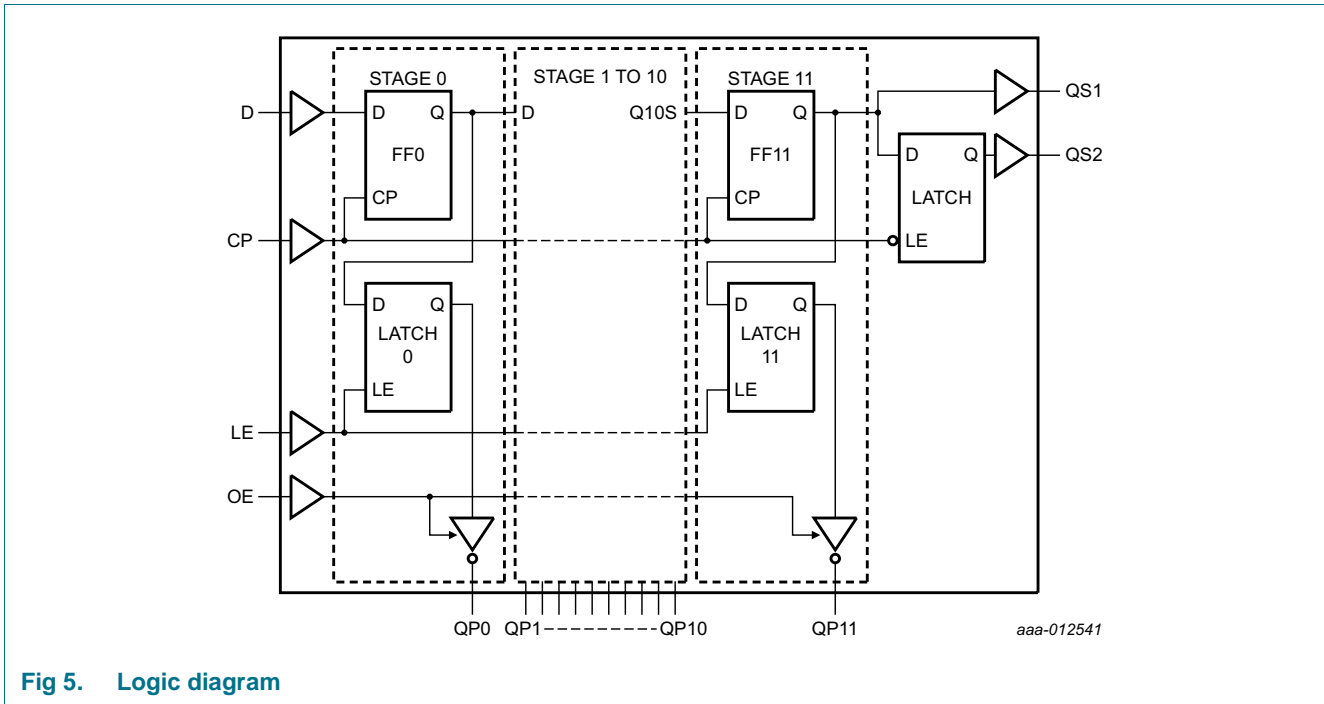
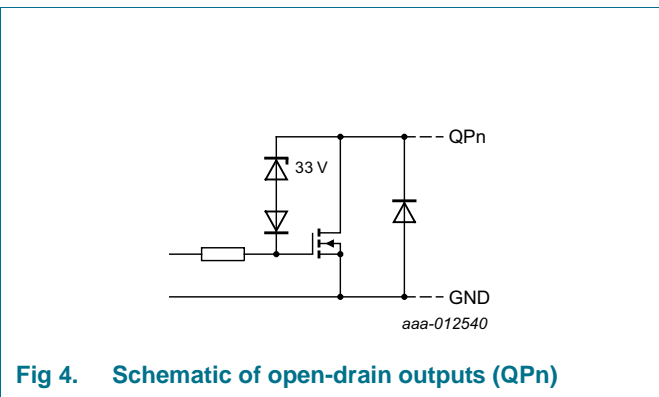
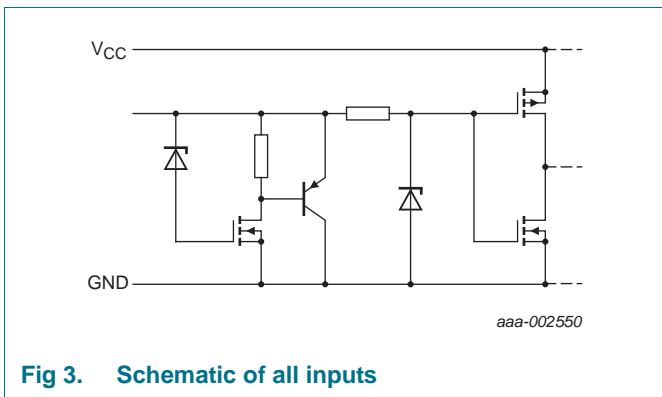
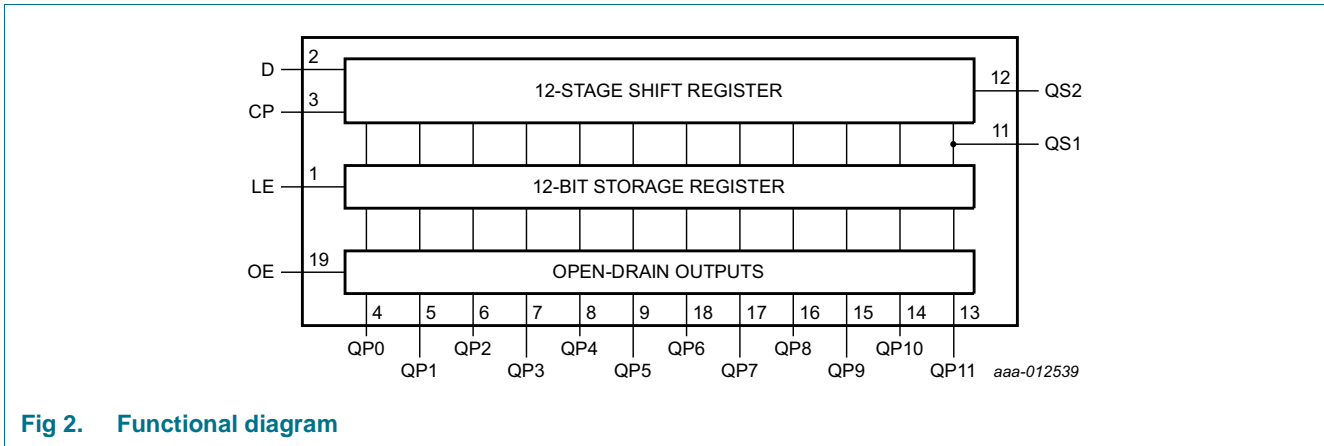


Fig 1. Logic symbol



6. Pinning information

6.1 Pinning

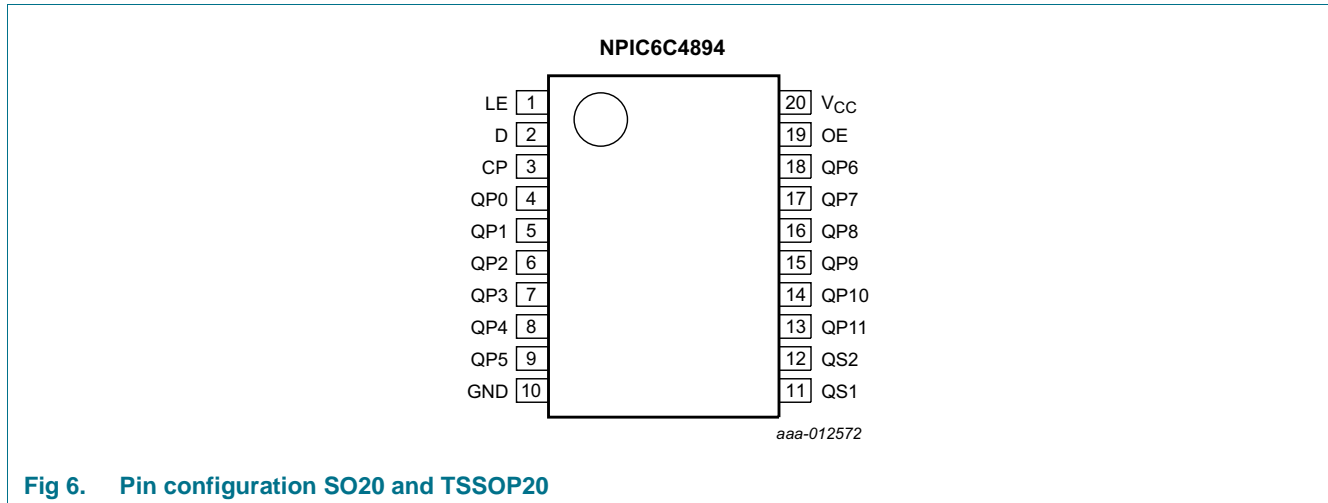


Fig 6. Pin configuration SO20 and TSSOP20

6.2 Pin description

Table 2. Pin description

Symbol	Pin	Description
LE	1	latch enable input
D	2	serial data input
CP	3	clock input
QP0 to QP11	4, 5, 6, 7, 8, 9, 18, 17, 16, 15, 14, 13	parallel output
GND	10	ground (0 V)
QS1	11	serial output
QS2	12	serial output
OE	19	output enable input
V _{CC}	20	supply voltage

7. Functional description

Table 3. Function table^[1]

At the positive clock edge, the information in the 10th register stage is transferred to the 11th register stage and the QS output

Control			Input	Parallel output		Serial output	
CP	OE	LE	D	QP0	QPn	QS1 ^[2]	QS2 ^[3]
↑	L	X	X	Z	Z	Q10S	no change
↓	L	X	X	Z	Z	no change	Q11S
↑	H	L	X	no change	no change	Q10S	no change
↑	H	H	L	Z	QPn-1	Q10S	no change
↑	H	H	H	L	QPn-1	Q10S	no change
↓	H	H	H	no change	no change	no change	Q11S

[1] H = HIGH voltage level; L = LOW voltage level; X = don't care; ↑ = LOW-to-HIGH clock transition; ↓ = HIGH-to-LOW clock transition; Z = high-impedance OFF-state.

[2] Q10S = the data in register stage 10 before the LOW to HIGH clock transition.

[3] Q11S = the data in register stage 11 before the HIGH to LOW clock transition.

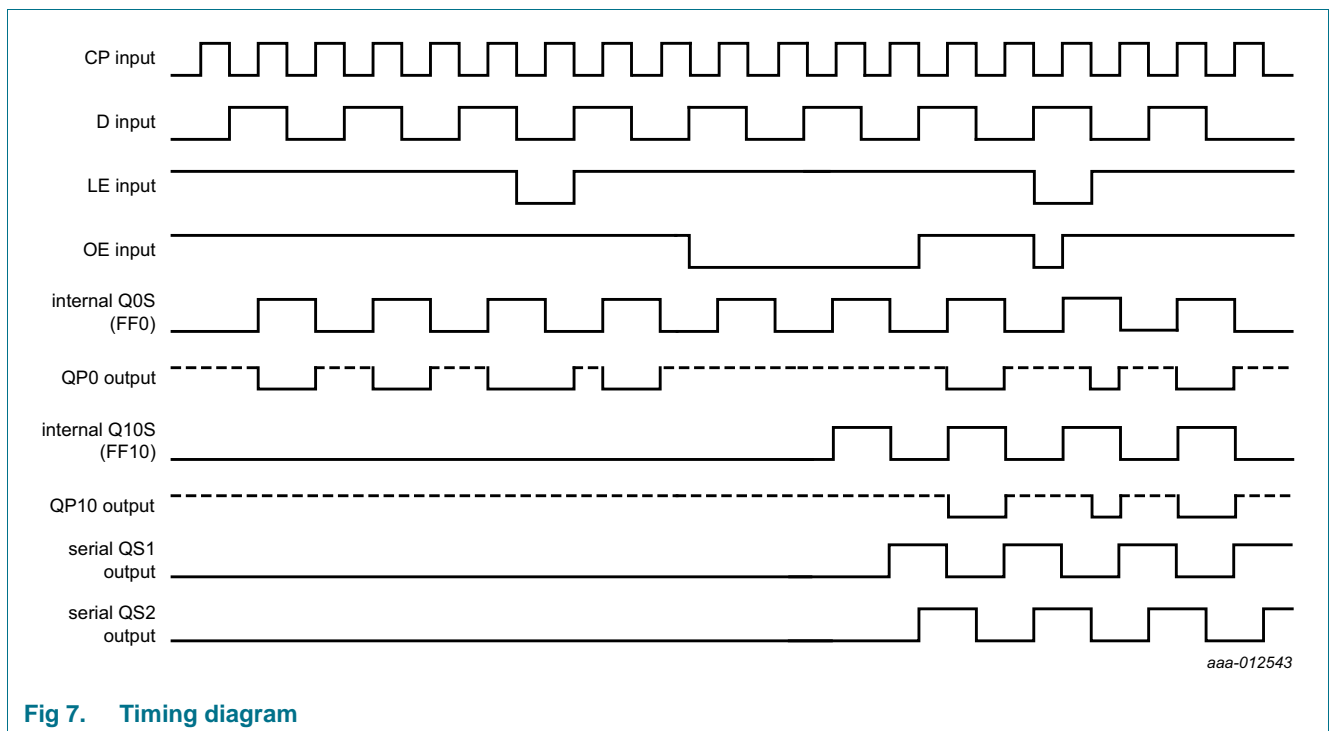


Fig 7. Timing diagram

8. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Max	Unit
V_{CC}	supply voltage		-0.5	+7.0	V
V_I	input voltage		-0.3	+7.0	V
V_{DS}	drain-source voltage	QPn [1]	-	+33	V
V_O	output voltage	QSn	-0.5	+7.0	V
I_{IK}	input clamping current	$V_I < 0.5 \text{ V}$ or $V_I > V_{CC} + 0.5 \text{ V}$	-	± 50	mA
I_{OK}	output clamping current	QSn; $V_O < 0.5 \text{ V}$ or $V_O > V_{CC} + 0.5 \text{ V}$	-	± 100	mA
$I_{d(SD)}$	source-drain diode current	continuous	-	250	mA
		pulsed [2]	-	500	mA
I_D	drain current	$T_{amb} = 25 \text{ }^\circ\text{C}$			
		continuous; each output; all outputs on	-	100	mA
		pulsed; each output; all outputs on [2]	-	250	mA
I_{DM}	peak drain current	single output; $T_{amb} = 25 \text{ }^\circ\text{C}$	[2]	250	mA
E_{AS}	non-repetitive avalanche energy	single pulse; see Figure 8 and Figure 16	[3]	30	mJ
I_{AL}	avalanche current	see Figure 8 and Figure 16	[3]	200	mA
T_{stg}	storage temperature		-65	+150	$^\circ\text{C}$
P_{tot}	total power dissipation	$T_{amb} = 25 \text{ }^\circ\text{C}$	[4]		
		SO20	-	1500	mW
		TSSOP20	-	1250	mW
		$T_{amb} = 125 \text{ }^\circ\text{C}$	[4]		
		SO20	-	300	mW
		TSSOP20	-	250	mW

[1] Each power EDNMOS source is internally connected to GND.

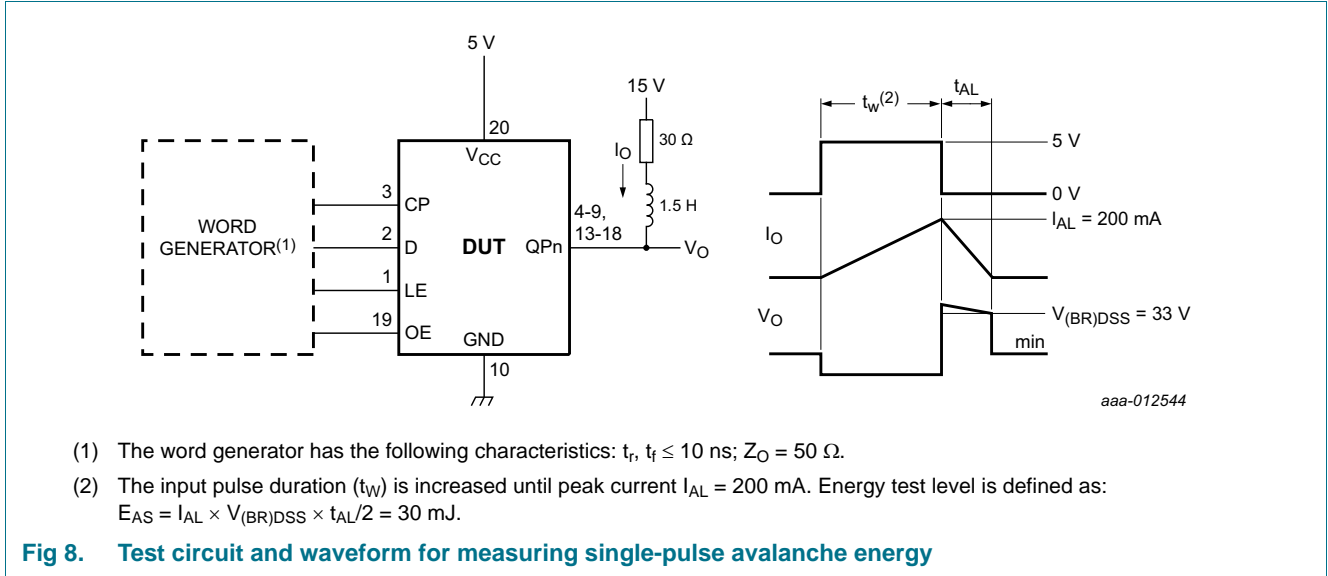
[2] Pulse duration $\leq 100 \mu\text{s}$ and duty cycle $\leq 2 \%$.

[3] $V_{DS} = 15 \text{ V}$; starting junction temperature (T_j) = $25 \text{ }^\circ\text{C}$; $L = 1.5 \text{ H}$; avalanche current (I_{AL}) = 200 mA.

[4] For SO20 package: above $25 \text{ }^\circ\text{C}$ the value of P_{tot} derates linearly with $12 \text{ mW}/^\circ\text{C}$.

For TSSOP20 package: above $25 \text{ }^\circ\text{C}$ the value of P_{tot} derates linearly with $10 \text{ mW}/^\circ\text{C}$.

8.1 Test circuit and waveform



9. Recommended operating conditions

Table 5. Recommended operating conditions

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{CC}	supply voltage		4.5	5.0	5.5	V
V_I	input voltage		0	-	5.5	V
I_D	drain current	pulsed drain output current; $V_{CC} = 5$ V; $T_{amb} = 25$ °C; all outputs on	[1][2]	-	250	mA
T_{amb}	ambient temperature		-40	-	+125	°C

[1] Pulse duration ≤ 100 μ s and duty cycle ≤ 2 %.

[2] Technique should limit $T_j - T_{amb}$ to 10 °C maximum.

10. Static characteristics

Table 6. Static characteristics

At recommended operating conditions unless otherwise specified; Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	T _{amb} = 25 °C			T _{amb} = -40 °C to 125 °C			Unit
			Min	Typ	Max	Min	Typ	Max	
V _{IH}	HIGH-level input voltage		0.85V _{CC}	-	-	-	-	-	V
V _{IL}	LOW-level input voltage		-	-	0.15V _{CC}	-	-	-	V
V _{OH}	HIGH-level output voltage	QSn; V _I = V _{IH} or V _{IL}							
		I _O = -20 μA; V _{CC} = 4.5 V	4.4	4.49	-	-	-	-	V
		I _O = -4 mA; V _{CC} = 4.5 V	4.0	4.2	-	-	-	-	V
V _{OL}	LOW-level output voltage	QSn; V _I = V _{IH} or V _{IL}							
		I _O = 20 μA; V _{CC} = 4.5 V	-	0.005	0.1	-	-	-	V
		I _O = 4 mA; V _{CC} = 4.5 V	-	0.3	0.5	-	-	-	V
I _I	input leakage current	V _{CC} = 5.5 V; V _I = V _{CC} or GND	-	-	±1	-	-	-	μA
V _{(BR)DSS}	drain-source breakdown voltage	QPn; I _O = 1 mA	33	37	-	-	-	-	V
V _{SD}	source-drain voltage	QPn; I _O = 100 mA	-1.2	-0.85	-	-	-	-	V
I _{CC}	supply current	V _{CC} = 5.5 V; V _I = V _{CC} or GND							
		OE = LOW	-	0.006	200	-	-	-	μA
		OE = HIGH	-	0.01	500	-	-	-	μA
		OE = LOW; CP = 5 MHz; see Figure 15 and Figure 17	-	1	5	-	-	-	mA
I _O	output current	QPn; V _O = 0.5 V [1][2][3]	-	140	-	-	-	-	mA
I _{OZ}	OFF-state output current	QPn; V _{CC} = 5.5 V; V _{DS} = 30 V	-	0.002	0.2	-	0.15	0.3	μA
R _{DSon}	drain-source on-state resistance	see Figure 18 and Figure 19 [1][2]							
		V _{CC} = 4.5 V; I _O = 50 mA	-	2.7	9	-	4.3	12	Ω
		V _{CC} = 4.5 V; I _O = 100 mA	-	2.8	10	-	-	-	Ω

[1] Technique should limit T_j - T_{amb} to 10 °C maximum.

[2] These parameters are measured with voltage-sensing contacts separate from the current-carrying contacts.

[3] The output current is defined for a consistent comparison between devices from different sources. It is the current that produces a voltage drop of 0.5 V.

11. Dynamic characteristics

Table 7. Dynamic characteristics

At recommended operating conditions unless otherwise specified; Voltages are referenced to GND (ground = 0 V); For test circuit, see [Figure 15](#).

Symbol	Parameter	Conditions	T _{amb} = 25 °C			Unit
			Min	Typ	Max	
t _{pd}	propagation delay	CP to QSn; see Figure 9 ^[1]	-	5	-	ns
t _{TLH}	LOW to HIGH output transition time	QPn; see Figure 12	-	60	-	ns
		QSn; see Figure 9	-	6	-	ns
t _{THL}	HIGH to LOW output transition time	QPn; see Figure 12	-	18	-	ns
		QSn; see Figure 9	-	6	-	ns
t _{PLZ}	LOW to OFF-state propagation delay	CP, LE and OE to QPn; I _O = 75 mA; see Figure 10 , Figure 11 , Figure 12 and Figure 20	-	105	-	ns
t _{PZL}	OFF-state to LOW propagation delay	CP, LE and OE to QPn; I _O = 75 mA; see Figure 10 , Figure 11 , Figure 12 and Figure 20	-	10	-	ns
f _{clk(max)}	maximum clock frequency	CP; see Figure 9 ^[2]	10	-	-	MHz
t _{su}	set-up time	D to CP; see Figure 13	20	-	-	ns
t _h	hold time	D to CP; see Figure 13	20	-	-	ns
t _W	pulse width	CP, LE; see Figure 9 and Figure 11	40	-	-	ns
t _{rr}	reverse recovery time	I _O = -100 mA; dI/dt = 10 A/μs; see Figure 14 ^{[3][4]}	-	120	-	ns
t _a	reverse recovery current rise time	I _O = -100 mA; dI/dt = 10 A/μs; see Figure 14 ^{[3][4]}	-	100	-	ns

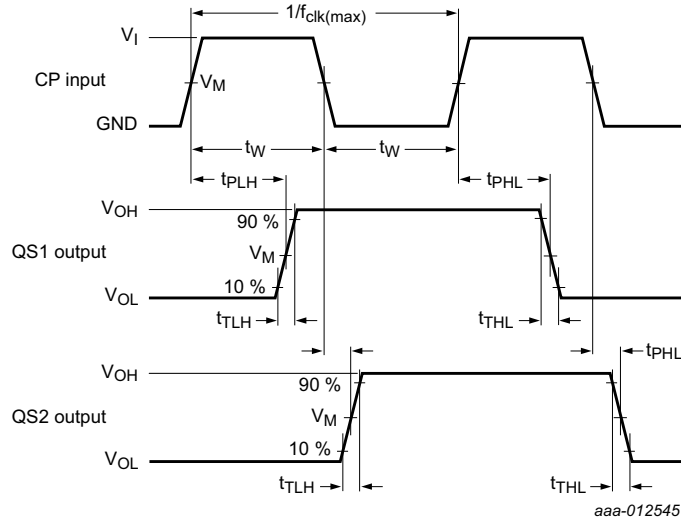
[1] t_{pd} is the same as t_{PLH} and t_{PHL}.

[2] This is the maximum serial clock frequency assuming cascaded operation where serial data is passed from one stage to a second stage. The clock period allows for CP → QSn propagation delay and setup time plus some timing margin.

[3] Technique should limit T_J - T_{amb} to 10 °C maximum.

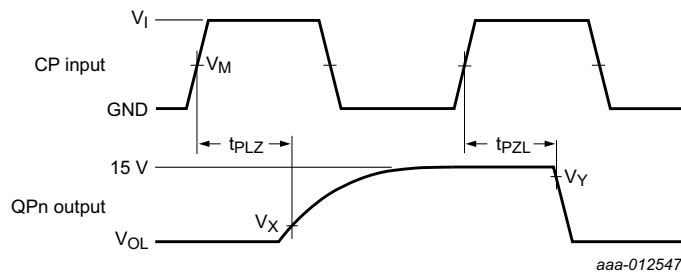
[4] These parameters are measured with voltage-sensing contacts separate from the current-carrying contacts.

11.1 Waveforms and test circuits



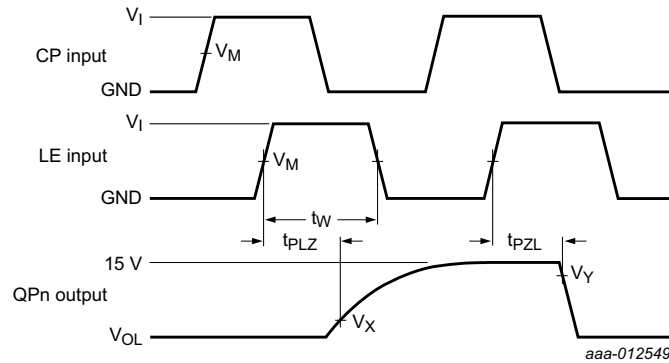
Measurement points are given in [Table 8](#).
 V_{OL} and V_{OH} are typical output voltage levels that occur with the output load.

Fig 9. Propagation delay clock (CP) to output (QS1, QS2), clock pulse width, maximum clock frequency and output transition time



Measurement points are given in [Table 8](#).
 V_{OL} and V_{OH} are typical output voltage levels that occur with the output load.

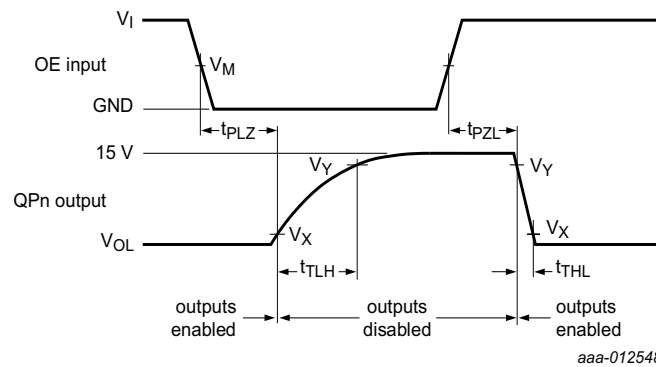
Fig 10. Propagation delay clock (CP) to output (QPn)



Measurement points are given in [Table 8](#).

V_{OL} is the typical output voltage level that occurs with the output load.

Fig 11. Latch enable (LE) to output (QPn) propagation delays and the latch enable pulse width



Measurement points are given in [Table 8](#).

V_{OL} is the typical output voltage level that occurs with the output load.

Fig 12. Output enable (OE) to output (QPn) and output transition time

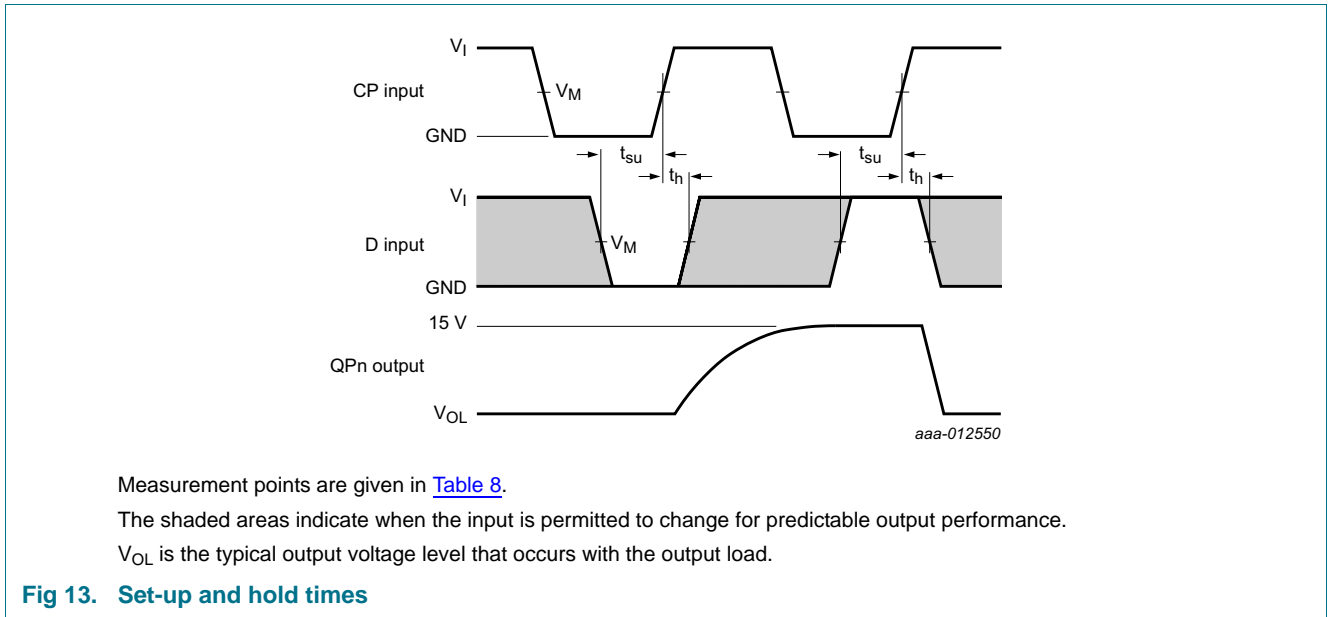
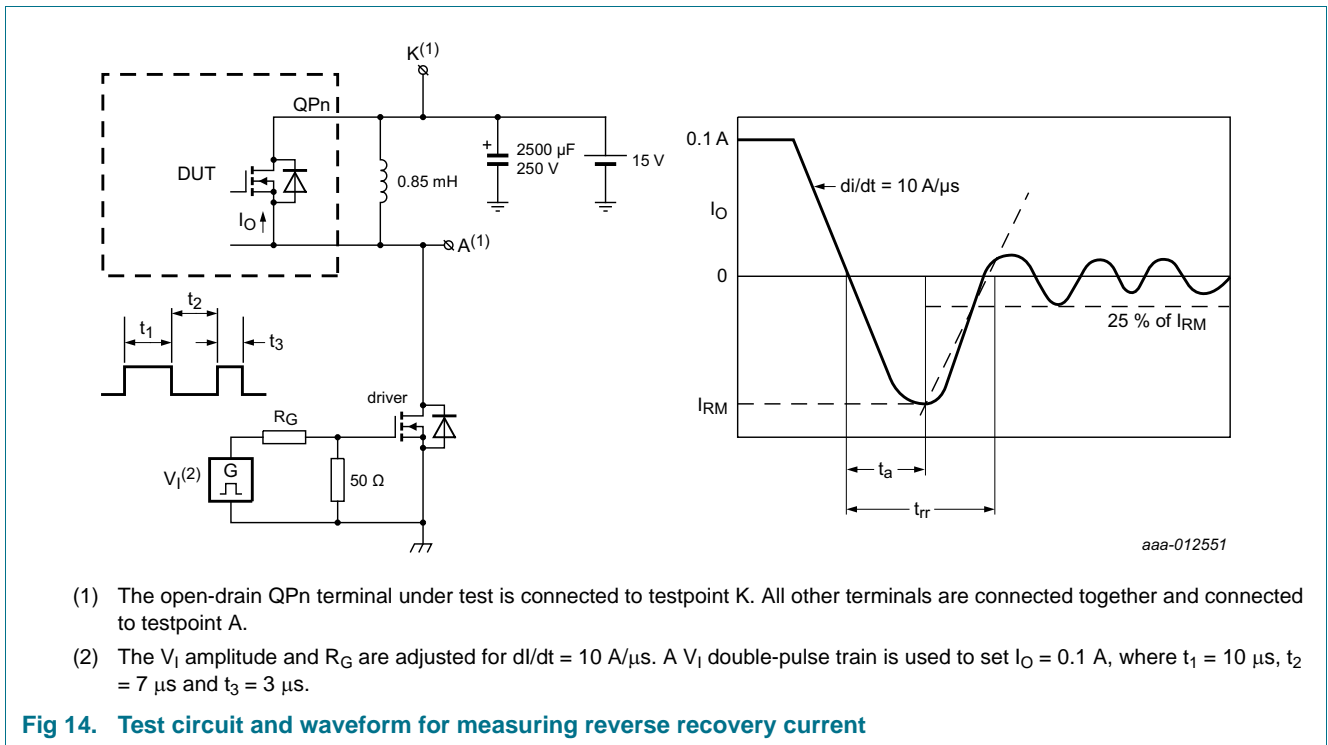


Table 8. Measurement points

Supply voltage	Input	Output		
V_{CC}	V_M	V_M	V_X	V_Y
5 V	$0.5V_{CC}$	$0.5V_{DS}$	$0.1V_{DS}$	$0.9V_{DS}$



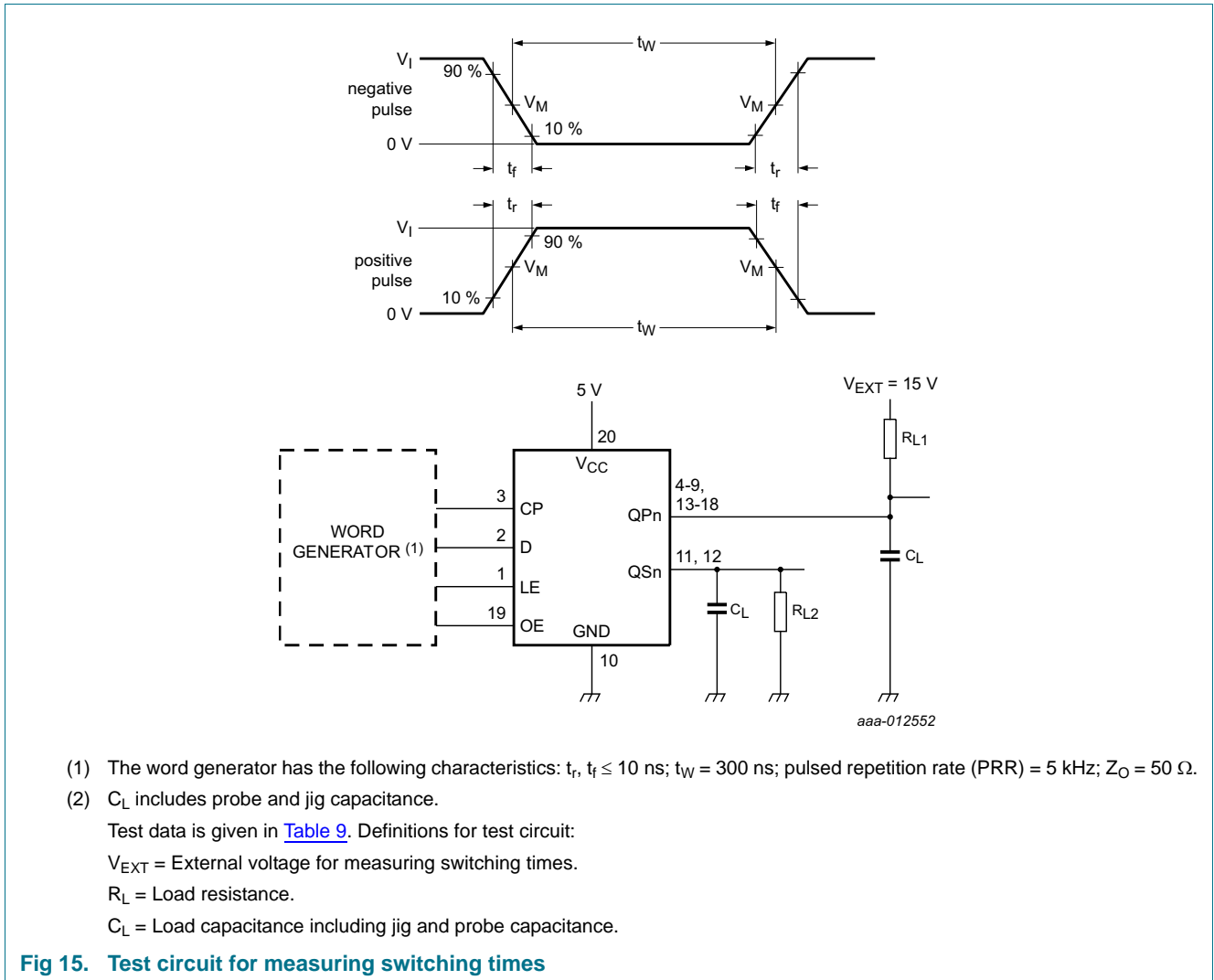
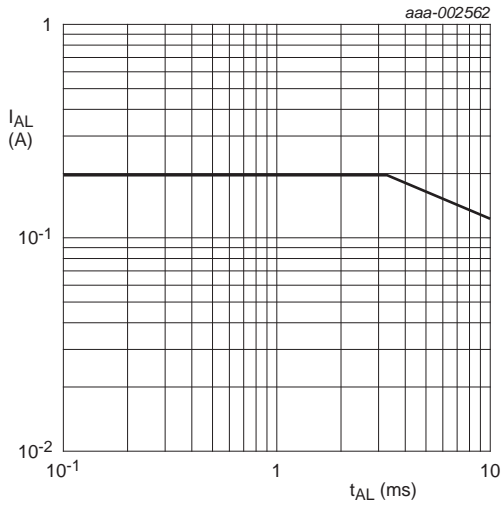


Table 9. Test data

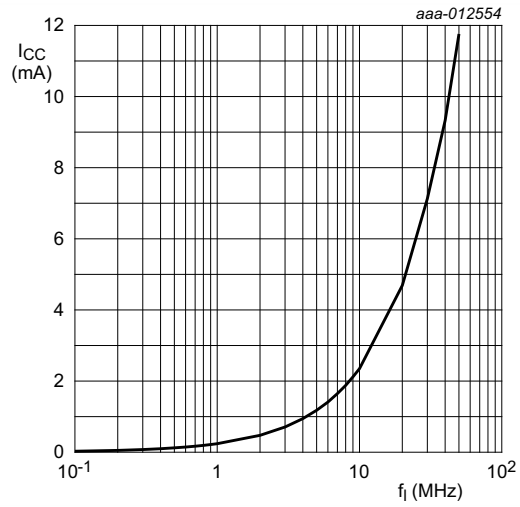
Supply voltage	Input			Load		
	V_I	t_r, t_f	V_M	C_L	R_{L1}	R_{L2} ^[1]
5 V	5 V	≤ 10 ns	50%	30 pF	200 Ω	2 k Ω

[1] Do not connect R_{L2} when measuring the supply current (I_{CC}).



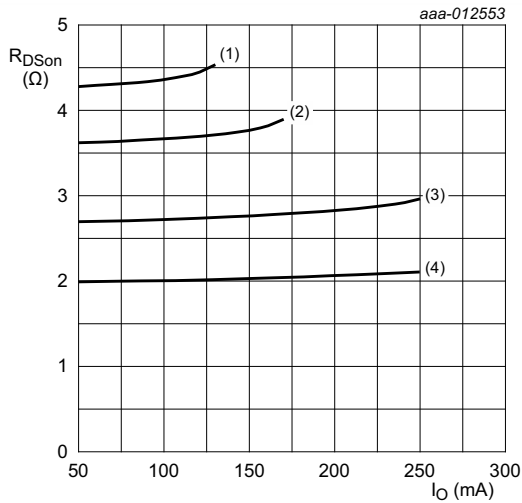
$T_{amb} = 25\text{ }^{\circ}\text{C}; V_{CC} = 5\text{ V.}$

Fig 16. Avalanche current (peak) versus time duration of avalanche



$T_{amb} = -40\text{ }^{\circ}\text{C to } 125\text{ }^{\circ}\text{C}; V_{CC} = 5\text{ V.}$

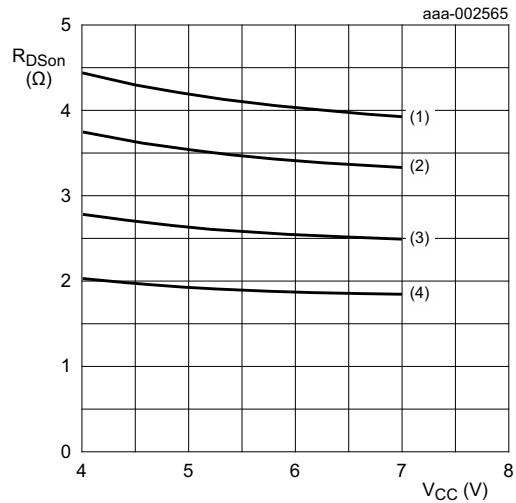
Fig 17. Supply current versus frequency



$V_{CC} = 4.5\text{ V}; V_I = V_{CC}\text{ or GND.}$

- (1) $T_{amb} = 125\text{ }^{\circ}\text{C}$
- (2) $T_{amb} = 85\text{ }^{\circ}\text{C}$
- (3) $T_{amb} = 25\text{ }^{\circ}\text{C}$
- (4) $T_{amb} = -40\text{ }^{\circ}\text{C}$

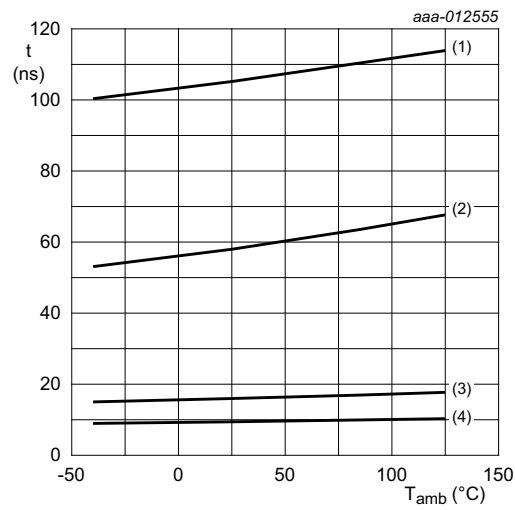
Fig 18. Drain-source on-state resistance versus drain current



$V_I = V_{CC}\text{ or GND}; I_O = 50\text{ mA.}$

- (1) $T_{amb} = 125\text{ }^{\circ}\text{C}$
- (2) $T_{amb} = 85\text{ }^{\circ}\text{C}$
- (3) $T_{amb} = 25\text{ }^{\circ}\text{C}$
- (4) $T_{amb} = -40\text{ }^{\circ}\text{C}$

Fig 19. Static drain-source on-state resistance versus supply voltage



$V_{CC} = 5\text{ V}$; $I_O = 75\text{ mA}$, this technique should limit $T_j - T_{amb}$ to 10 °C maximum.

- (1) t_{PLZ} .
- (2) t_{TLH} .
- (3) t_{THL} .
- (4) t_{PZL} .

Fig 20. Switching time versus temperature

12. Package outline

SO20: plastic small outline package; 20 leads; body width 7.5 mm

SOT163-1

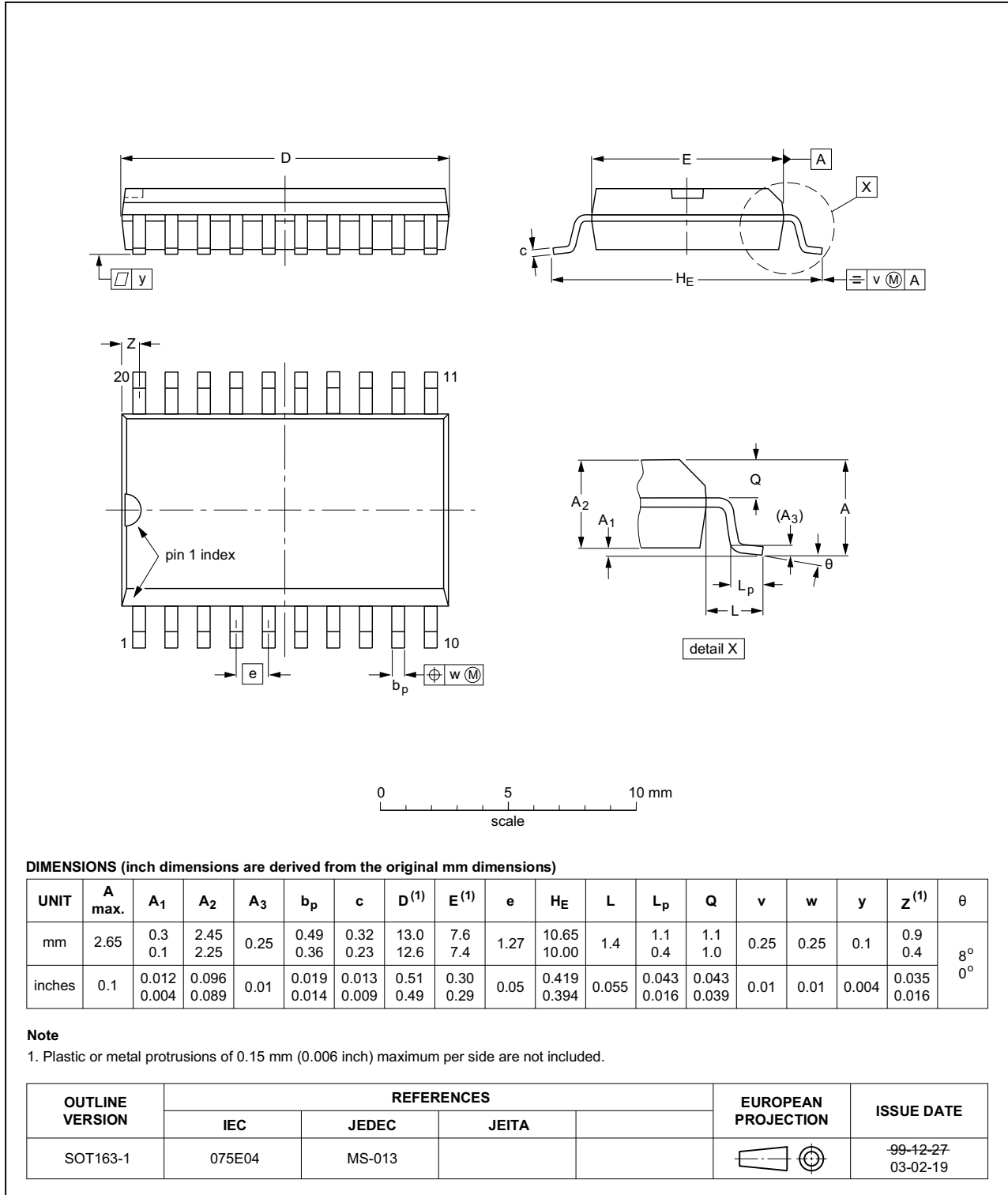


Fig 21. Package outline SOT163-1 (SO20)

TSSOP20: plastic thin shrink small outline package; 20 leads; body width 4.4 mm

SOT360-1

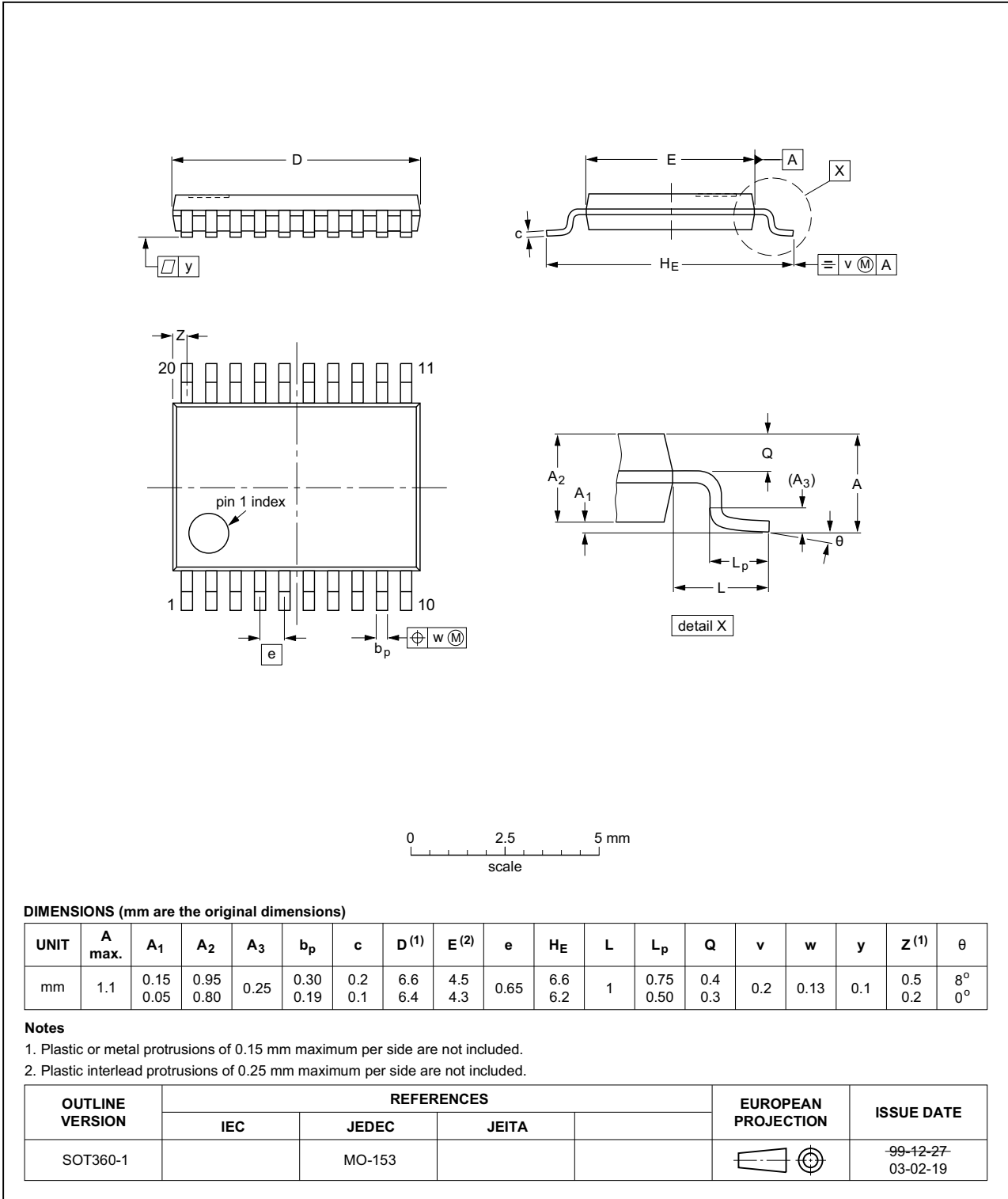


Fig 22. Package outline SOT360-1 (TSSOP20)

13. Abbreviations

Table 10. Abbreviations

Acronym	Description
CDM	Charged Device Model
CMOS	Complementary Metal Oxide Semiconductor
DUT	Device Under Test
EDNMOS	Extended Drain Negative Metal Oxide Semiconductor
ESD	ElectroStatic Discharge
HBM	Human Body Model
TTL	Transistor-Transistor Logic

14. Revision history

Table 11. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
NPIC6C4894 v.1	20140417	Product data sheet	-	-

15. Legal information

15.1 Data sheet status

Document status ^{[1][2]}	Product status ^[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL <http://www.nexperia.com>.

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For sales office addresses, please send an email to: salesaddresses@nexperia.com

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