

IGBT SIP Module (Ultrafast IGBT)



IMS-2

PRIMARY CHARACTERISTICS	
OUTPUT CURRENT IN A TYPICAL 20 kHz MOTOR DRIVE	
V_{CES}	600 V
I_{RMS} per phase (2.1 kW total) with $T_C = 90\text{ }^\circ\text{C}$	7.1 A_{RMS}
T_J	125 $^\circ\text{C}$
Supply voltage	360 V_{DC}
Power factor	0.8
Modulation depth (see fig. 1)	115 %
$V_{CE(on)}$ (typical) at $I_C = 6.8\text{ A}$, 25 $^\circ\text{C}$	1.7 V
Speed	8 kHz to 30 kHz
Package	SIP
Circuit configuration	Three phase inverter

FEATURES

- Fully isolated printed circuit board mount package
- Switching-loss rating includes all “tail” losses
- HEXFRED® soft ultrafast diodes
- Optimized for medium speed, see fig. 1 for current vs. frequency curve
- UL approved file E78996
- Designed and qualified for industrial level
- Material categorization: for definitions of compliance please see www.vishay.com/doc?99912


**RoHS
COMPLIANT**

DESCRIPTION

The IGBT technology is the key to Vishay’s Semiconductors advanced line of IMS (Insulated Metal Substrate) power modules. These modules are more efficient than comparable bipolar transistor modules, while at the same time having the simpler gate-drive requirements of the familiar power MOSFET. This superior technology has now been coupled to a state of the art materials system that maximizes power throughput with low thermal resistance. This package is highly suited to motor drive applications and where space is at a premium.

ABSOLUTE MAXIMUM RATINGS				
PARAMETER	SYMBOL	TEST CONDITIONS	MAX.	UNITS
Collector to emitter voltage	V_{CES}		600	V
Continuous collector current, each IGBT	I_C	$T_C = 25\text{ }^\circ\text{C}$	13	A
		$T_C = 100\text{ }^\circ\text{C}$	6.8	
Pulsed collector current	$I_{CM}^{(1)}$		40	
Clamped inductive load current	$I_{LM}^{(2)}$		40	
Diode continuous forward current	I_F	$T_C = 100\text{ }^\circ\text{C}$	6.1	
Diode maximum forward current	I_{FM}		40	
Gate to emitter voltage	V_{GE}		± 20	V
Isolation voltage	V_{ISOL}	Any terminal to case, $t = 1\text{ min}$	2500	V_{RMS}
Maximum power dissipation, each IGBT	P_D	$T_C = 25\text{ }^\circ\text{C}$	36	W
		$T_C = 100\text{ }^\circ\text{C}$	14	
Operating junction and storage temperature range	T_J, T_{Stg}		-40 to +150	$^\circ\text{C}$
Soldering temperature		For 10 s, (0.063" (1.6 mm) from case)	300	
Mounting torque		6-32 or M3 screw	5 to 7 (0.55 to 0.8)	lbf · in (N · m)

Notes

(1) Repetitive rating; $V_{GE} = 20\text{ V}$, pulse width limited by maximum junction temperature (see fig. 20)

(2) $V_{CC} = 80\% (V_{CES})$, $V_{GE} = 20\text{ V}$, $L = 10\text{ }\mu\text{H}$, $R_G = 23\text{ }\Omega$ (see fig. 19)



THERMAL AND MECHANICAL SPECIFICATIONS				
PARAMETER	SYMBOL	TYP.	MAX.	UNITS
Junction-to-case, each IGBT, one IGBT in conduction	R_{thJC} (IGBT)	-	3.5	°C/W
Junction-to-case, each diode, one diode in conduction	R_{thJC} (DIODE)	-	5.5	
Case to sink, flat, greased surface	R_{thCS} (MODULE)	0.10	-	
Weight of module		20	-	g
		0.7	-	oz.

ELECTRICAL SPECIFICATIONS ($T_J = 25\text{ }^\circ\text{C}$ unless otherwise specified)							
PARAMETER	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNITS	
Collector to emitter breakdown voltage	$V_{(BR)CES}$ ⁽¹⁾	$V_{GE} = 0\text{ V}, I_C = 250\text{ }\mu\text{A}$	600	-	-	V	
Temperature coeff. of breakdown voltage	$\Delta V_{(BR)CES}/\Delta T_J$	$V_{GE} = 0\text{ V}, I_C = 1.0\text{ mA}$	-	0.63	-	V/°C	
Collector to emitter saturation voltage	$V_{CE(on)}$	$I_C = 6.8\text{ A}$	$V_{GE} = 15\text{ V}$ See fig. 2, 5	-	1.70	2.2	V
		$I_C = 13\text{ A}$		-	2.00	-	
		$I_C = 6.8\text{ A}, T_J = 150\text{ }^\circ\text{C}$		-	1.70	-	
Gate threshold voltage	$V_{GE(th)}$	$V_{CE} = V_{GE}, I_C = 250\text{ }\mu\text{A}$	3.0	-	6.0	mV/°C	
Temperature coeff. of threshold voltage	$\Delta V_{GE(th)}/\Delta T_J$		-	-11	-		
Forward transconductance	g_{fe} ⁽²⁾	$V_{CE} = 100\text{ V}, I_C = 6.8\text{ A}$	4.0	6.0	-	S	
Zero gate voltage collector current	I_{CES}	$V_{GE} = 0\text{ V}, V_{CE} = 600\text{ V}$	-	-	250	μA	
		$V_{GE} = 0\text{ V}, V_{CE} = 600\text{ V}, T_J = 150\text{ }^\circ\text{C}$	-	-	2500		
Diode forward voltage drop	V_{FM}	$I_C = 12\text{ A}$	See fig. 13	-	1.4	1.7	V
		$I_C = 12\text{ A}, T_J = 150\text{ }^\circ\text{C}$		-	1.3	1.6	
Gate to emitter leakage current	I_{GES}	$V_{GE} = \pm 20\text{ V}$	-	-	± 100	nA	

Notes

- (1) Pulse width $\leq 80\text{ }\mu\text{s}$, duty factor $\leq 0.1\%$
- (2) Pulse width $5.0\text{ }\mu\text{s}$; single shot

SWITCHING CHARACTERISTICS ($T_J = 25\text{ }^\circ\text{C}$ unless otherwise specified)							
PARAMETER	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNITS	
Total gate charge (turn-on)	Q_g	$I_C = 6.8\text{ A}$ $V_{CC} = 400\text{ V}$ See fig. 8	-	53	79	nC	
Gate to emitter charge (turn-on)	Q_{ge}		-	7.7	12		
Gate to collector charge (turn-on)	Q_{gc}		-	21	31		
Turn-on delay time	$t_{d(on)}$	$T_J = 25\text{ }^\circ\text{C}$ $I_C = 6.8\text{ A}, V_{CC} = 480\text{ V}$ $V_{GE} = 15\text{ V}, R_G = 23\text{ }\Omega$ Energy losses include "tail" and diode reverse recovery. See fig. 9, 10, 11, 18	-	43	-	ns	
Rise time	t_r		-	14	-		
Turn-off delay time	$t_{d(off)}$		-	95	140		
Fall time	t_f		-	83	190		
Turn-on switching loss	E_{on}		-	0.17	-		mJ
Turn-off switching loss	E_{off}		-	0.15	-		
Total switching loss	E_{ts}	-	0.32	0.45			
Turn-on delay time	$t_{d(on)}$	$T_J = 150\text{ }^\circ\text{C}$ $I_C = 6.8\text{ A}, V_{CC} = 480\text{ V}$ $V_{GE} = 15\text{ V}, R_G = 23\text{ }\Omega$ Energy losses include "tail" and diode reverse recovery See fig. 9, 10, 11, 18	-	41	-	ns	
Rise time	t_r		-	16	-		
Turn-off delay time	$t_{d(off)}$		-	110	-		
Fall time	t_f		-	230	-		
Total switching loss	E_{ts}		-	0.52	-		mJ
Input capacitance	C_{ies}		$V_{GE} = 0\text{ V}$	-	1100		-
Output capacitance	C_{oes}	$V_{CC} = 30\text{ V}$	-	73	-		
Reverse transfer capacitance	C_{res}	$f = 1.0\text{ MHz}$ See fig. 7	-	14	-		
Diode reverse recovery time	t_{rr}	$T_J = 25\text{ }^\circ\text{C}$	See fig. 14	-	42	60	ns
		$T_J = 125\text{ }^\circ\text{C}$		-	83	120	
Diode peak reverse recovery charge	I_{rr}	$T_J = 25\text{ }^\circ\text{C}$	See fig. 15	-	3.5	6.0	A
		$T_J = 125\text{ }^\circ\text{C}$		-	5.6	10	
Diode reverse recovery charge	Q_{rr}	$T_J = 25\text{ }^\circ\text{C}$	See fig. 16	-	80	180	nC
		$T_J = 125\text{ }^\circ\text{C}$		-	220	600	
Diode peak rate of fall of recovery during t_b	$dl_{(rec)M}/dt$	$T_J = 25\text{ }^\circ\text{C}$	See fig. 17	-	180	-	A/ μs
		$T_J = 125\text{ }^\circ\text{C}$		-	116	-	

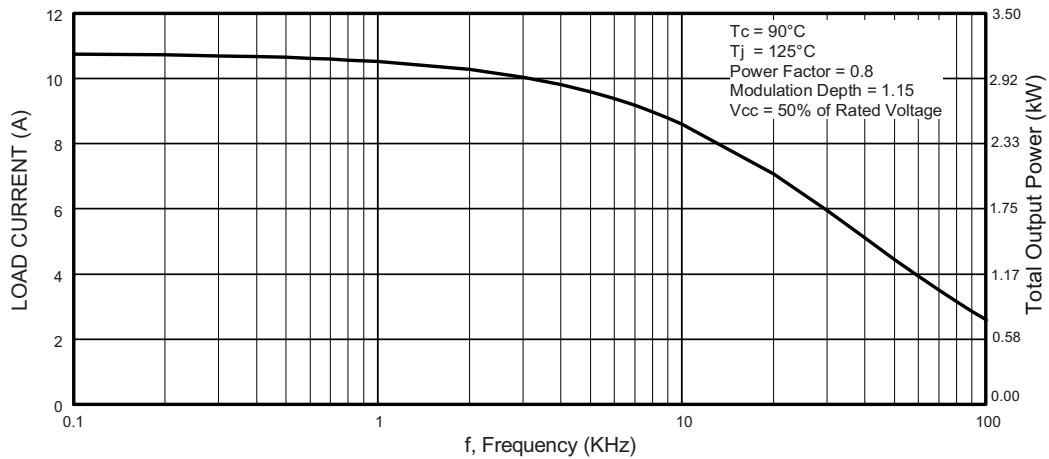


Fig. 1 - Typical Load Current vs. Frequency
(Load Current = I_{RMS} of Fundamental)

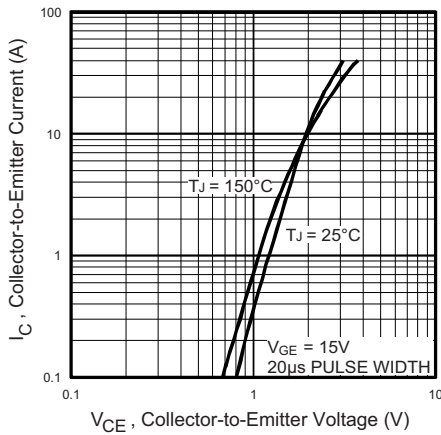


Fig. 2 - Typical Output Characteristics

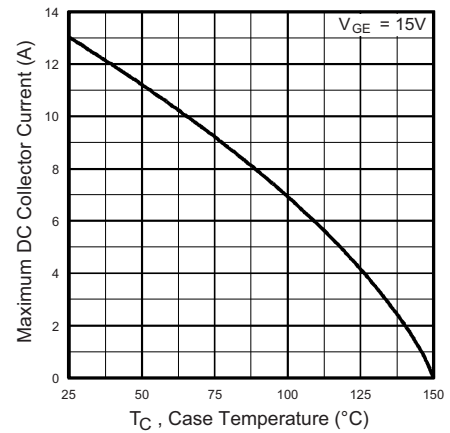


Fig. 4 - Maximum Collector Current vs. Case Temperature

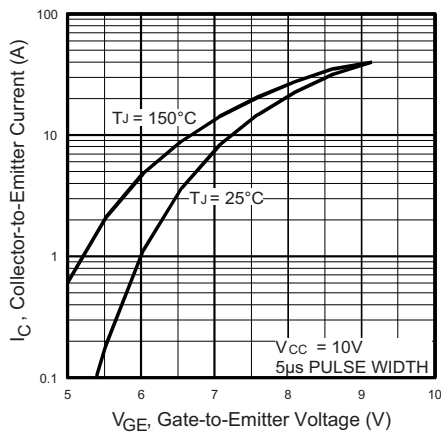


Fig. 3 - Typical Transfer Characteristics

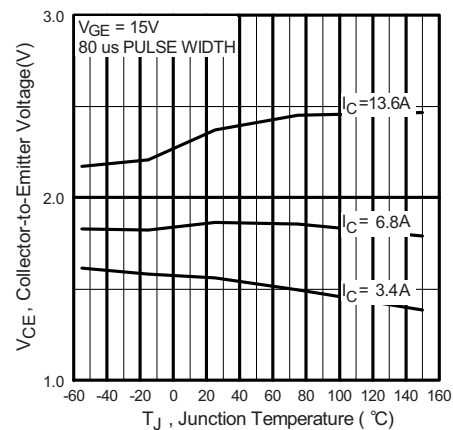


Fig. 5 - Typical Collector to Emitter Voltage vs. Junction Temperature

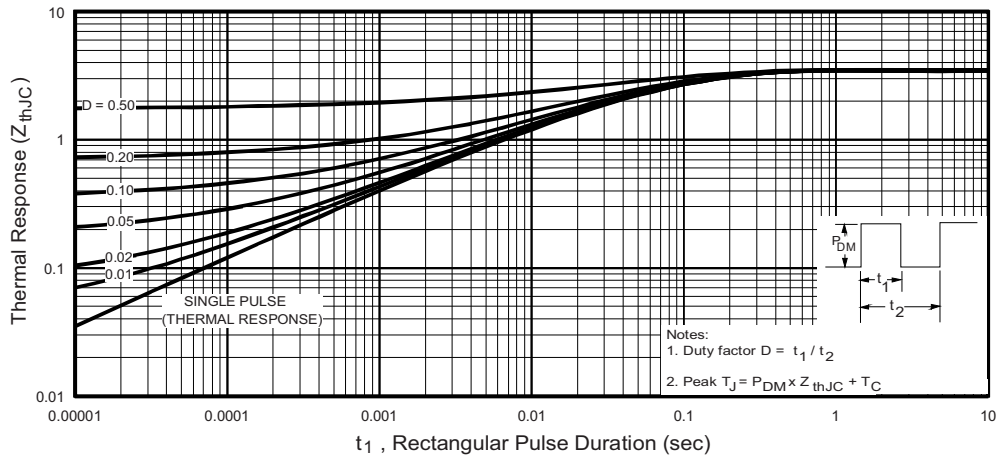


Fig. 6 - Maximum Effective Transient Thermal Impedance, Junction to Case

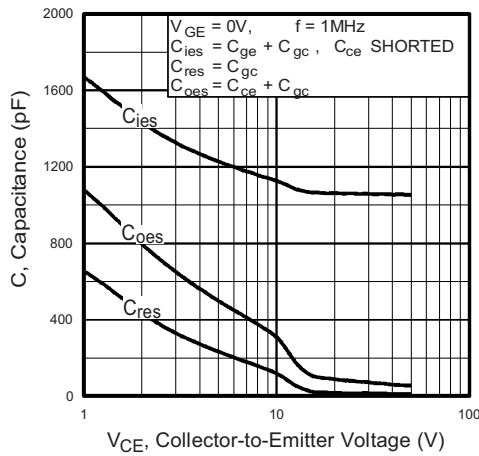


Fig. 7 - Typical Capacitance vs. Collector to Emitter Voltage

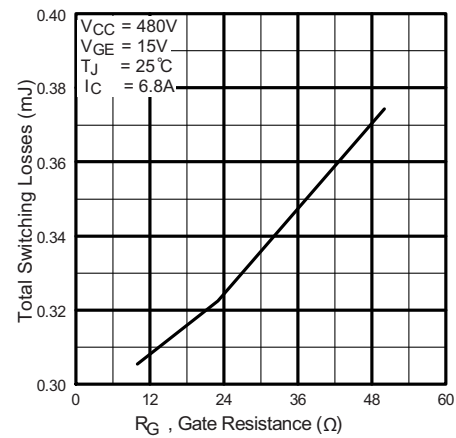


Fig. 9 - Typical Switching Losses vs. Gate Resistance

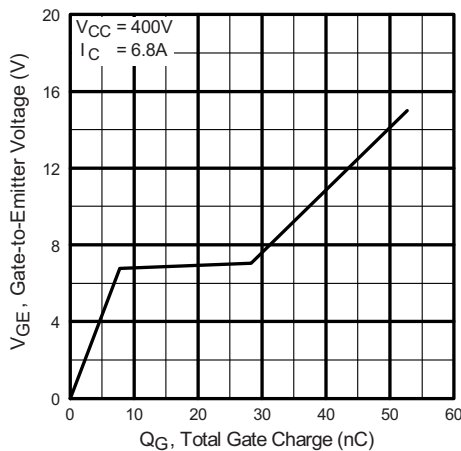


Fig. 8 - Typical Gate Charge vs. Gate to Emitter Voltage

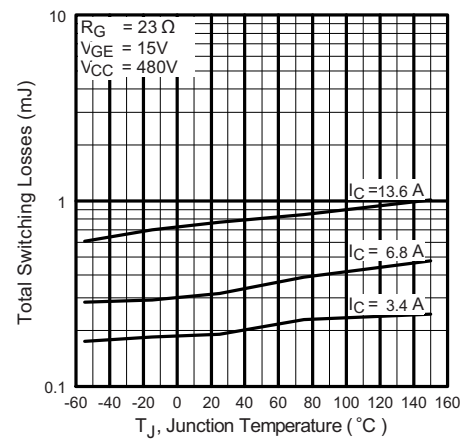


Fig. 10 - Typical Switching Losses vs. Junction Temperature

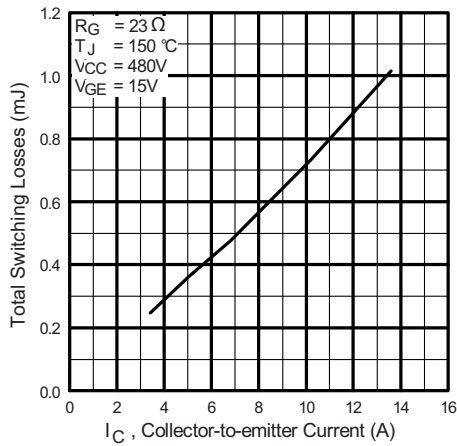


Fig. 11 - Typical Switching Losses vs. Collector to Emitter Current

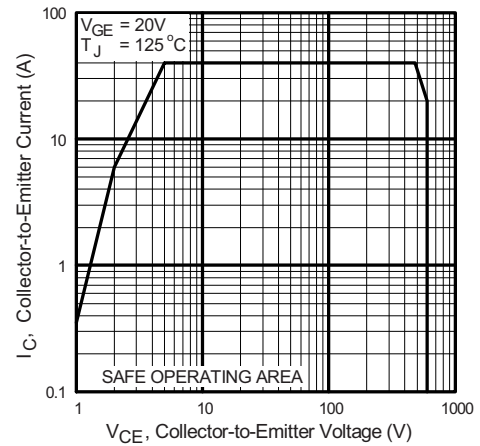


Fig. 12 - Turn-Off SOA

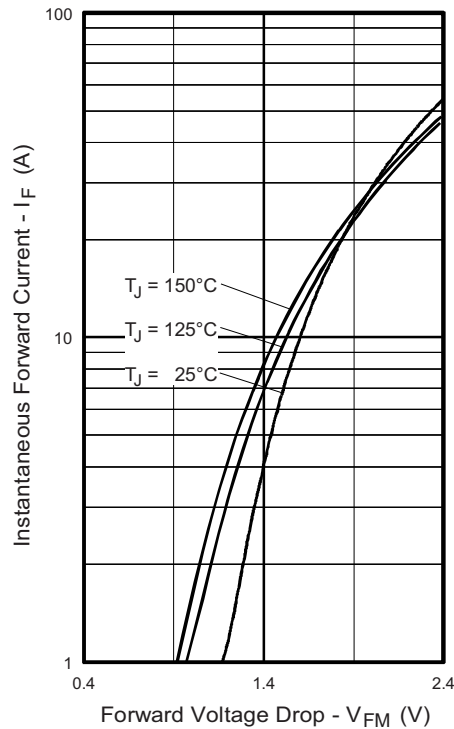


Fig. 13 - Maximum Forward Voltage Drop vs. Instantaneous Forward Current

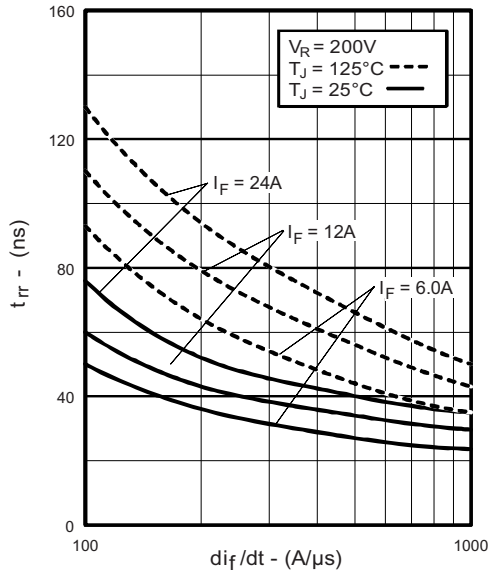


Fig. 14 - Typical Reverse Recovery Time vs. di_F/dt

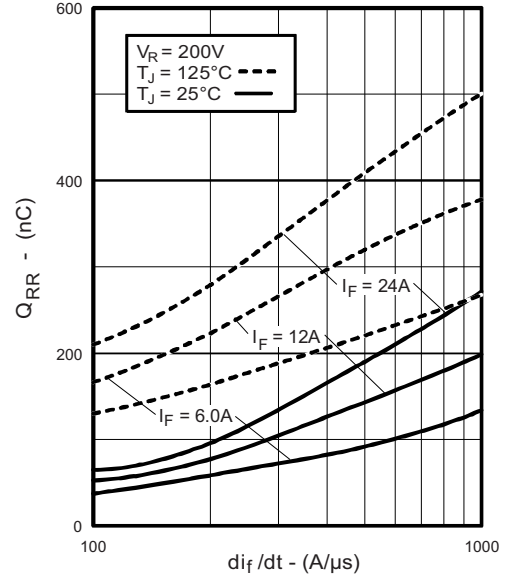


Fig. 16 - Typical Stored Charge vs. di_F/dt

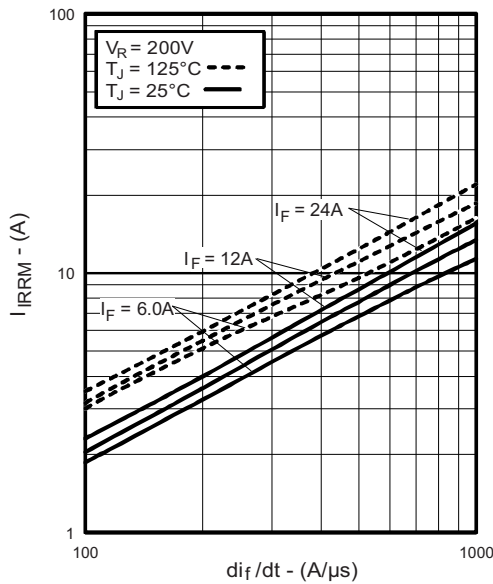


Fig. 15 - Typical Recovery Current vs. di_F/dt

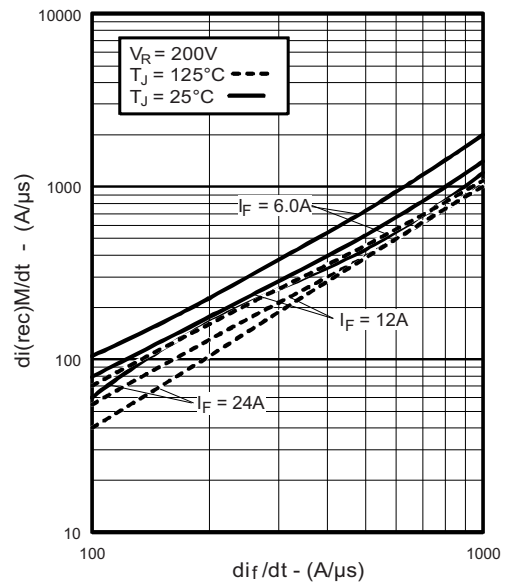


Fig. 17 - Typical $di_{(rec)M}/dt$ vs di_F/dt

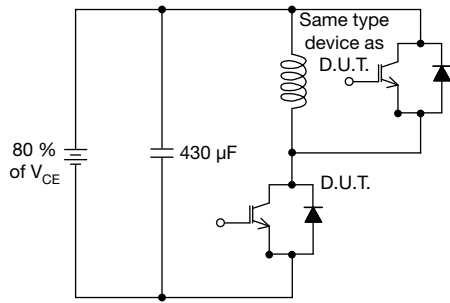


Fig. 18a - Test Circuit for Measurements of I_{LM} , E_{on} , $E_{off(diode)}$, t_{rr} , Q_{rr} , I_{rr} , $t_{d(on)}$, t_r , $t_{d(off)}$, t_f

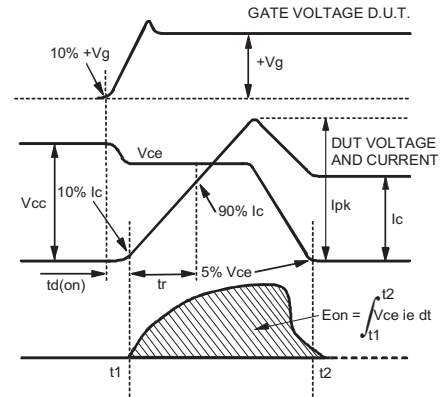


Fig. 18c - Test Waveforms for Circuit of Fig. 18a, Defining E_{on} , $t_{d(on)}$, t_r

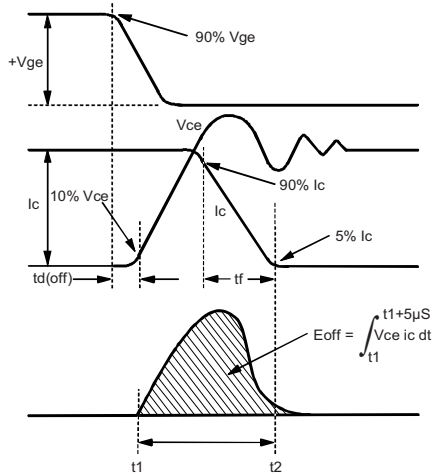


Fig. 18b - Test Waveforms for Circuit of Fig. 18a, Defining E_{off} , $t_{d(off)}$, t_f

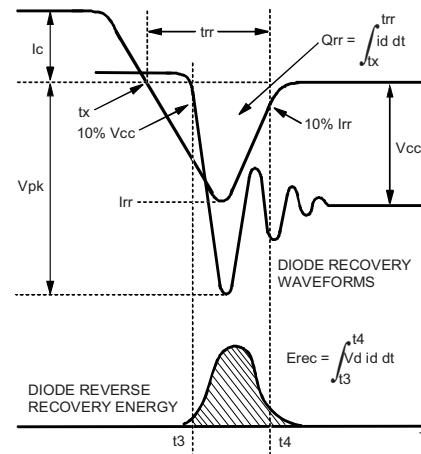


Fig. 18d - Test Waveforms for Circuit of Fig. 18a, Defining E_{rec} , t_{rr} , Q_{rr} , I_{rr}

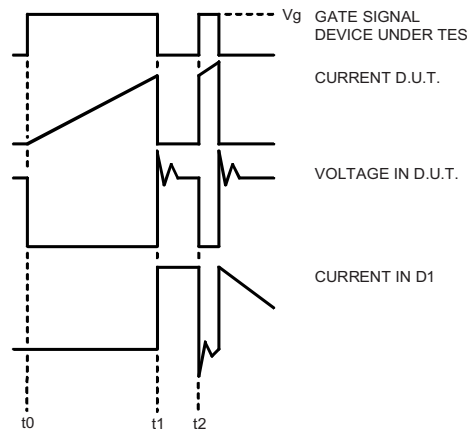


Fig. 18e - Macro Waveforms for Figure 18a's Test Circuit

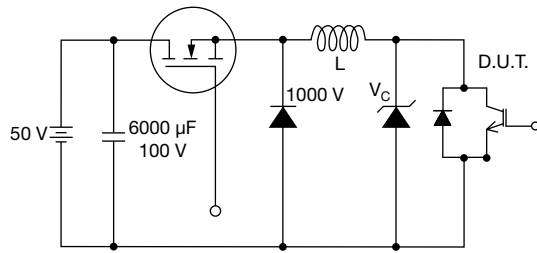


Fig. 19 - Clamped Inductive Load Test Circuit

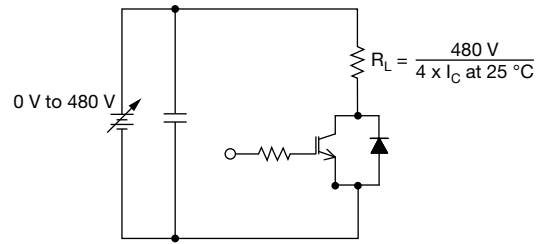
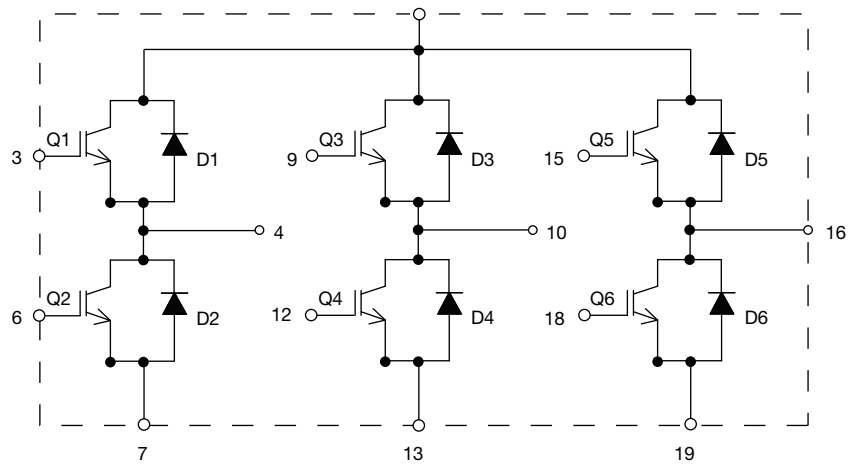


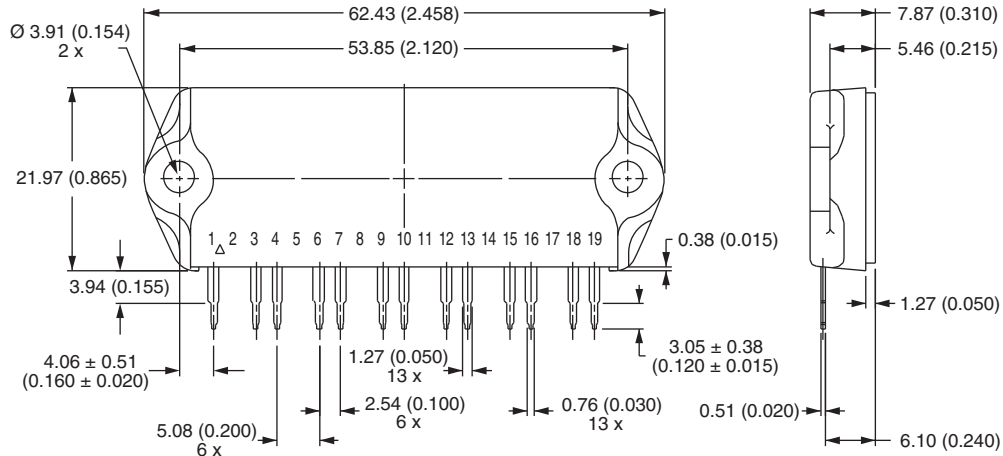
Fig. 20 - Pulsed Collector Current Test Circuit

CIRCUIT CONFIGURATION

LINKS TO RELATED DOCUMENTS

Dimensions	www.vishay.com/doc?95066
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IMS-2 (SIP)

DIMENSIONS in millimeters (inches)



IMS-2 Package Outline (13 Pins)

Notes

- (1) Tolerance unless otherwise specified ± 0.254 mm (0.010")
- (2) Controlling dimension: inch
- (3) Terminal numbers are shown for reference only



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