# CY7C1021BN

# 1-Mbit (64 K × 16) Static RAM

## Features

- Temperature ranges
  - Commercial: 0 °C to 70 °C
  - Industrial: –40 °C to 85 °C
  - Automotive-A: –40 °C to 85 °C
  - Automotive-E: –40 °C to 125 °C
- High speed
  - $t_{AA}$ = 15 ns (Automotive)
- Complementary metal oxide semiconductor (CMOS) for optimum speed/power
- Low active power
  - 825 mW (maximum)
- Automatic power down when deselected
- Independent control of upper and lower bits
- Available in Pb-free and non Pb-free 44-pin TSOP II and 44-pin 400-mil-wide SOJ

## Functional Description

The CY7C1021BN is a high performance CMOS static RAM organized as 65,536 words by 16 bits. This device has an automatic power down feature that significantly reduces power consumption when deselected.

Writing to the device is accomplished by taking Chip Enable ($\overline{CE}$) and Write Enable ($\overline{WE}$) inputs LOW. If Byte Low Enable ($\overline{BLE}$) is LOW, then data from the input/output (I/O) pins ($I/O_1$ through $I/O_8$), is written into the location specified on the address pins ($A_0$ through $A_{15}$). If Byte High Enable ($\overline{BHE}$) is LOW, then data from I/O pins ($I/O_9$ through $I/O_{16}$) is written into the location specified on the address pins ($A_0$ through $A_{15}$).

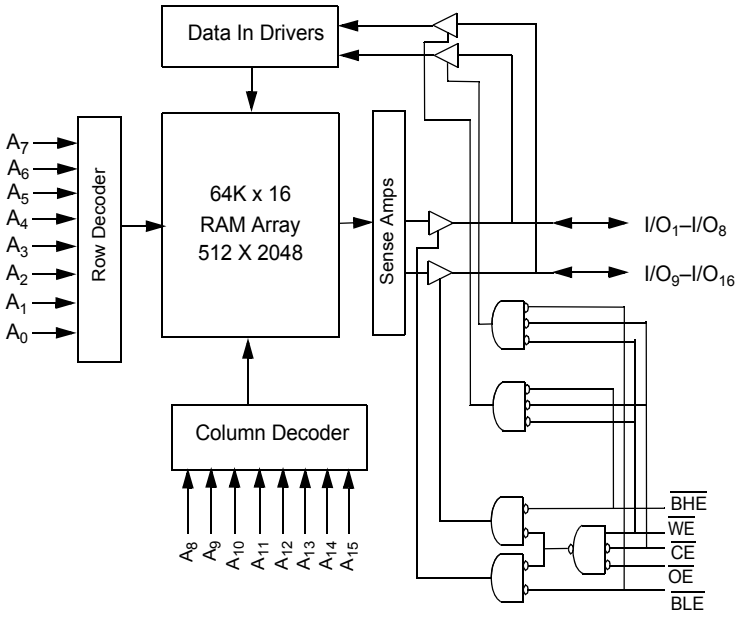
Reading from the device is accomplished by taking $\overline{CE}$ and Output Enable ($\overline{OE}$) LOW while forcing $\overline{WE}$ HIGH. If $\overline{BLE}$ is LOW, then data from the memory location specified by the address pins appears on $I/O_1$ to $I/O_8$. If $\overline{BHE}$ is LOW, then data from memory appears on $I/O_9$ to $I/O_{16}$. See the Truth Table on page 11 for a complete description of read and write modes.

The I/O pins ($I/O_1$ through $I/O_{16}$) are placed in a high impedance state when the device is deselected ($\overline{CE}$ HIGH), the outputs are disabled ($\overline{OE}$ HIGH), the $\overline{BHE}$ and $\overline{BLE}$ are disabled ($\overline{BHE}$, $\overline{BLE}$ HIGH), or during a write operation ($\overline{CE}$ LOW, $\overline{WE}$ LOW).

The CY7C1021BN is available in standard 44-pin TSOP type II and 44-pin 400-mil-wide SOJ packages. Use part number CY7C1021BN when ordering 15 ns $t_{AA}$.

For a complete list of related resources, click here.

## Logic Block Diagram



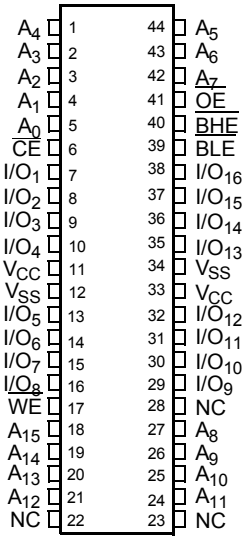
## Contents

## Selection Guide

| Description | | CY7C1021B-15 |
|---|---|---|
| Maximum access time (ns) | | 15 |
| Maximum operating current (mA) | Commercial/Industrial | 130 |
| | Automotive-A | 130 |
| | Automotive-E | 130 |
| Maximum CMOS standby current (mA) | Commercial/Industrial | 10 |
| | Commercial/Industrial (L version) | 0.5 |
| | Automotive-A (L version) | 0.5 |
| | Automotive-E | 15 |

## Pin Configuration

**Figure 1. 44-pin SOJ/TSOP II pinout (Top View)**



## Pin Definitions

| Pin Name | Pin Number | I/O Type | Description |
|---|---|---|---|
| $A_0$–$A_{15}$ | 1–5,18–21, 24–27, 42–44 | Input | Address inputs used to select one of the address locations. |
| $I/O_1$–$I/O_{16}$ | 7–10, 13–16, 29–32, 35–38 | Input/Output | Bidirectional data I/O lines. Used as input or output lines depending on operation. |
| NC | 22, 23, 28 | No Connect | Not connected to the die. |
| $\overline{WE}$ | 17 | Input/Control | Write enable input, active LOW. When selected LOW, a write is conducted. When deselected HIGH, a read is conducted. |
| $\overline{CE}$ | 6 | Input/Control | Chip enable input, active LOW. When LOW, selects the chip. When HIGH, deselects the chip. |
| $\overline{BHE}$, $\overline{BLE}$ | 40, 39 | Input/Control | Byte enable select inputs, active LOW. $\overline{BHE}$ controls $I/O_{16}$–$I/O_9$, $\overline{BLE}$ controls $I/O_8$–$I/O_1$. |
| $\overline{OE}$ | 41 | Input/Control | Output enable, active LOW. Controls the direction of the I/O pins. When LOW, the I/O pins are allowed to behave as outputs. When deasserted HIGH, I/O pins are tristated, and act as input data pins. |
| $V_{SS}$ | 12, 34 | Ground | Ground for the device. Should be connected to ground of the system. |
| $V_{CC}$ | 11, 33 | Power Supply | Power supply inputs to the device. |

## Maximum Ratings

Exceeding the maximum ratings may impair the useful life of the device. These user guidelines are not tested.

Storage temperature ..... –65 °C to +150 °C

Ambient temperature with power applied ..... –55 °C to +125 °C

Supply voltage on $V_{CC}$ relative to GND [1] .....–0.5 V to +7.0 V

DC voltage applied to outputs in High Z state [1] .....–0.5 V to $V_{CC}$ + 0.5 V

DC input voltage [1] .....–0.5 V to $V_{CC}$ + 0.5 V

Current into outputs (LOW) ..... 20 mA

Static discharge voltage (per MIL-STD-883, Method 3015) ..... > 2001 V

Latch-up current ..... > 200 mA

## Operating Range

| Range | Ambient Temperature ($T_A$)[2] | $V_{CC}$ |
|---|---|---|
| Commercial | 0 °C to +70 °C | 5 V ± 10% |
| Industrial | –40 °C to +85 °C | |
| Automotive-A | –40 °C to +85 °C | |
| Automotive-E | –40 °C to +125 °C | |

## Electrical Characteristics

Over the operating range

| Parameter | Description | Test Conditions | | -15 | | Unit |
|---|---|---|---|---|---|---|
| | | | | Min | Max | |
| $V_{OH}$ | Output HIGH voltage | $V_{CC}$ = Min, $I_{OH}$ = –4.0 mA | | 2.4 | – | V |
| $V_{OL}$ | Output LOW voltage | $V_{CC}$ = Min, $I_{OL}$ = 8.0 mA | | – | 0.4 | V |
| $V_{IH}$ | Input HIGH voltage | | | 2.2 | 6.0 | V |
| $V_{IL}$ | Input LOW voltage[1] | | | –0.5 | 0.8 | V |
| $I_{IX}$ | Input leakage current | GND ≤ $V_I$ ≤ $V_{CC}$ | Commercial / Industrial | –1 | +1 | µA |
| | | | Automotive-A | –1 | +1 | µA |
| | | | Automotive-E | –4 | +4 | µA |
| $I_{OZ}$ | Output leakage current | GND ≤ $V_I$ ≤ $V_{CC}$, Output Disabled | Commercial / Industrial | –1 | +1 | µA |
| | | | Automotive-A | –1 | +1 | µA |
| | | | Automotive-E | –4 | +4 | µA |
| $I_{CC}$ | $V_{CC}$ operating supply current | $V_{CC}$ = Max, $I_{OUT}$ = 0 mA, f = $f_{MAX}$ = $1/t_{RC}$ | Commercial / Industrial | – | 130 | mA |
| | | | Automotive-A | – | 130 | |
| | | | Automotive-E | – | 130 | |
| $I_{SB1}$ | Automatic CE power down current – TTL inputs | Max $V_{CC}$, $\overline{CE}$ ≥ $V_{IH}$, $V_{IN}$ ≥ $V_{IH}$ or $V_{IN}$ ≤ $V_{IL}$, f = $f_{MAX}$ | Commercial / Industrial | – | 40 | mA |
| | | | Automotive-A | – | 40 | |
| | | | Automotive-E | – | 50 | |
| $I_{SB2}$ | Automatic CE power down current – CMOS inputs | Max $V_{CC}$, $\overline{CE}$ ≥ $V_{CC}$ – 0.3 V, $V_{IN}$ ≥ $V_{CC}$ – 0.3 V, or $V_{IN}$ ≤ 0.3 V, f = 0 | Commercial / Industrial | – | 10 | mA |
| | | | Commercial / Industrial (L) | – | 0.5 | |
| | | | Automotive-A (L) | – | 0.5 | |
| | | | Automotive-E | – | 15 | |

**Notes**
1. $V_{IL}$ (min.) = –2.0 V and $V_{IH}$(max) = $V_{CC}$ + 0.5 V for pulse durations of less than 20 ns.
2. $T_A$ is the “Instant On” case temperature.

## Capacitance

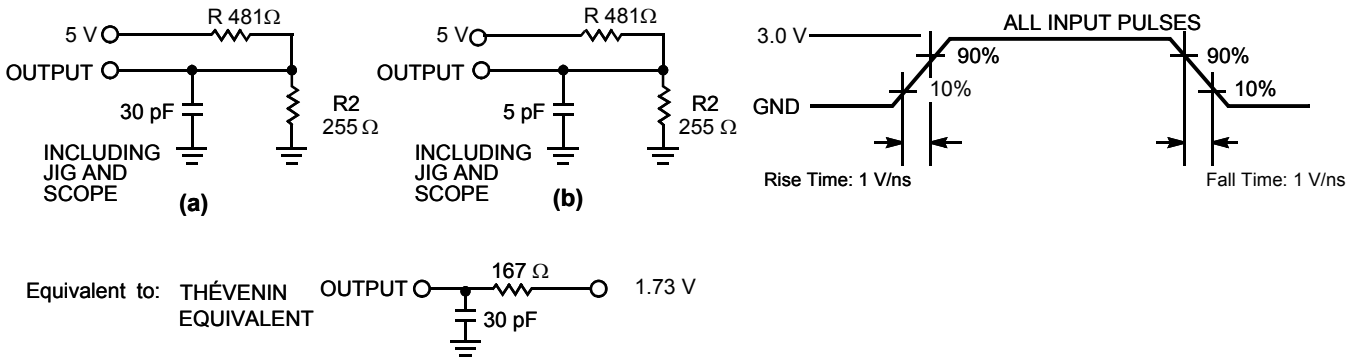
| Parameter [3] | Description | Test Conditions | Max | Unit |
|---|---|---|---|---|
| $C_{IN}$ | Input capacitance | $T_A$ = 25 °C, f = 1 MHz, $V_{CC}$ = 5.0 V | 8 | pF |
| $C_{OUT}$ | Output capacitance | | 8 | pF |

## Thermal Resistance

| Parameter [3] | Description | Test Conditions | 44-pin SOJ | 44-pin TSOP II | Unit |
|---|---|---|---|---|---|
| $\Theta_{JA}$ | Thermal resistance (junction to ambient) | Test conditions follow standard test methods and procedures for measuring thermal impedance, per EIA / JESD51. | 64.32 | 76.89 | °C/W |
| $\Theta_{JC}$ | Thermal resistance (junction to case) | | 31.03 | 14.28 | °C/W |

## AC Test Loads and Waveforms

**Figure 2. AC Test Loads and Waveforms**




**Note**
3. Tested initially and after any design or process changes that may affect these parameters.

## Switching Characteristics

Over the operating range

| Parameter [4] | Description | -15 | | Unit |
|---|---|---|---|---|
| | | Min | Max | |
| **Read Cycle** | | | | |
| $t_{RC}$ | Read cycle time | 15 | – | ns |
| $t_{AA}$ | Address to data valid | – | 15 | ns |
| $t_{OHA}$ | Data hold from address change | 3 | – | ns |
| $t_{ACE}$ | $\overline{CE}$ LOW to data valid | – | 15 | ns |
| $t_{DOE}$ | $\overline{OE}$ LOW to data valid | – | 7 | ns |
| $t_{LZOE}$ | $\overline{OE}$ LOW to low Z[4] | 0 | – | ns |
| $t_{HZOE}$ | $\overline{OE}$ HIGH to high Z[5, 6] | – | 7 | ns |
| $t_{LZCE}$ | $\overline{CE}$ LOW to low Z[5] | 3 | – | ns |
| $t_{HZCE}$ | $\overline{CE}$ HIGH to high Z[5, 6] | – | 7 | ns |
| $t_{PU}$ | $\overline{CE}$ LOW to power up | 0 | – | ns |
| $t_{PD}$ | $\overline{CE}$ HIGH to power down | – | 15 | ns |
| $t_{DBE}$ | Byte enable to data valid | – | 7 | ns |
| $t_{LZBE}$ | Byte enable to low Z[5] | 0 | – | ns |
| $t_{HZBE}$ | Byte disable to high Z[5, 6] | – | 7 | ns |
| **Write Cycle** [7, 8] | | | | |
| $t_{WC}$ | Write cycle time | 15 | – | ns |
| $t_{SCE}$ | $\overline{CE}$ LOW to write end | 10 | – | ns |
| $t_{AW}$ | Address setup to write end | 10 | – | ns |
| $t_{HA}$ | Address hold from write end | 0 | – | ns |
| $t_{SA}$ | Address setup to write start | 0 | – | ns |
| $t_{PWE}$ | $\overline{WE}$ pulse width | 12 | – | ns |
| $t_{SD}$ | Data setup to write end | 8 | – | ns |
| $t_{HD}$ | Data hold from write end | 0 | – | ns |
| $t_{LZWE}$ | $\overline{WE}$ HIGH to low Z[5] | 3 | – | ns |
| $t_{HZWE}$ | $\overline{WE}$ LOW to high Z[5, 6] | – | 7 | ns |
| $t_{BW}$ | Byte enable to write end | 9 | – | ns |

**Notes**

4. Test conditions assume signal transition time of 3 ns or less, timing reference levels of 1.5 V, input pulse levels of 0 to 3.0 V, and output loading of the specified $I_{OL}/I_{OH}$ and 30 pF load capacitance.
5. At any temperature and voltage condition, $t_{HZCE}$ is less than $t_{LZCE}$, $t_{HZOE}$ is less than $t_{LZOE}$, $t_{HZBE}$ is less than $t_{LZBE}$, and $t_{HZWE}$ is less than $t_{LZWE}$ for any device.
6. $t_{HZOE}$, $t_{HZBE}$, $t_{HZCE}$, and $t_{HZWE}$ are specified with a load capacitance of 5 pF as in part (b) of Figure 2 on page 6. Transition is measured ±500 mV from steady-state voltage.
7. The internal write time of the memory is defined by the overlap of $\overline{CE}$ LOW, $\overline{WE}$ LOW, and $\overline{BHE}$ / $\overline{BLE}$ LOW. $\overline{CE}$, $\overline{WE}$, and $\overline{BHE}$ / $\overline{BLE}$ must be LOW to initiate a write, and the transition of these signals can terminate the write. The input data setup and hold timing should be referenced to the leading edge of the signal that terminates the write.
8. The minimum write cycle pulse width for the Write Cycle No. 3 ($\overline{WE}$ Controlled, $\overline{OE}$ LOW) should be equal to sum of $t_{SD}$ and $t_{HZWE}$.

## Switching Waveforms

**Figure 3. Read Cycle No. 1** [9, 10]

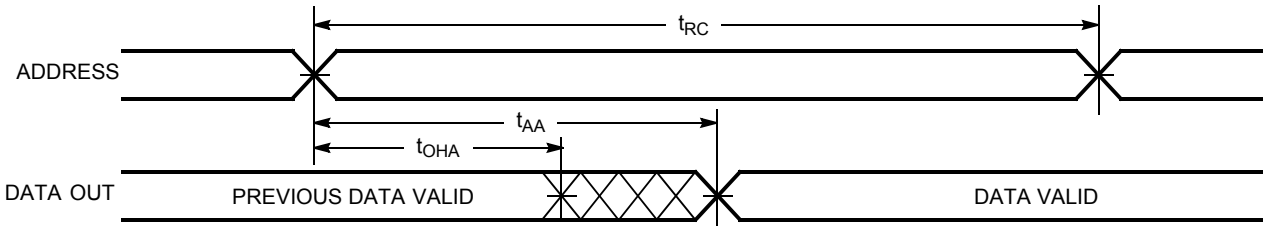
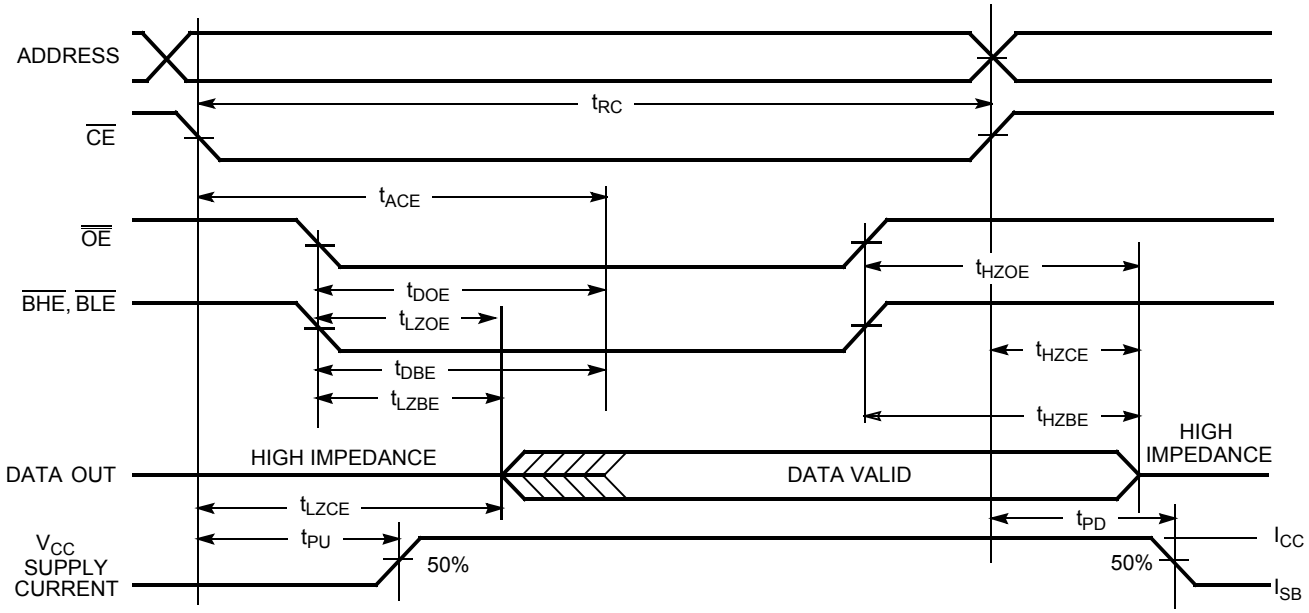



**Figure 4. Read Cycle No. 2 ($\overline{OE}$ Controlled)** [10, 11]




**Notes**
9. Device is continuously selected. $\overline{OE}$, $\overline{CE}$, $\overline{BHE}$, and $\overline{BHE}$ = $V_{IL}$.
10. $\overline{WE}$ is HIGH for read cycle.
11. Address valid prior to or coincident with $\overline{CE}$ transition LOW.

## Switching Waveforms (continued)

**Figure 5. Write Cycle No. 1 ($\overline{CE}$ Controlled) [12, 13]**

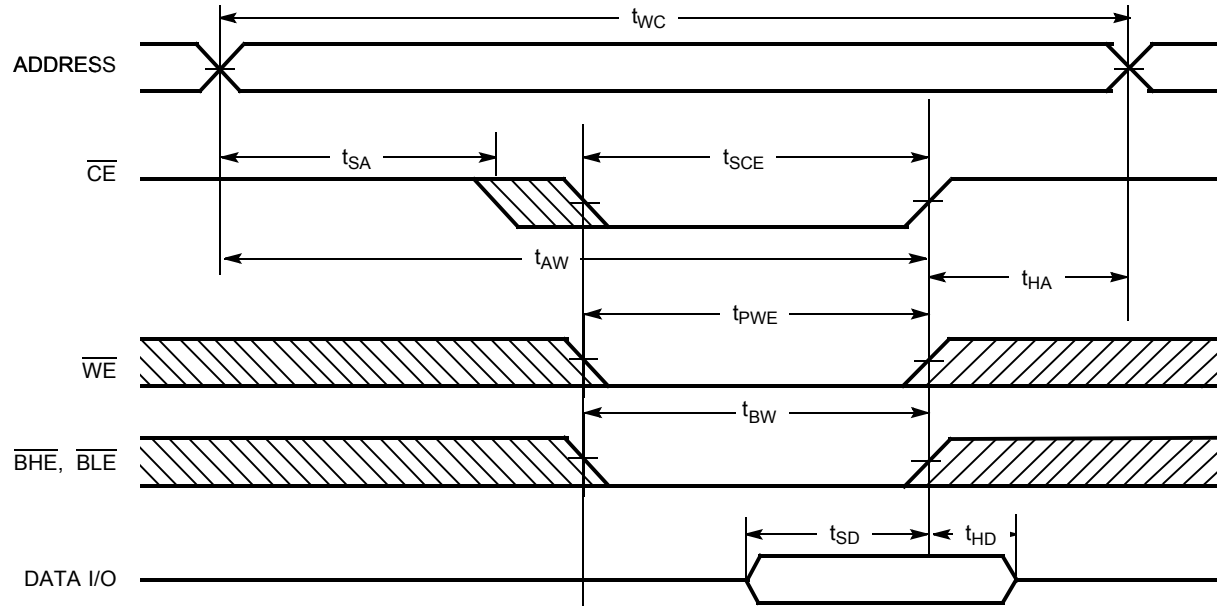
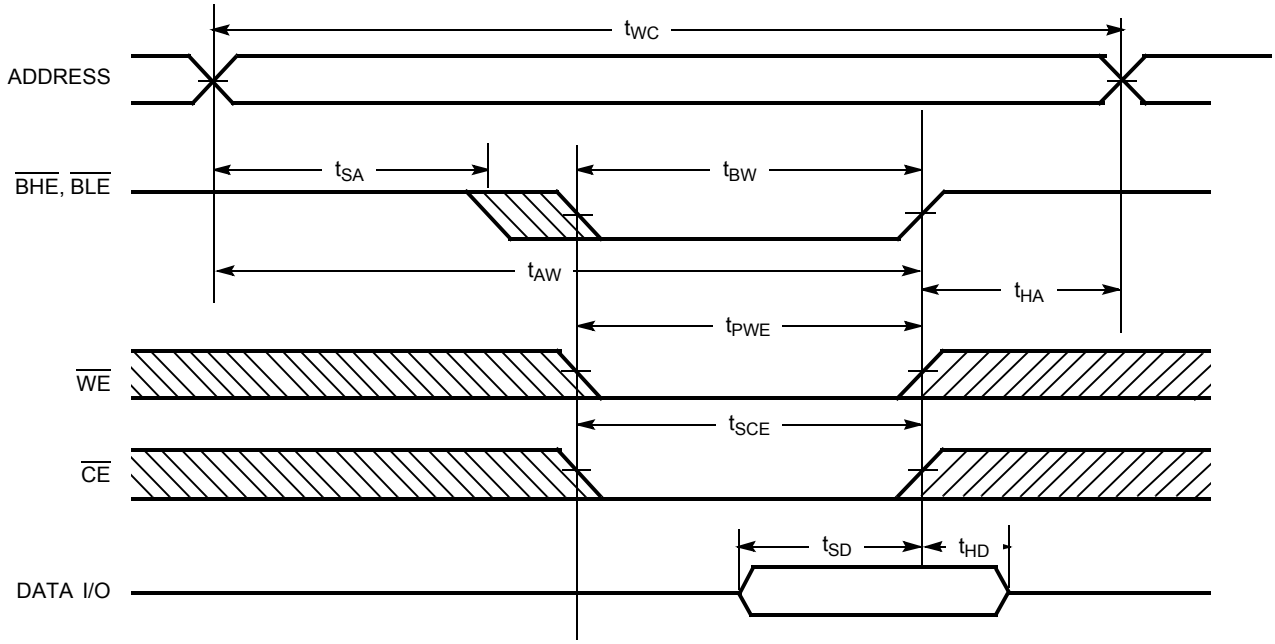


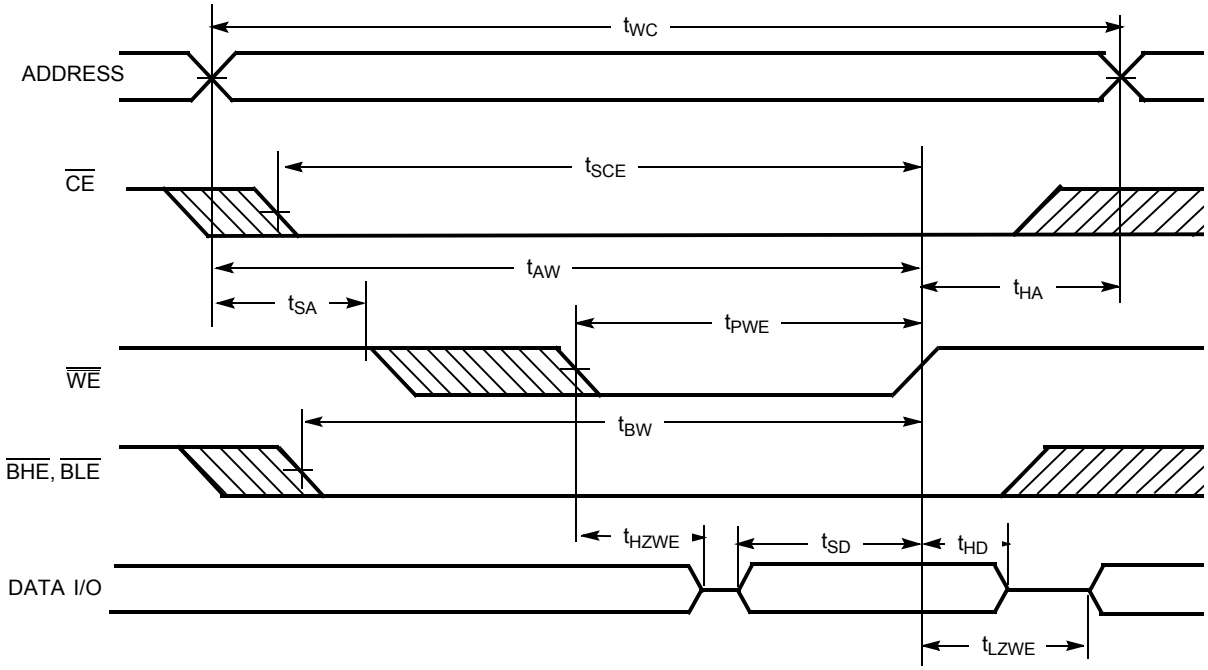

**Figure 6. Write Cycle No. 2 ($\overline{BLE}$ or $\overline{BHE}$ Controlled)**




**Notes**
12. Data I/O is high impedance if $\overline{OE}$ or $\overline{BHE}$ and/or $\overline{BLE}$= $V_{IH}$.
13. If $\overline{CE}$ goes HIGH simultaneously with $\overline{WE}$ going HIGH, the output remains in a high impedance state.

## Switching Waveforms (continued)

**Figure 7. Write Cycle No. 3 (WE Controlled, OE LOW)**



## Truth Table

| $\overline{CE}$ | $\overline{OE}$ | $\overline{WE}$ | $\overline{BLE}$ | $\overline{BHE}$ | $I/O_1–I/O_8$ | $I/O_9–I/O_{16}$ | Mode | Power |
|---|---|---|---|---|---|---|---|---|
| H | X | X | X | X | High Z | High Z | Power down | Standby ($I_{SB}$) |
| L | L | H | L | L | Data out | Data out | Read - All bits | Active ($I_{CC}$) |
| | | | L | H | Data out | High Z | Read - Lower bits only | Active ($I_{CC}$) |
| | | | H | L | High Z | Data out | Read - Upper bits only | Active ($I_{CC}$) |
| L | X | L | L | L | Data In | Data In | Write - All bits | Active ($I_{CC}$) |
| | | | L | H | Data In | High Z | Write - Lower bits only | Active ($I_{CC}$) |
| | | | H | L | High Z | Data In | Write - Upper bits only | Active ($I_{CC}$) |
| L | H | H | X | X | High Z | High Z | Selected, outputs disabled | Active ($I_{CC}$) |
| L | X | X | H | H | High Z | High Z | Selected, outputs disabled | Active ($I_{CC}$) |

## Ordering Information

Cypress offers other versions of this product type in many different configurations and features. The following table contains only the list of parts that are currently available. For a complete listing of all options, refer to the product summary page at http://www.cypress.com/products or contact your local sales representative.

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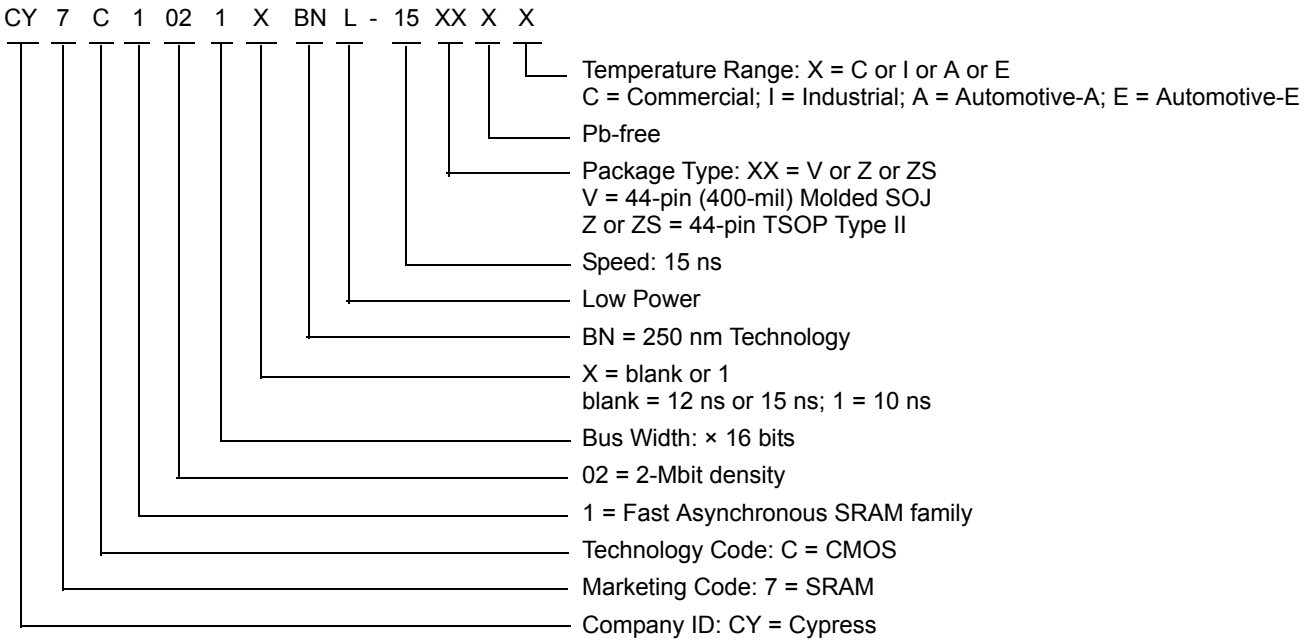
| Speed (ns) | Ordering Code | Package Diagram | Package Type | Operating Range |
|---|---|---|---|---|
| 15 | CY7C1021BNL-15VXC | 51-85082 | 44-pin (400-mil) Molded SOJ (Pb-free) | Commercial |
| | CY7C1021BNL-15ZXI | 51-85087 | 44-pin TSOP Type II (Pb-free) | Industrial |
| | CY7C1021BNL-15ZSXA | 51-85087 | 44-pin TSOP Type II (Pb-free) | Automotive-A |
| | CY7C1021BN-15ZSXE | | | Automotive-E |

### Ordering Code Definitions



## Package Diagrams

**Figure 8. 44-pin SOJ (400 Mils) V44.4 Package Outline, 51-85082**

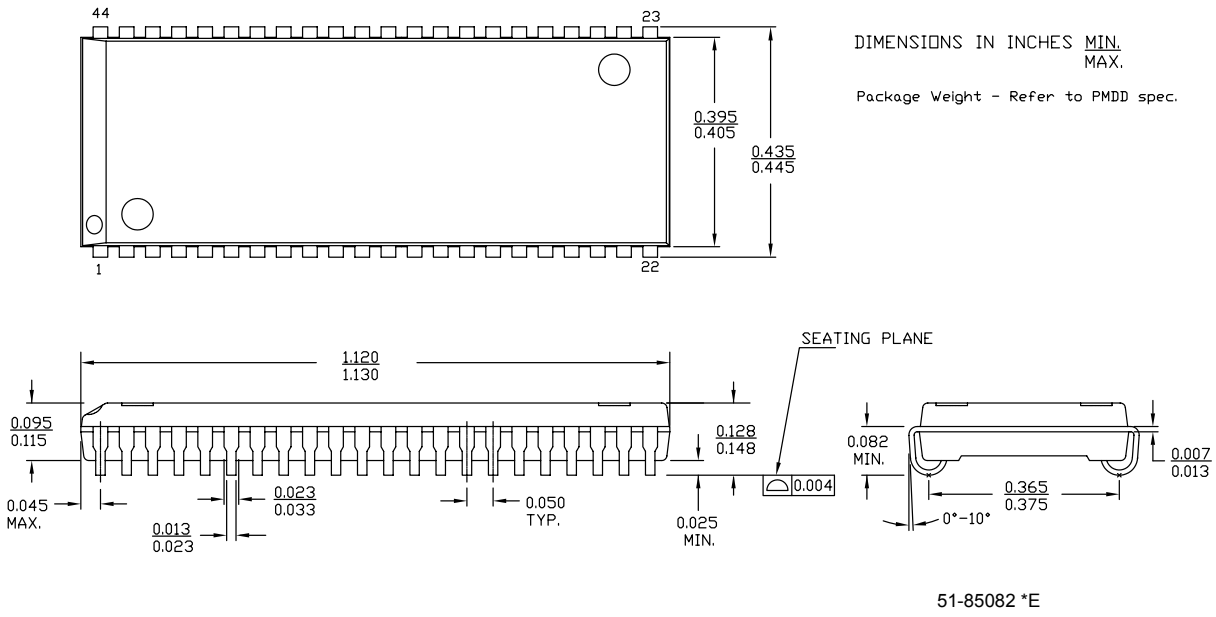
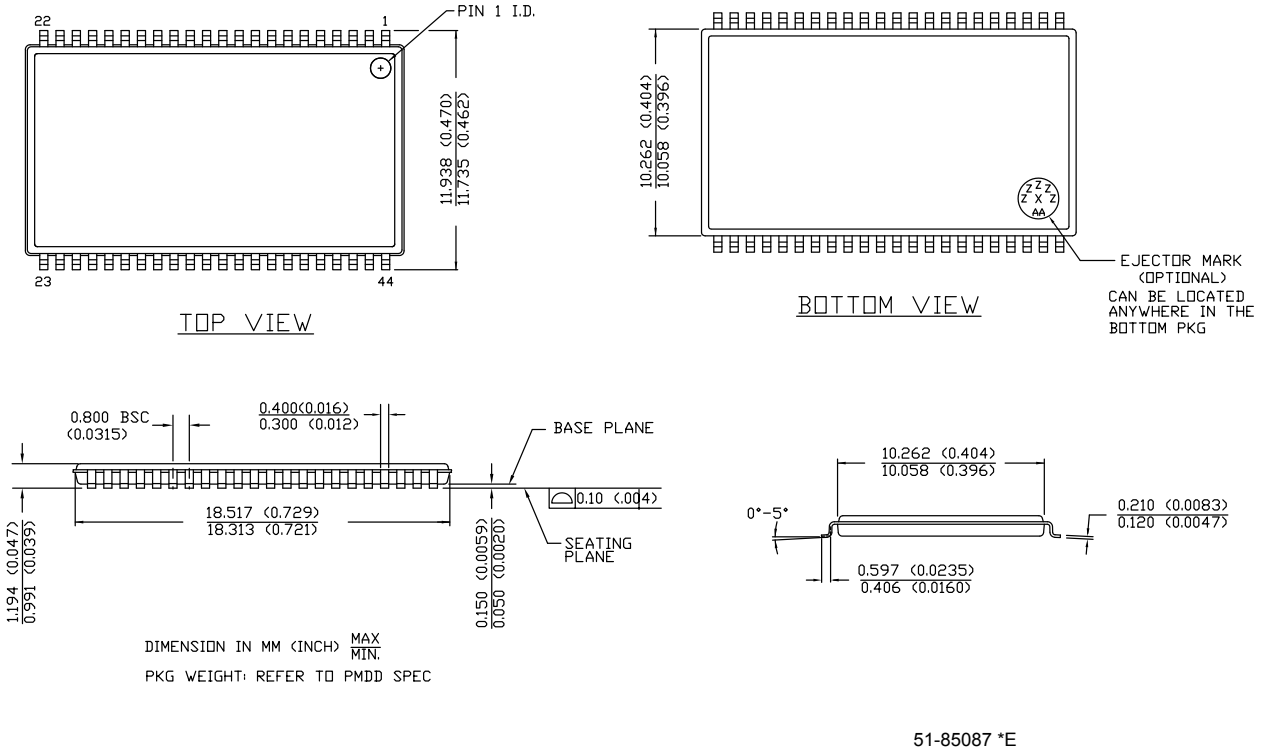



**Figure 9. 44-pin TSOP Z44-II Package Outline, 51-85087**



## Acronyms

| Acronym | Description |
|---|---|
| $\overline{BHE}$ | Byte High Enable |
| $\overline{BLE}$ | Byte Low Enable |
| $\overline{CE}$ | Chip Enable |
| CMOS | Complementary Metal Oxide Semiconductor |
| I/O | Input/Output |
| $\overline{OE}$ | Output Enable |
| SOJ | Small Outline J-lead |
| SRAM | Static Random Access Memory |
| TSOP | Thin Small Outline Package |
| TTL | Transistor-Transistor Logic |
| $\overline{WE}$ | Write Enable |

## Document Conventions

### Units of Measure

| Symbol | Unit of Measure |
|---|---|
| °C | degree Celsius |
| MHz | megahertz |
| µA | microampere |
| mA | milliampere |
| mm | millimeter |
| mW | milliwatt |
| ns | nanosecond |
| Ω | ohm |
| % | percent |
| pF | picofarad |
| V | volt |
| W | watt |

## Document History Page

| Document Title: CY7C1021BN, 1-Mbit (64 K × 16) Static RAM<br>Document Number: 001-06494 | | | | |
|---|---|---|---|---|
| **Rev.** | **ECN No.** | **Submission Date** | **Orig. of Change** | **Description of Change** |
| ** | 423877 | See ECN | NXR | New data sheet. |
| *A | 505726 | See ECN | NXR | Removed $I_{OS}$ parameter from DC Electrical Characteristics table.<br>Updated Ordering Information (Added Automotive products). |
| *B | 2897061 | 03/22/10 | AJU | Updated Ordering Information (Removed obsolete parts).<br>Updated Package Diagrams. |
| *C | 2947254 | 06/08/10 | RAME | Updated Pin Definitions (Replaced "Byte write select inputs" with "Byte Enable select inputs" in description of pin $\overline{BHE}$, $\overline{BLE}$).<br>Updated AC Test Loads and Waveforms (Updated Figure 2 (Added ohm (Ω) symbol in Thevenin equivalent circuit)).<br>Updated Switching Characteristics (Updated Note 5 (Included $t_{HZBE}$ and $t_{LZBE}$ in the note)).<br>Updated Ordering Information (Included operating range for CY7C1021BNL-15ZXI in ordering information table). |
| *D | 3328634 | 26/07/2011 | AJU | Updated Features (Removed the information associated with speed bins -10 and -12).<br>Removed the note "For best practice recommendations, refer to the Cypress application note, SRAM System Design Guidelines-AN1064." in page 1 and its reference in Functional Description.<br>Updated Functional Description (Removed the information associated with speed bins -10 and -12).<br>Updated Selection Guide (Removed the information associated with speed bins -10 and -12).<br>Updated Electrical Characteristics (Removed the information associated with speed bins -10 and -12).<br>Updated Switching Characteristics (Removed the information associated with speed bins -10 and -12).<br>Updated Ordering Information.<br>Added Acronyms and Units of Measure.<br>Updated to new template. |
| *E | 4125119 | 09/16/2013 | VINI | Updated Package Diagrams:<br>spec 51-85082 – Changed revision from *C to *E.<br>spec 51-85087 – Changed revision from *C to *E.<br>Updated to new template.<br>Completing Sunset Review. |
| *F | 4545523 | 10/20/2014 | VINI | Updated Document Title to read as "CY7C1021BN, 1-Mbit (64 K × 16) Static RAM".<br>Removed CY7C10211BN related information in all instances across the document.<br>Updated Switching Characteristics:<br>Removed "CY7C1021B" and retained "-15" in column heading "CY7C1021B-15".<br>Added Note 8 and referred the same note in "Write Cycle".<br>Added $t_{PWE}$ parameter and its details.<br>Completing Sunset Review. |
| *G | 4557296 | 10/31/2014 | VINI | Updated Switching Characteristics:<br>Updated minimum and maximum values of $t_{PWE}$ parameter. |
| *H | 4578500 | 12/16/2014 | VINI | Updated Ordering Information:<br>Removed the prune part number CY7C1021BN-15VXE. |
| *I | 4984333 | 10/23/2015 | NILE | Updated to new template.<br>Completing Sunset Review. |

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