CS1610A/11A
CS1612A/13A

TRIAC Dimmable LED Driver IC

Features

- Best-in-class Dimmer Compatibility
  - Leading-edge (TRIAC) Dimmers
  - Trailing-edge Dimmers
  - Center-cut Dimmers
  - Digital Dimmers (with Integrated Power Supply)
- Up to 90% Efficiency
- Optimized for ≤25W Input Power
- Flicker-free Dimming
- 0% Minimum Dimming Level
- Quasi-resonant Second Stage with Constant-current Output
  - Flyback and Buck
- Fast Startup
- Tight LED Current Regulation: Better than ±5%
- Primary-side Regulation (PSR)
- >0.9 Power Factor
- IEC-61000-3-2 Compliant
- NEMA SSL6 Compatible
- Soft Start
- Protections:
  - Output Open/Short
  - Current-sense Resistor Open/Short
  - External Overtemperature Using NTC

Overview

The CS1610A/1A/12A/13A is a digital control IC engineered to deliver a high-efficiency, cost-effective, flicker-free, phase-dimmable, solid-state lighting (SSL) solution for the incandescent lamp-replacement market. The CS1610A/11A is designed to control a quasi-resonant flyback topology. The CS1612A/13A is designed to control a buck topology. The CS1610A/12A and CS1611A/13A are designed for 120VAC and 230VAC line voltage applications, respectively.

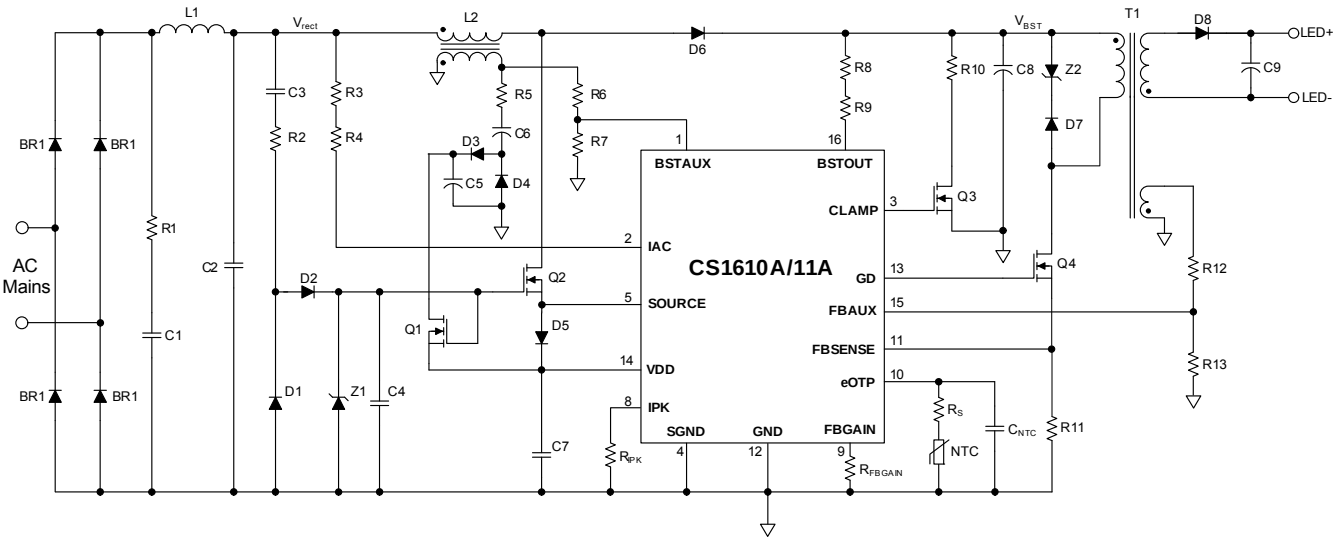
The CS1610A/11A/12A/13A integrates a critical conduction mode (CRM) boost converter that provides power factor correction and dimmer compatibility with a constant output current, quasi-resonant second stage. An adaptive dimmer compatibility algorithm controls the boost stage and dimmer compatibility operation mode to enable flicker-free operation to <2% output current with leading-edge, trailing-edge, center-cut, and digital dimmers (dimmers with an integrated power supply).

Applications

- Dimmable Retrofit LED Lamps
- Dimmable LED Luminaries
- Offline LED Drivers
- Commercial Lighting

Ordering Information

See **page 16.**



Preliminary Product Information

This document contains information for a product under development. Cirrus Logic reserves the right to modify this product without notice.

Cirrus Logic, Inc.
http://www.cirrus.com

1. INTRODUCTION

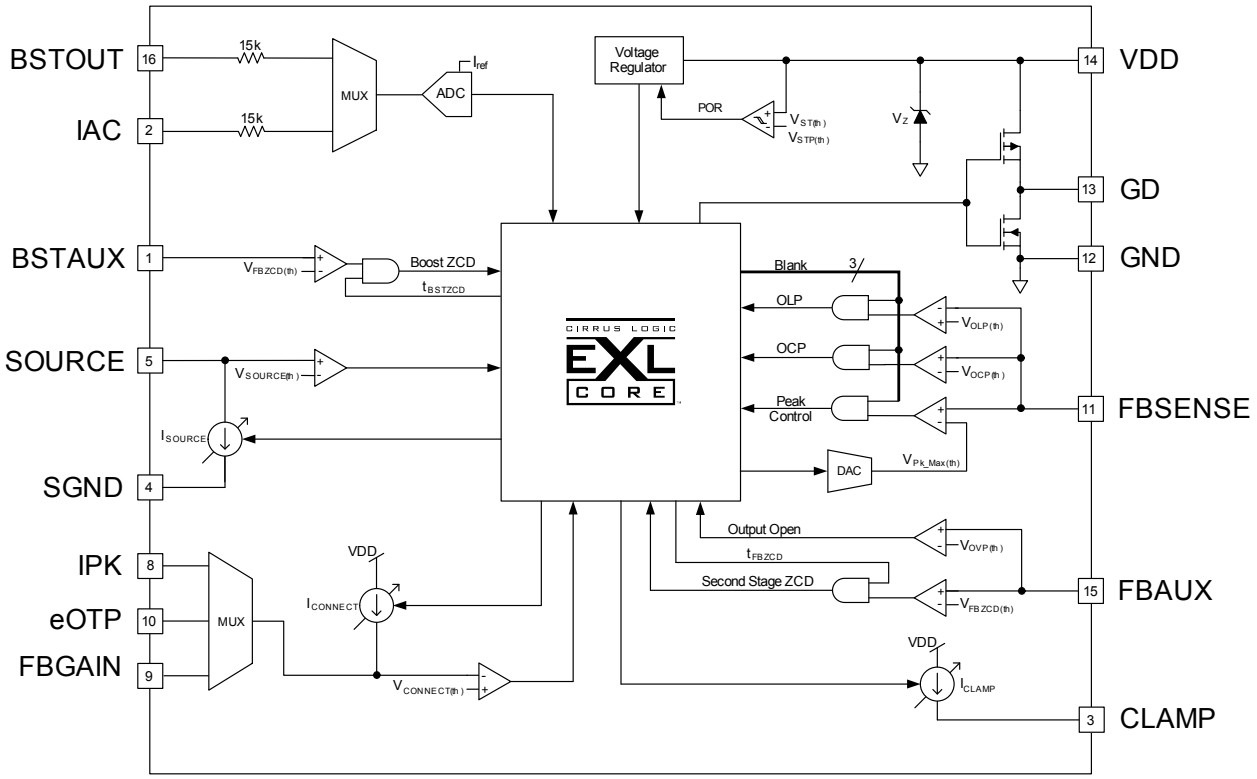


Figure 1. CS1610A/11A/12A/13A Block Diagram

A typical schematic using the CS1610A/11A for flyback applications is shown on the previous page.

Startup current is provided from a patent-pending, external, high-voltage source-follower network. In addition to providing startup current, this unique topology is integral in providing compatibility with digital dimmers by ensuring V_{DD} power is always available to the IC. During steady-state operation, an auxiliary winding on the boost inductor back-biases the source-follower circuit and provides steady-state operating current to the IC to improve system efficiency.

The rectified input voltage is sensed as a current into pin IAC and is used to control the adaptive dimmer compatibility algorithm and extract the phase of the input voltage for output dimming control. During steady-state operation, the external high-voltage, source-follower circuit is source-switched in critical conduction mode (CRM) to boost the input voltage. This allows the boost stage to maintain good power factor, provides dimmer compatibility, reduces bulk capacitor ripple current, and provides a regulated input voltage to the second stage.

The output voltage of the CRM boost is sensed by the current into the boost output voltage sense pin BSTOUT. The quasi-resonant second stage is implemented with peak-current mode primary-side control, which eliminates the need for additional components to provide feedback from the secondary and reduces system cost and complexity.

Voltage across an external user-selected resistor is sensed through pin FBSENSE to control the peak current through the second stage inductor. Leading-edge and trailing-edge blanking on pin FBSENSE prevents false triggering.

Pin FBAUX is used to sense the second stage inductor demagnetization to ensure quasi-resonant switching of the output stage.

When an external negative temperature coefficient (NTC) thermistor is connected to the eOTP pin, the CS1610A/11A/12A/13A monitors the system temperature, allowing the controller to reduce the output current of the system. If the temperature reaches a designated high set point, the IC is shutdown and stops switching.

2. PIN DESCRIPTION

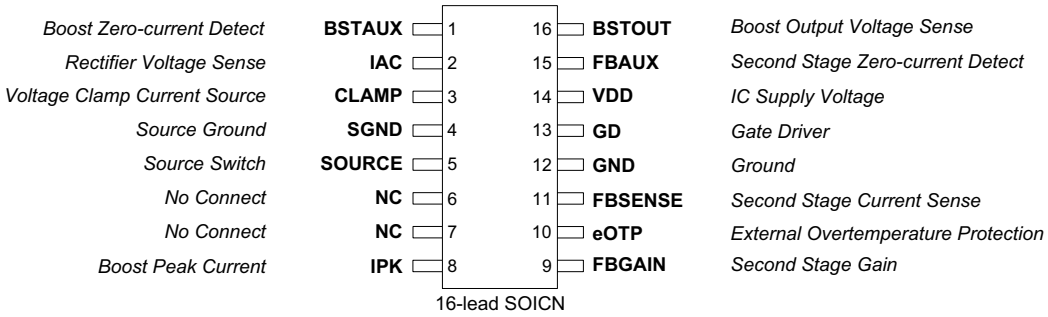


Figure 2. CS1610A/11A/12A/13A Pin Assignments

Pin Name	Pin #	I/O	Description
BSTAUX	1	IN	**Boost Zero-current Detect** — Boost Inductor demagnetization sensing input for zero-current detection (ZCD) information. The pin is connected to the PFC boost inductor auxiliary winding through an external resistor divider.
IAC	2	IN	**Rectifier Voltage Sense** — A current proportional to the rectified line voltage is fed into this pin. The current is measured with an A/D converter.
CLAMP	3	OUT	**Voltage Clamp Current Source** — Connect to a voltage clamp circuit on the output of the boost stage.
SGND	4	PWR	**Source Ground** — Common reference current return for the SOURCE pin.
SOURCE	5	IN	**Source Switch** — Connected to the source of the boost stage external high-voltage FET.
NC	6	IN	**No Connect** — Connect this pin to VDD using a pull-up resistor.
NC	7	IN	**No Connect** — Connect this pin to VDD using a pull-up resistor.
IPK	8	IN	**Boost Peak Current** — Connect a resistor to this pin to set the peak current of the boost circuit.
FBGAIN	9	IN	**Second Stage Gain** — Connect a resistor to this pin to set the switching frequency gain for the second stage.
eOTP	10	IN	**External Overtemperature Protection** — Connect an external NTC thermistor to this pin, allowing the internal A/D converter to sample the change to NTC resistance.
FBSENSE	11	IN	**Second Stage Current Sense** — The current flowing in the second stage FET is sensed across a resistor. The resulting voltage is applied to this pin and digitized for use by the second stage computational logic to determine the FET's duty cycle.
GND	12	PWR	**Ground** — Common reference. Current return for both the input signal portion of the IC and the gate driver.
GD	13	OUT	**Gate Driver** — Gate drive for the second stage power FET.
VDD	14	PWR	**IC Supply Voltage** — Connect a storage capacitor to this pin to serve as a reservoir for operating current for the device, including the gate drive current to the power transistor.
FBAUX	15	IN	**Second Stage Zero-current Detect** — Second stage inductor sensing input. The pin is connected to the second stage inductor's auxiliary winding through an external resistor divider.
BSTOUT	16	IN	**Boost Output Voltage Sense** — A current proportional to the boost output is fed into this pin. The current is measured with an A/D converter.

3. CHARACTERISTICS AND SPECIFICATIONS

3.1 Electrical Characteristics

Typical characteristics conditions:
- T_A = 25 °C, V_{DD} = 12 V, GND = 0 V
- All voltages are measured with respect to GND.
- Unless otherwise specified, all currents are positive when flowing into the IC.

Minimum/Maximum characteristics conditions:
- T_J = -40 °C to +125 °C, V_{DD} = 11 V to 17 V, GND = 0 V

Parameter	Condition	Symbol	Min	Typ	Max	Unit
VDD Supply Voltage						
Operating Range	After Turn-on	V_{DD}	11	-	17	V
Turn-on Threshold Voltage	V_{DD} Increasing	$V_{ST(th)}$	-	9.0	-	V
Turn-off Threshold Voltage (UVLO)	V_{DD} Decreasing	$V_{STP(th)}$	-	7.7	-	V
Zener Voltage (Note 1)	I_{DD} = 20 mA	V_Z	18.5	-	19.8	V
VDD Supply Current						
Startup Supply Current	$V_{DD} < V_{ST(th)}$	I_{ST}	-	-	350	µA
Operating Supply Current (Note 2)	C_L = 0.25 nF, $F_{sw} \leq$ 70 kHz		-	4.0	-	mA
Reference						
Reference Current CS1610A/12A CS1611A/13A	 V_{BST} = 200 V V_{BST} = 400 V	I_{ref}	 - -	 133 133	 - -	 µA µA
Boost						
Maximum Switching Frequency		$f_{BST(Max)}$	-	-	200	kHz
Clamp Current		I_{CLAMP}	-	-3.7	-	mA
Dimmer Attach Peak Current CS1610A/12A CS1611A/13A	 $108 \leq V_{line} \leq 132$ $207 \leq V_{line} \leq 253$		 - -	 590 508	 - -	 mA mA
DCM Delay in No-dimmer Mode CS1610A CS1611A/12A/13A			 - -	 0.0 6.4	 - -	 µs µs
Boost Zero-Current Detect						
BSTZCD Threshold		$V_{BSTZCD(th)}$	-	200	-	mV
BSTZCD Blanking		t_{BSTZCD}	-	3.5	-	µs
ZCD Sink Current (Note 3)		I_{ZCD}	-2	-	-	mA
BSTAUX Upper Voltage	I_{ZCD} = 1 mA		-	V_{DD}+0.6	-	V
Boost Protection						
Boost Overvoltage Protection (BOP) CS1610A/12A CS1611A/13A	 $108 \leq V_{line} \leq 132$ $207 \leq V_{line} \leq 253$	$V_{BOP(th)}$	 - -	 162 148	 - -	 µA µA
Clamp Turn On CS1610A/12A CS1611A/13A	 $108 \leq V_{line} \leq 132$ $207 \leq V_{line} \leq 253$		 - -	 147 142	 - -	 µA µA
Second Stage Current Sense						
Sense Resistor Short Threshold		$V_{OLP(th)}$	-	200	-	mV
Peak Control Threshold		$V_{Pk\_Max(th)}$	-	1.4	-	V
Leading-edge Blanking		t_{LEB}	-	550	-	ns
Delay to Output			-	-	100	ns

Parameter	Condition	Symbol	Min	Typ	Max	Unit
Second Stage Zero-current Detect						
FBZCD Threshold		$V_{FBZCD(th)}$	-	200	-	mV
FBZCD Blanking CS1610A/12A CS1611A/13A		t_{FBZCB}	 - -	 2 2.8	 - -	 µs µs
ZCD Sink Current (Note 3)		I_{ZCD}	-2	-	-	mA
FBAUX Upper Voltage	I_{ZCD} = 1mA		-	V_{DD}+0.6	-	V
Second Stage Pulse Width Modulator						
Minimum On Time			-	0.55	-	µs
Maximum On Time CS1610A/11A/13A CS1612A			 - -	 8.8 12.0	 - -	 µs µs
Minimum Switching Frequency		$t_{FB(Min)}$	-	625	-	Hz
Maximum Switching Frequency (Note 4)		$t_{FB(Max)}$	-	200	-	kHz
Second Stage Gate Driver						
Output Source Resistance		Z_{OUT}	-	20.3	-	Ω
Output Sink Resistance		Z_{OUT}	-	9.4	-	Ω
Rise Time	C_L = 0.25nF		-	-	30	ns
Fall Time	C_L = 0.25nF		-	-	20	ns
Second Stage Protection						
Overcurrent Protection (OCP)		$V_{OCP(th)}$	-	1.69	-	V
Overvoltage Protection (OVP)		$V_{OVP(th)}$	-	1.25	-	V
Open Loop Protection (OLP)		$V_{OLP(th)}$	-	200	-	mV
External Overtemperature Protection (eOTP), Boost Peak Current, Second Stage Frequency Gain						
Pull-up Current Source – Maximum		$I_{CONNECT}$	-	80	-	µA
Conductance Accuracy (Note 5)			-	-	±5	%
Conductance Offset (Note 5)			-	±250	-	nS
Current Source Voltage Threshold		$V_{CONNECT(th)}$	-	1.25	-	V
Internal Overtemperature Protection (iOTP)						
Thermal Shutdown Threshold (Note 6)		T_{SD}	-	143	-	ºC
Thermal Shutdown Hysteresis (Note 6)		$T_{SD(Hy)}$	-	12	-	ºC

Notes:
1. The CS1610A/11A/12A/13A has an internal shunt regulator that limits the voltage on the VDD pin. V_Z, the shunt regulation voltage, is defined in the *VDD Supply Voltage* section on *page 4*.
2. For test purposes, load capacitance C_L is connected to pin GD and is equal to 0.25nF.
3. External circuitry should be designed to ensure that the ZCD current drawn from the internal clamp diode when it is forward biased does not exceed specification.
4. Switching period (T1+T2) ≥ 5 µs. Period T1 and T2 are defined in the *Control Parameters* section on *page 12*.
5. The conductance is specified in Siemens (S or 1/Ω). Each LSB of the internal ADC corresponds to 250nS or one parallel 4MΩ resistor. Full scale corresponds to 256 parallel 4MΩ resistors or 15.625kΩ.
6. Specifications are guaranteed by design and are characterized and correlated using statistical process methods.

3.2 Thermal Resistance

Symbol	Parameter		Value	Unit
θ_{JA}	Junction-to-Ambient Thermal Impedance	2 Layer PCB 4 Layer PCB	135 129	°C/W °C/W
θ_{JC}	Junction-to-Case Thermal Impedance	2 Layer PCB 4 Layer PCB	50 43	°C/W °C/W

3.3 Absolute Maximum Ratings

Characteristics conditions:

All voltages are measured with respect to GND.

Pin	Symbol	Parameter		Value	Unit
14	V_{DD}	IC Supply Voltage		18.5	V
1, 2, 5, 8, 9, 10,11,15,16		Analog Input Maximum Voltage		-0.5 to (V_{DD}+0.5)	V
1, 2, 8, 9, 10, 11, 15, 16		Analog Input Maximum Current		5	mA
13	V_{GD}	Gate Drive Output Voltage		-0.3 to (V_{DD}+0.3)	V
13	I_{GD}	Gate Drive Output Current		-1.0 / +0.5	A
5	I_{SOURCE}	Current into Pin		1.1	A
3	I_{CLAMP}	Clamp Output Current		5	mA
-	P_D	Total Power Dissipation		400	mW
-	T_J	Junction Temperature Operating Range	(Note 7)	-40 to +125	°C
-	T_{Stg}	Storage Temperature Range		-65 to +150	°C
All Pins	ESD	Electrostatic Discharge Capability	Human Body Model Charged Device Model	2000 500	V V

Note: 7. Long-term operation at the maximum junction temperature will result in reduced product life. Derate internal power dissipation at the rate of 50 mW / °C for variation over temperature.

WARNING:

Operation at or beyond these limits may result in permanent damage to the device.
Normal operation is not guaranteed at these extremes.

4. TYPICAL PERFORMANCE PLOTS

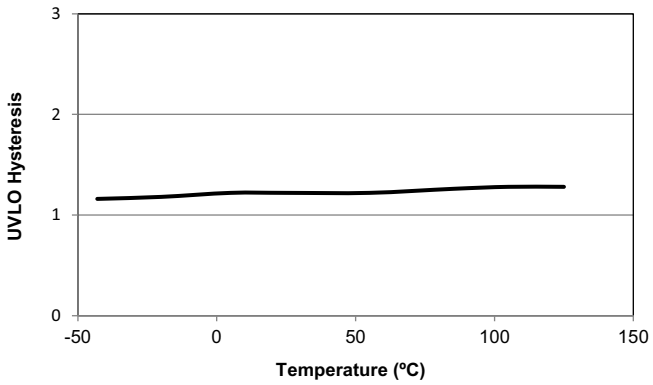


Figure 3. UVLO Characteristics

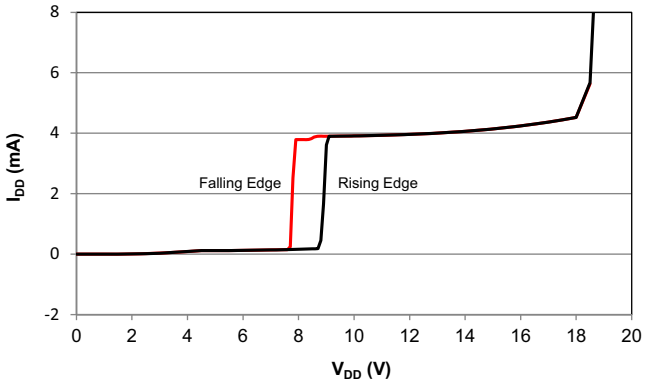


Figure 4. Supply Current vs. Voltage

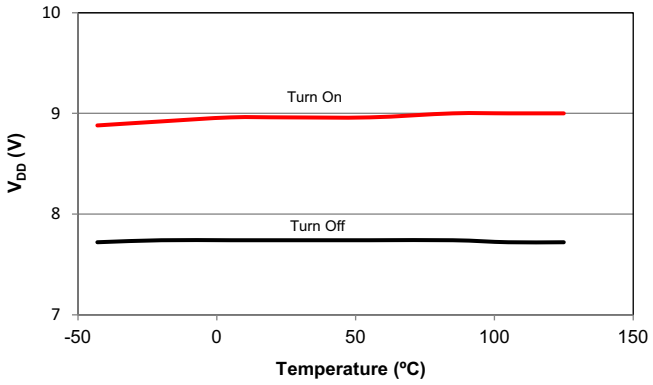


Figure 5. Turn On/Off Threshold Voltage vs. Temperature

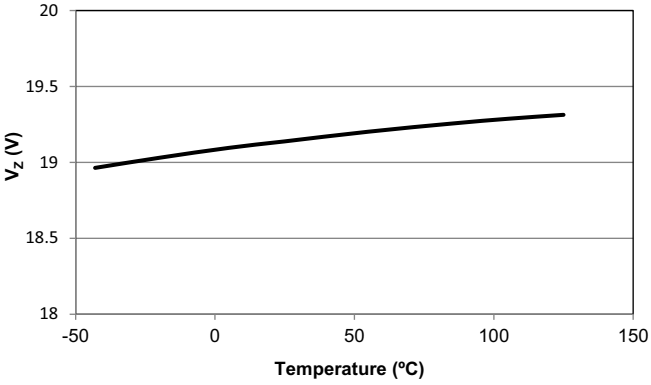


Figure 6. Zener Voltage vs. Temperature

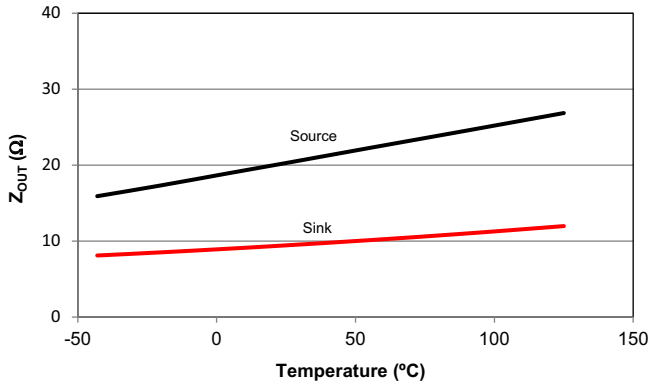


Figure 7. Gate Drive Resistance vs. Temperature

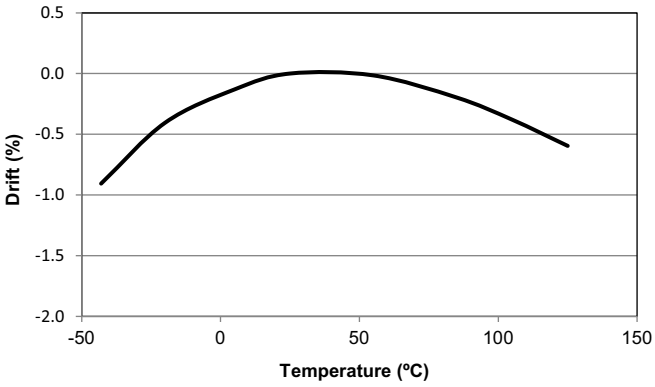


Figure 8. Reference Current I_{ref} Drift vs. Temperature

5. GENERAL DESCRIPTION

5.1 Overview

The CS1610A/11A/12A/13A is a digital control IC engineered to deliver a high-efficiency, cost-effective, flicker-free, phase-dimmable, solid-state lighting (SSL) solution for the incandescent lamp-replacement market. The CS1610A/11A/12A/13A has best-in-class dimmer compatibility and mixed-load compatibility because it is enhanced with a center-cut algorithm and a mixed-load compatibility algorithm. The CS1610A/11A is designed to control a quasi-resonant flyback topology. The CS1612A/13A is designed to control a buck topology. The CS1610A/12A and CS1611A/13A are designed for 120VAC and 230VAC line voltage applications, respectively.

The CS1610A/11A/12A/13A integrates a critical conduction mode (CRM) boost converter that provides power factor correction and dimmer compatibility with a constant output current, quasi-resonant second stage. An adaptive dimmer compatibility algorithm controls the boost stage and dimmer compatibility operation mode to enable flicker-free operation to <2% output current with leading-edge, trailing-edge, and digital dimmers (dimmers with an integrated power supply).

5.2 Startup Circuit

An external, high-voltage source-follower circuit is used to deliver startup current to the IC. During steady-state operation, an auxiliary winding on the boost inductor biases this circuit to an off state to improve system efficiency, and all IC supply current is generated from the auxiliary winding. The patent-pending technology of the external, high-voltage source-follower circuit enables system compatibility with digital dimmers (dimmers containing an internal power supply) by providing a continuous path for the dimmer's power supply to recharge during its off state. During steady-state operation, high-voltage FET Q2 is source-switched by a variable internal current source on the SOURCE pin to create the boost circuit. A Schottky diode with a forward voltage less than 0.6V is recommended for diode D5. Schottky diode D5 will limit inrush current through the internal diode, preventing damage to the IC.

5.3 Dimmer Switch Detection

The CS1610A/11A/12A/13A dimmer switch detection algorithm determines if the SSL system is controlled by a regular switch, a leading-edge dimmer, or a trailing-edge dimmer. Dimmer switch detection is implemented using two modes: Dimmer Learn Mode and Dimmer Validate Mode. These assist in limiting the system power losses. Once the IC reaches UVLO start threshold $V_{ST(th)}$ and begins operating, the CS1610A/11A/12A/13A is in Dimmer Learn Mode, allowing the dimmer switch detection circuit to set the operating state of the IC to one of three modes: No-dimmer Mode, Leading-edge Mode, or Trailing-edge Mode.

5.3.1 Dimmer Learn Mode

In Dimmer Learn Mode, the dimmer detection circuit spends approximately two line-cycles learning whether there is a dimmer switch and, if present, whether it is a trailing-edge or leading-edge dimmer. In Dimmer Learn Mode, a modified version of the leading-edge algorithm is used. The trailing-side slope of the input line voltage is sensed to decide whether the dimmer switch is a trailing-edge dimmer. The dimmer detection circuit transitions to Dimmer Validate Mode once the circuit detects a dimmer is present.

5.3.2 Dimmer Validate Mode

During normal operation, the CS1610A/11A/12A/13A is in Dimmer Validate Mode. This instructs the dimmer detection circuit to periodically validate that the IC is executing the correct algorithm for the attached dimmer. The dimmer detection algorithm periodically verifies the IC operating state as a protection against incorrect detection. As additional protection, the output of the dimmer detection algorithm is low-pass filtered to prevent noise or transient events from changing the IC's operating mode. The IC will return to Dimmer Learn Mode when it has determined that the wrong algorithm is being executed.

5.3.3 No-dimmer Mode

Upon detection that the line is not phase cut with a dimmer, the CS1610A/11A/12A/13A operates in No-dimmer Mode, where it provides a power factor that is in excess of 0.9. The CS1610A/11A/12A/13A accomplishes this by boosting in CRM and DCM mode. The CS1610A boosts in CRM mode only. The peak current is modulated to provide link regulation. The CS1610A/11A/12A/13A alternates between two settings of peak current. To regulate the boost output voltage, the device uses a peak current set by resistor R_{IPK}. The time that this current is used is determined by an internal compensation loop to regulate the boost output voltage. The internal algorithm will reduce the peak current of the boost stage to maintain output voltage regulation and obtain the desired power factor.

5.3.4 Leading-edge Mode

In Leading-edge Mode, the CS1610A/11A/12A/13A regulates boost output voltage V_{BST} while maintaining the dimmer phase angle (see Figure 9). The device executes a CCM boost algorithm using dimmer attach current as the initial peak current on the initial firing event of the dimmer. After gaining control of the incoming current, the device transitions to a CRM boost algorithm to regulate the boost output voltage. The device periodically executes a probe event on the incoming waveform. The information from the probe event is beneficial to maintaining proper operation with the dimmer circuitry.

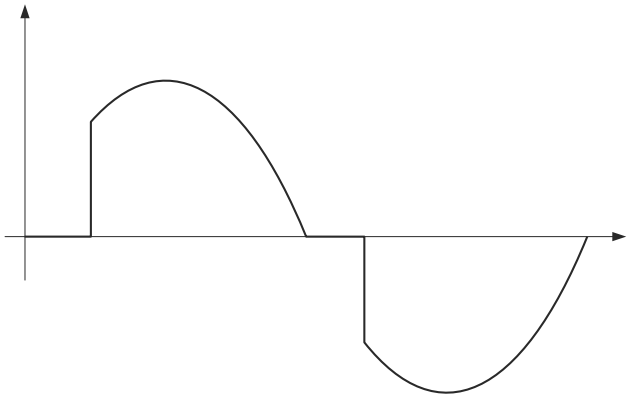


Figure 9. Leading-edge Mode Phase Cut Waveform

5.3.5 Trailing-edge Mode

In Trailing-edge Mode, the CS1610A/11A/12A/13A determines its operation based on the falling edge of the input voltage waveform (see Figure 10). To allow the dimmer to operate properly, the CS1610A/11A/12A/13A must charge the capacitor in the dimmer on the falling edge of the input voltage. To accomplish this, the CS1610A/11A/12A/13A always executes the boost algorithm on this falling edge. To ensure maximum compatibility with dimmer components, the device boosts during this falling edge event using a peak current that must meet a minimum value. In Trailing-edge Mode, only CRM boosting is used.

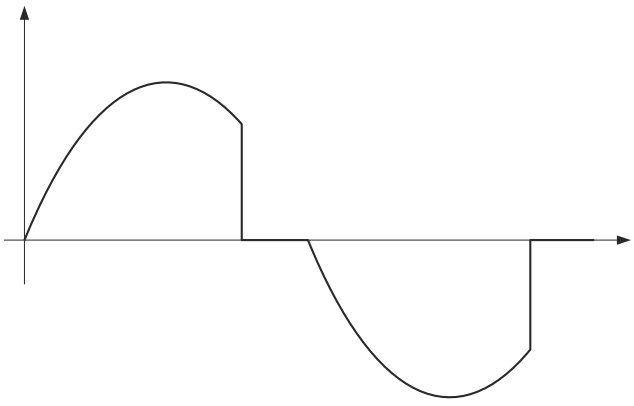


Figure 10. Trailing-edge Mode Phase Cut Waveform

5.3.6 Center-cut Mode

In Center-cut Mode, the CS1610A/11A/12A/13A determines its operation based on the leading-edge, zero-crossing and falling edge of the input voltage waveform (see Figure 11). To provide proper dimmer operation, the device implements the same techniques used in the Leading-edge Mode. The boost algorithm uses the dimmer attach current as the initial peak current for the initial firing event of the dimmer. Additionally, the CS1610A/11A/12A/13A provides a low impedance path during the zero-crossing event of the input waveform and uses trailing-edge mode techniques to charge the dimmer capacitor on the falling edge of the input waveform.

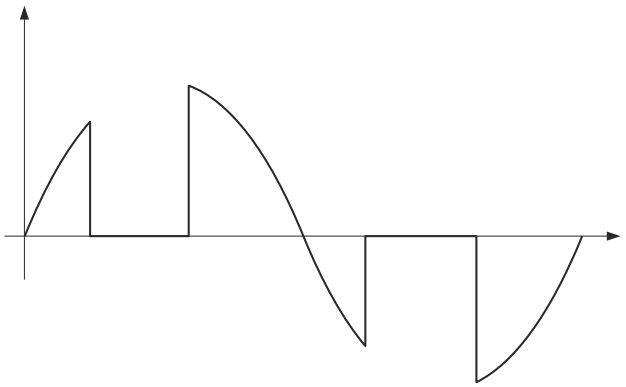


Figure 11. Center-cut Mode Phase Cut Waveform

5.4 Boost Stage

The high-voltage FET in the source-follower startup circuit is source-switched by a variable current source on the SOURCE pin to operate a boost circuit. Peak FET switching current is set with an external resistor on pin IPK.

In No-dimmer Mode, the boost stage begins operating when the start threshold is reached during each rectified half line-cycle and is disabled at the nominal boost output voltage. The peak FET switching current determines the percentage of the rectified input voltage conduction angle over which the boost stage will operate. The control algorithm adjusts the peak FET switching current to maximize the operating time of the boost stage, thus improving the input power factor.

When operating in Leading-edge Mode, the boost stage ensures the hold current requirement of the dimmer is met from the initiation of each half-line dimmer conduction cycle until the peak of the rectified input voltage. The Trailing-edge Mode boost stage ensures that the trailing-edge is exposed at the correct time with the correct current.

5.4.1 Maximum Peak Current

The maximum boost inductor peak current is set using external resistor R_{IPK} on pin IPK, which is sampled periodically by an ADC. Maximum power output is proportional to peak current code $I_{PK(code)}$. See Equation 1:

$$P_{IN(max)} = \frac{\delta(I_{PK(BST)} \times V_{rms(typ)})}{2} \quad [Eq.1]$$

where,

δ = a correction term of 0.55

$V_{rms(typ)}$ = nominal operating input RMS voltage

$I_{PK(BST)}$ = peak current code $I_{PK(code)} \times 4.1\,mA$

Resistor R_{IPK} is calculated using peak current code $I_{PK(code)}$. See Equation 2:

$$R_{IPK} = \frac{4M\Omega}{I_{PK(code)}} \quad [Eq.2]$$

5.4.2 Output BSTOUT Sense & Input IAC Sense

A current proportional to boost output voltage V_{BST} is supplied to the IC on pin BSTOUT and is used as a feedback control signal (see Figure 12). The ADC is used to measure the magnitude of current I_{BSTOUT} through resistor R_{BST}. The magnitude of current I_{BSTOUT} is then compared to an internal reference current I_{ref} of 133µA.

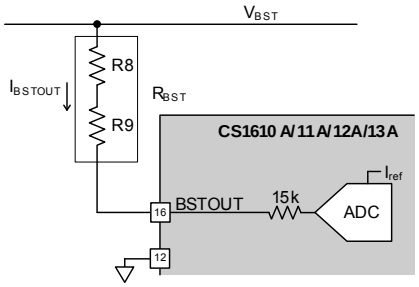


Figure 12. BSTOUT Input Pin Model

Resistor R_{BST} sets the feedback current at the nominal boost output voltage. For the CS1611A/13A, resistor R_{BST} is calculated as shown in Equation 3:

$$R_{BST} = \frac{V_{BST}}{I_{ref}} = \frac{400V}{133\mu A} \cong 3M\Omega \quad [Eq.3]$$

where,

V_{BST} = nominal boost output voltage

I_{ref} = internal reference current

For 120VAC line voltage applications (CS1610A/12A), nominal boost output voltage V_{BST} is 200V, and resistor R_{BST} is 1.5MΩ.

By using digital loop compensation, the voltage feedback signal does not require an external compensation network.

A current proportional to the AC input voltage is supplied to the IC on pin IAC and is used by the boost control algorithm (see Figure 13).

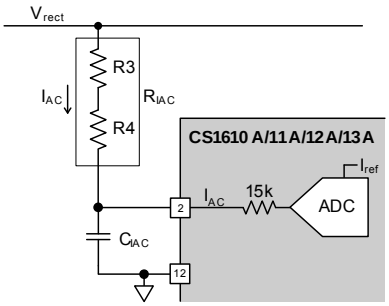


Figure 13. IAC Input Pin Model

Resistor R_{IAC} sets current I_{AC} and is defined in Equation 4:

$$R_{IAC} = R_{BST} \quad [Eq.4]$$

For optimal performance, capacitor C_{IAC} should be connected from pin IAC to ground in 230V circuits using the CS1611A or CS1613A. Resistors R_{IAC} and R_{BST} should use 1% or better resistors for best V_{BST} voltage accuracy.

5.4.3 Boost Auxiliary Winding

The boost auxiliary winding is used for zero-current detection (ZCD). The voltage on the auxiliary winding is sensed through the BSTAUX pin of the IC. It is also used to deliver current during steady-state operation, as mentioned in section 5.2 *Startup Circuit* on page 8.

5.4.4 Boost Overvoltage Protection

The CS1610A/11A/12A/13A supports boost overvoltage protection (BOP) to protect the bulk capacitor C8 (see Figure 15). If the boost output voltage exceeds the overvoltage protection thresholds of 249V for a 120V system, or 448V for a 230V system, a BOP fault signal is generated. The control logic continuously averages this BOP fault signal, and if at any point in time the average exceeds a set event threshold, the boost stage is disabled. The BOP fault averaging algorithm sets the event threshold such that the boost output voltage is never allowed to stay above the BOP threshold for more than 1.6ms.

During a boost overvoltage protection event, the second stage is kept enabled, and its dim input is railed to full scale. This allows the second stage to dissipate the stored energy on bulk capacitor C8 quickly, bringing down the boost output voltage to a safe value. A visible flash on the LED might appear, indicating that an overvoltage event has occurred. When the boost output voltage drops to 195V for a 120V application or 368V for a 230V application, the boost stage is enabled, and the system returns to normal operation.

5.5 Voltage Clamp Circuit

To keep dimmers conducting and prevent them from misfiring, a minimum power needs to be delivered from the dimmer to the load. This power is nominally around 2W for 230V and 120V TRIAC dimmers. At low dim angles (≤90°), this excess power cannot be converted into light by the second output stage due to the dim mapping at light loads. Boost stage output voltage V_{BST} can rise above the safe operating voltage of the primary-side bulk capacitor C8.

The CS1610A/11A/12A/13A provides active clamp circuitry on the CLAMP pin, as shown in Figure 14.

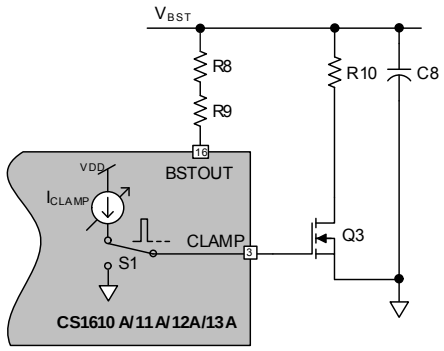


Figure 14. CLAMP Pin Model

A PWM control loop ensures that boost output voltage V_{BST} does not exceed 227V for 120VAC applications or 432V for 230VAC applications. This control turns on the MOSFET of the voltage clamp circuit, allowing the clamp circuit to sink current through the load resistor R10, preventing boost output voltage V_{BST} from exceeding the maximum safe voltage.

5.5.1 Clamp Overpower Protection

The CS1610A/11A/12A/13A clamp overpower protection (COP) digital controlled timer clocks the turn-on time of the clamp circuit over a one second period. If within a given one second period the clamp circuit turn-on time exceeds 51.2ms for a CS1610A/12A or 76.8ms for a CS1611A/13A a COP fault condition occurs and the system shuts down. If after any given one second period a COP event does not occur, the timer is reset to zero. The COP fault state is not cleared until the power to the IC is recycled.

5.6 Dimming Signal Extraction and the Dim Mapping Algorithm

When operating with a dimmer, the dimming signal is extracted in the time domain and is proportional to the conduction angle of the dimmer. A control variable is passed to the quasi-resonant second stage to achieve 2% to 100% output currents.

5.7 Quasi-resonant Second Stage

The second stage is a quasi-resonant current-regulated DC-DC converter capable of flyback or buck operation, delivering the highest possible efficiency at a constant current while minimizing line frequency ripple. Primary-side control is used to simplify system design and reduce system cost and complexity.

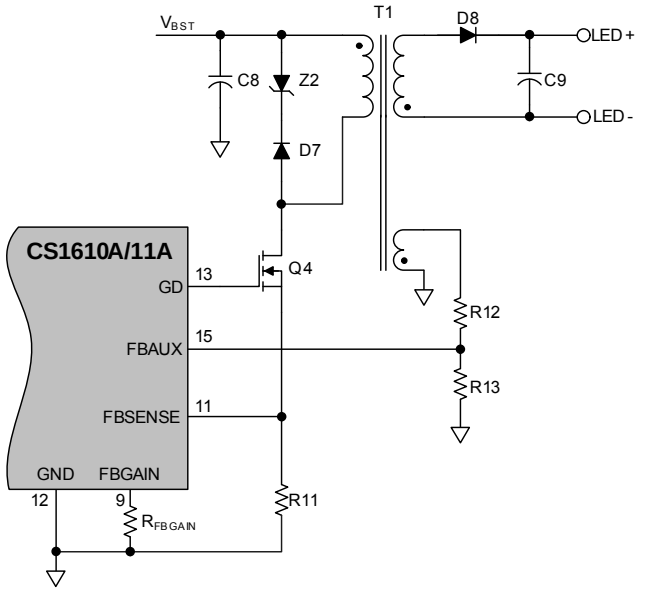


Figure 15. Flyback Model

The digital algorithm ensures monotonic dimming from 2% to 100% of the dimming range with a linear relationship between the dimming signal and the LED current. The flyback stage is controlled by sensing current in the transformer primary.

A quasi-resonant buck stage is illustrated in Figure 16. The buck stage is controlled by measuring current in the buck inductor and voltage on the auxiliary winding.

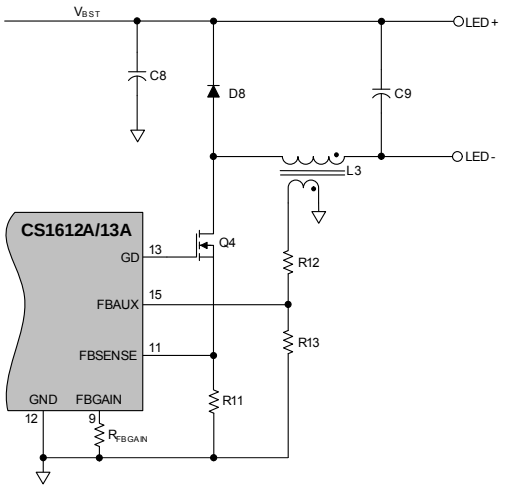


Figure 16. Buck Model

The digital buck algorithm ensures monotonic dimming from 2% to 100% of the dimming range with a linear relationship between the dimming signal and the LED current.

Quasi-resonant operation is achieved by detecting second stage inductor demagnetization via an auxiliary winding. The digital control algorithm rejects line-frequency ripple created on the second stage input by the front-end boost stage, resulting in the highest possible LED efficiency and long LED life.

5.7.1 Auxiliary Winding Configuration

The auxiliary winding is also used for zero-current detection (ZCD) and overvoltage protection (OVP). The auxiliary winding is sensed through the FBAUX pin of the IC.

5.7.2 Control Parameters

The second stage control parameters assure the following:

- **Line Regulation** — The LED current remains constant despite a ±10% AC line voltage variation.
- **Effect of Variation in Transformer Magnetizing Inductance** — The LED current remains constant over a ±20% variation in magnetizing inductance.

The second stage requires three inputs and generates one key output. The FBSENSE pin is used to sense the current in the second stage inductor. When the current reaches a certain threshold, the gate drive turns 'OFF' (output on pin GD). The sensed current and the FB_{Gain} input are used to determine the total switching period TT. The zero-current detect input on pin FBAUX is used to determine the demagnetization period T2. The controller then uses the total switching period TT to determine gate turn-on time.

The FB_{Gain} input is set using resistor R_{FBGAIN}. Resistor R_{FBGAIN} must be selected to ensure that the switching period TT is greater than the resonant switching period $T_{critical}$ at maximum output power. See Equation 5:

$$TT > (T_{critical} = T1 + T2) \quad \text{[Eq. 5]}$$

where,

$T_{critical}$ = resonant switching period at max power

T1 = gate turn-on time

T2 = demagnetization time

Total switching period TT is computed for flyback topology using Equation 6:

$$TT \propto I_{PK(FB)} \times T2 \times \frac{FB_{Gain}}{\tau} \quad \text{[Eq. 6]}$$

where,

τ = dimming factor, proportional to the duty cycle of the dimmer; between 0 and 1

$I_{PK(FB)}$ = transformer primary winding current

FB_{Gain} = constant TT/T2; computed at full load

For buck topology, the switching period TT is computed using Equation 7:

$$TT \propto I_{PK(FB)} \times (T1 + T2) \times \frac{FB_{Gain}}{\tau} \quad \text{[Eq. 7]}$$

where,

τ = dimming factor, proportional to the duty cycle of the dimmer, between 0 and 1

$I_{PK(FB)}$ = transformer primary winding current

FB_{Gain} = constant TT/(T1 + T2); computed at full load

An appropriate value for resistor R_{FBGAIN} needs to be selected to provide the correct gain constant FB_{Gain}. Resistor R_{FBGAIN} is calculated using Equation 8:

$$R_{FBGAIN} = \frac{62.5k\Omega}{(FB_{Gain} \times 2) - 1} \quad \text{[Eq. 8]}$$

The value of gain constant FB_{Gain} also has a bearing on the linearity of the dimming factor versus the LED current curve and must be selected using Application Note AN364: *Design Guide for a CS1610 and CS1611 Dimmer-compatible SSL Circuit* and AN372: *Design Guide for a CS1612 and CS1613 Dimmer-compatible SSL Circuit*.

5.7.3 Output Open Circuit Protection

Output open circuit protection and output overvoltage protection (OVP) is implemented by monitoring the output voltage through the transformer auxiliary winding. If the voltage on the FBAUX pin exceeds OVP threshold $V_{OVP(th)}$ of 1.25V, a fault condition occurs. The IC output is disabled, and the controller attempts to restart after one second.

5.7.4 Overcurrent Protection

Overcurrent protection (OCP) is implemented by monitoring the voltage across the second stage sense resistor. If this voltage exceeds OCP threshold $V_{OCP(th)}$ of 1.69V, a fault condition occurs. The IC output is disabled, and the controller attempts to restart after one second.

5.7.5 Open Loop Protection

Both open loop protection (OLP) and protection against a short of the second stage sense resistor are implemented by monitoring the voltage across the sense resistor. If the voltage on pin FBSENSE does not reach protection OLP threshold $V_{OLP(th)}$ of 200mV, the IC output is disabled, and the controller attempts to restart after one second.

5.8 Overtemperature Protection

The CS1610A/11A/12A/13A incorporates both internal overtemperature protection (iOTP) and the ability to connect an external overtemperature sense circuit for IC protection. Typically, a negative temperature coefficient (NTC) thermistor is used.

5.8.1 Internal Overtemperature Protection

Internal overtemperature protection (iOTP) is activated, and switching is disabled, when the die temperature of the device exceeds 135°C. There is a hysteresis of about 14°C before resuming normal operation.

5.8.2 External Overtemperature Protection

The external overtemperature protection (eOTP) pin is used to implement overtemperature protection using an external NTC thermistor. The total resistance on the eOTP pin is converted to an 8-bit digital 'CODE' (which gives an indication of the temperature) using a digital feedback loop, which adjusts current $I_{CONNECT}$ into the NTC thermistor and series resistor R_S to maintain a constant reference voltage $V_{CONNECT(th)}$ of 1.25V. Figure 17 illustrates the functional block diagram when connecting an optional external NTC temperature sensor to the eOTP circuit.

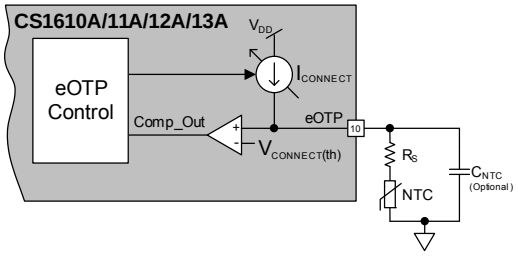


Figure 17. eOTP Functional Diagram

Current $I_{CONNECT}$ is generated from an 8-bit controlled current source with a full-scale current of 80µA. See Equation 9:

$$I_{CONNECT} = \frac{V_{CONNECT(th)}}{R} \quad \text{[Eq. 9]}$$

When the loop is in equilibrium, the voltage on pin eOTP fluctuates around voltage threshold $V_{CONNECT(th)}$. The digital 'CODE' output by the ADC is used to generate current $I_{CONNECT}$. In normal operating mode, current $I_{CONNECT}$ is updated once every seventh half line-cycle by a single ± LSB step. See Equation 10:

$$CODE \times \left[\frac{I_{CONNECT}}{2^N}\right] = \frac{V_{CONNECT(th)}}{R_{NTC} + R_S} \quad \text{[Eq. 10]}$$

Using Equation 10 solve for digital CODE. See Equation 11:

$$CODE = \frac{2^N \times V_{CONNECT(th)}}{I_{CONNECT} \times (R_{NTC} + R_S)}$$

$$= \frac{256 \times 1.25\,V}{(80\mu A) \times (R_{NTC} + R_S)} \quad \text{[Eq. 11]}$$

$$= \frac{4M\Omega}{(R_{NTC} + R_S)}$$

The tracking range of this resistance ADC is approximately 15.5kΩ to 4MΩ. The series resistor R_S is used to adjust the resistance of the NTC thermistor to fall within this ADC tracking range so that the entire 8-bit dynamic range of the ADC is well used. A 14kΩ (±1% tolerance) series resistor is required to allow measurements of up to 130°C to be within the eOTP tracking range when a 100kΩ NTC thermistor with a Beta of 4334 is used. The eOTP tracking circuit is designed to function accurately with external capacitance up to 470pF. A higher 8-bit code output reflects a lower resistance and hence a higher external temperature.

The ADC output code is filtered to suppress noise and compared against a reference code that corresponds to 125/130°C. If the temperature exceeds this threshold, the chip enters an external overtemperature state and shuts down. This is not a latched protection state, and the ADC keeps tracking the temperature in this state in order to clear the fault state once the temperature drops below 110°C.

When exiting reset, the chip enters startup and the ADC quickly (<5ms) tracks the external temperature to check if it is below the 110°C reference code before the boost and second stages are powered up. If this check fails, the rest of the system will not be initialized until the external temperature is below 110°C.

For external overtemperature protection, a second low-pass filter with a time constant of two minutes filters the ADC output and uses it to scale down the internal dim level of the system (and hence LED current I_{LED}) if the temperature exceeds 95°C (see Figure 18). The large time constant for this filter ensures that the dim scaling does not happen spontaneously and is not noticeable (suppress spurious glitches). LED current I_{LED} starts reducing when resistor R_{NTC} is approximately 6.3kΩ (assuming a 14kΩ, ±1% tolerance, series resistor), which corresponds to a temperature of 95°C for a 100kΩ NTC (100kΩ at 25°C). LED current I_{LED} is scaled until the NTC thermistor value reaches 2.5kΩ (125°C). The CS1610A/11A/12A/13A uses this calculated value to scale output LED current I_{LED}, as shown in Figure 18.

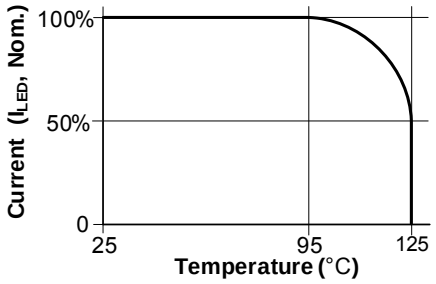
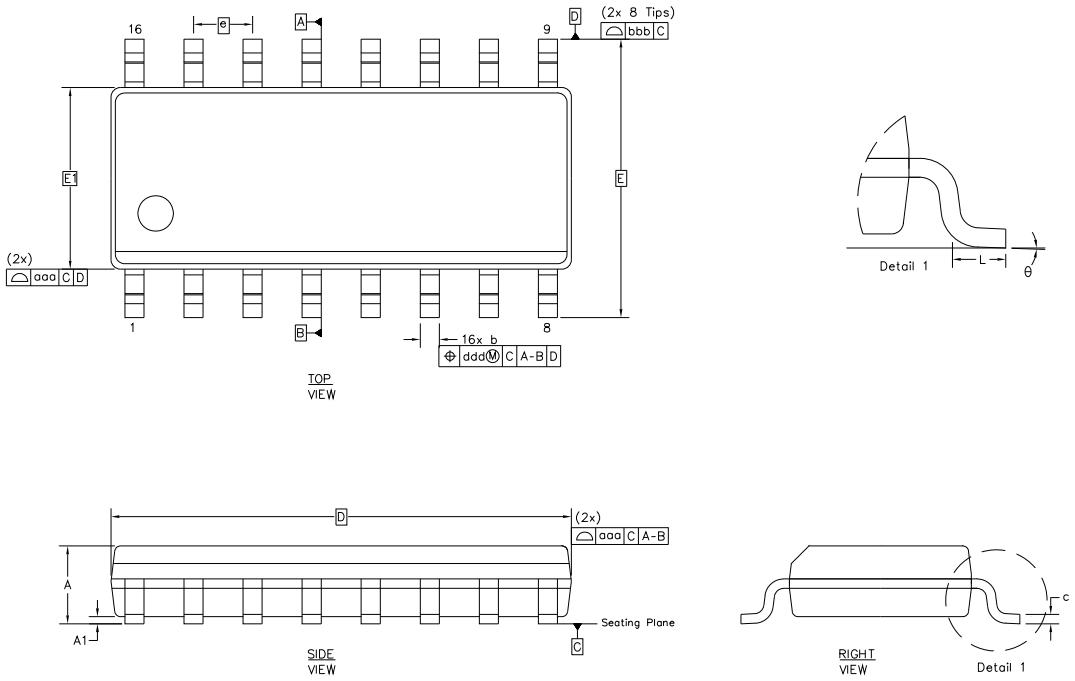


Figure 18. LED Current vs. eOTP Temperature

Beyond this temperature, the IC shuts down using the mechanism discussed above. If the external overtemperature protection feature is not required, connect the eOTP pin to GND using a 50kΩ-to-500kΩ resistor to disable the eOTP feature.

6. PACKAGE DRAWING

16-PIN SOICN (150 MIL BODY)



	mm			inch		
Dimension	**MIN**	**NOM**	**MAX**	**MIN**	**NOM**	**MAX**
A	- -	- -	1.75	- -	- -	0.069
A1	0.10	- -	0.25	0.004	- -	0.010
b	0.31	- -	0.51	0.012	- -	0.020
c	0.10	- -	0.25	0.004	- -	0.010
D	9.90 BSC			0.390 BSC		
E	6.00 BSC			0.236 BSC		
E1	3.90 BSC			0.154 BSC		
e	1.27 BSC			0.050 BSC		
L	0.40	- -	1.27	0.016	- -	0.050
Θ	0°	- -	8°	0°	- -	8°
aaa	0.10			0.004		
bbb	0.25			0.010		
ddd	0.25			0.010		

Notes:
1. Controlling dimensions are in millimeters.
2. Dimensions and tolerances per ASME Y14.5M.
3. This drawing conforms to JEDEC outline MS-012, variation AC for standard 16 SOICN narrow body.
4. Recommended reflow profile is per JEDEC/IPC J-STD-020.

7. ORDERING INFORMATION

Ordering Number	Container	AC Line Voltage	Temperature Range	Package Description
CS1610A-FSZ	Bulk	120VAC	-40 °C to +125 °C	16-lead SOICN, Lead (Pb) Free
CS1610A-FSZR	Tape & Reel			
CS1611A-FSZ	Bulk	230VAC	-40 °C to +125 °C	16-lead SOICN, Lead (Pb) Free
CS1611A-FSZR	Tape & Reel			
CS1612A-FSZ	Bulk	120VAC	-40 °C to +125 °C	16-lead SOICN, Lead (Pb) Free
CS1612A-FSZR	Tape & Reel			
CS1613A-FSZ	Bulk	230VAC	-40 °C to +125 °C	16-lead SOICN, Lead (Pb) Free
CS1613A-FSZR	Tape & Reel			

8. ENVIRONMENTAL, MANUFACTURING, & HANDLING INFORMATION

Part Number	Peak Reflow Temp	MSL Rating[a]	Max Floor Life[b]
CS1610A-FSZ	260°C	3	7 Days
CS1611A-FSZ	260°C	3	7 Days
CS1612A-FSZ	260°C	3	7 Days
CS1613A-FSZ	260°C	3	7 Days

a. MSL (Moisture Sensitivity Level) as specified by IPC/JEDEC J-STD-020.

b. Stored at 30°C, 60% relative humidity.

9. REVISION HISTORY

Revision	Date	Changes
PP1	JAN 2012	Initial release.
PP2	APR 2012	Removed ambient temperature range specification, increased power dissipation specification. Corrected typographical errors.
PP3	MAR 2013	Added Center-cut Mode and context corrections.
PP4	AUG 2013	Content clarification

Contacting Cirrus Logic Support

For all product questions and inquiries contact a Cirrus Logic Sales Representative.
To find one nearest you go to http://www.cirrus.com