EQCO62T20.3 6.25 Gbps Asymmetric Coax Driver
EQCO31T20.3 3.125 Gbps Asymmetric Coax Driver

1.1 Introduction

The EQCO62X20[1] chipset is a driver/equalizer chipset that forms a bidirectional full duplex communication link over a single coax cable.

The EQCO62X20 chipset is designed to transport up to 6.25 Gbps over the downlink channel and to transport 21 Mbps over the uplink channel. The *EQCO62T20* is designed to transmit the downlink signal up to 6.25 Gbps and receive the uplink signal. The *EQCO62R20* is designed to receive the downlink signal up to 6.25 Gbps and to transmit the uplink signal. Power can be transferred over the same cable via external inductors.

The chipset is designed to work with several types of 75 Ω coaxial cables including legacy cables as well as thin flexible lightweight cables.

1.2 Applications

This solution is useful and economical for many markets and applications, including the following:

- High definition Camera links
- Machine Vision, Military, Aerospace, Medical, Broadcast & Surveillance cameras
  - Single coax cable carries power, video data and camera control stream

1.3 Features

- Complies with the CoaXPress v1.1 camera standard [1]
- Supports up to 68 meters of cable at 6.25 Gbps using high quality coax
- Supports up to 212 meters of cable at 1.25 Gbps using high quality coax
- Single chip solutions for both the camera side and the frame grabber side, making a bidirectional connection over a single 75 Ω coax cable
- Full duplex bidirectional data channel
  - Downlink speeds from 1.25 Gbps up to 6.25 Gbps; differential interfacing straightforward with internal termination resistors
  - Flexible, protocol agnostic uplink supporting up to 21 Mbps, allowing nanoseconds precise triggering events driven by the frame grabber
- Supports Power distribution over the coax up to 900 mA, on top of the data signals allowing to power the camera through the same coax
- Low power consumption (<70 mW, 1.2 V supply)
- 16-pin, 0.65 mm pin pitch, 4 mm QFN package
- Small PCB footprint for EQCO62T20 and off-chip components, with guaranteed RF-performance
- -40 - +85 ˚C industrial temperature range
- Pb-free and RoHS compliant

[1] The EQCO31T20 and EQCO31R20 are lower speed versions of the EQCO62T20 and EQCO62R20, with a maximum bit rate of 3.125 Gbps for the high speed downlink and the same uplink speed.

1.4 Typical Link Performance

Table 1 gives an overview of typical link performance at room temperature for the link containing the EQCO62T20.3 coax driver in conjunction with the EQCO62R20.3 receiver, using the downlink channel, uplink channel and power transmission simultaneously. Performance for EQCO62X20.3 and EQCO31X20.3 is equal for bit rates up to 3.125 Gbps.

BELDEN

Name		Belden 7731A	Belden 1694A	Belden 1505A	Belden 1505F	Belden 1855A
	Type	Long Distance	Industry Standard	Compromis Coax	*Flexible*	Thinnest cable
Diameter	(mm)	10.3	6.99	5.94	6.15	4.03
1.25 Gbps	(m)	194	130	107	80	55
2.5 Gbps	(m)	162	110	94	66	55
3.125 Gbps	(m)	147	100	86	60	55
5.0 Gbps	(m)	87	60	52	35	38
6.25 Gbps	(m)	58	40	35	23	25

GEPCO

Name		Gepco VHD1100	Gepco VSD2001	Gepco VPM2000	Gepco VHD2000M	Gepco VDM230
	Type	Long Distance	Industry Standard	Compromis Coax	*Flexible*	Thinnest cable
Diameter	(mm)	10.3	6.91	6.15	6.15	4.16
1.25 Gbps	(m)	212	140	109	81	66
2.5 Gbps	(m)	185	120	94	67	66
3.125 Gbps	(m)	169	110	86	61	62
5.0 Gbps	(m)	102	66	53	36	38
6.25 Gbps	(m)	68	44	35	24	25

CANARE*

Name		Canare L-7CFB	Canare L-5CFB	Canare L-4CFB	Canare L-3CFB	Canare L-2.5CFB
	Type	Long Distance	Industry Standard	Compromis Coax	Thin Cable	Thinnest Cable
Diameter	(mm)	10.2	7.7	6.1	5.5	4
1.25 Gbps	(m)	165	118	94	72	43
2.5 Gbps	(m)	135	98	79	66	43
3.125 Gbps	(m)	122	88	71	60	43
5.0 Gbps	(m)	71	52	42	36	30
6.25 Gbps	(m)	46	34	28	24	20

* specs from Canare only up to 2GHz, 5 Gbps and 6.25 Gbps performance are by extrapolation!

Table 1: Typical link performance

2 Functional Description

2.1 Overview

The EQCO62X20 single coax chipset is designed to simultaneously transmit and receive signals on a single 75 Ω coax cable. In one direction a downlink signal is transmitted. In the opposite direction a lower speed uplink is provided. The EQCO62X20 chipset consists of 2 chips. The EQCO62T20 is a high speed line driver with integrated low speed receiver. The EQCO62R20 is a high speed receiver with integrated low speed transmitter. Figure 1 illustrates a typical EQCO62X20 link set-up.

The downlink signal is transmitted with 600 mV transmit amplitude at the EQCO62T20 side. This signal is attenuated in the coax and recovered by an equalizer [2] integrated in the EQCO62R20. The low speed uplink [3] is transmitted with a lower amplitude of 130 mV to limit the crosstalk with the downlink channel.

The downlink channel is intended for 8B/10B NRZ coded data with bitrates from 1.25 Gbps up to 6.25 Gbps. The low speed uplink has a maximum bit rate of 21 Mbps and has a single ended LVTLL input and output. The uplink can operate with DC balanced, DC unbalanced or even burst mode data.

On top of the downlink channel and the low speed uplink the system allows power transmission over the coax by using ferrite beads and external inductors [4]. These external inductors give the communication channel a high pass characteristic. The uplink receiver inside the EQCO62T20 chip recovers the signal lost by this high pass filter. Appropriate inductors need to be selected for correct operation of the link. Correct operation is only guaranteed with the inductor combination used in our evaluation board, even though other components might be suited.

The EQCO62X20 chipset is compatible with the CoaXPress v1.0 camera standard.

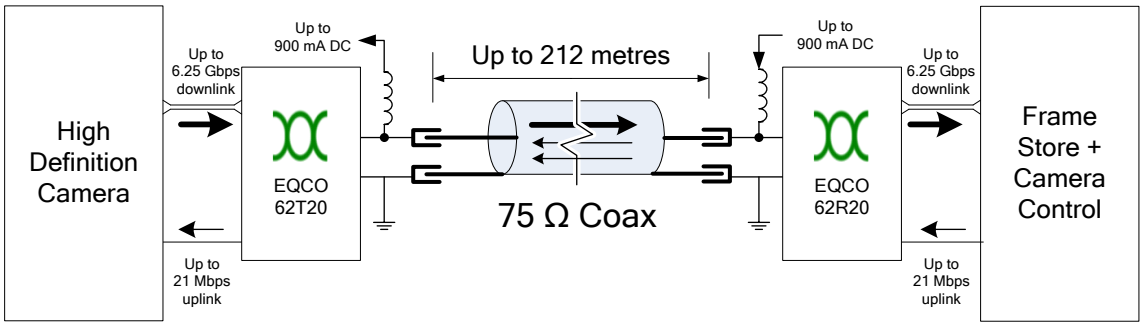

Figure 1: Typical EQCO62X20 link set-up

2.2 Package and Pinout

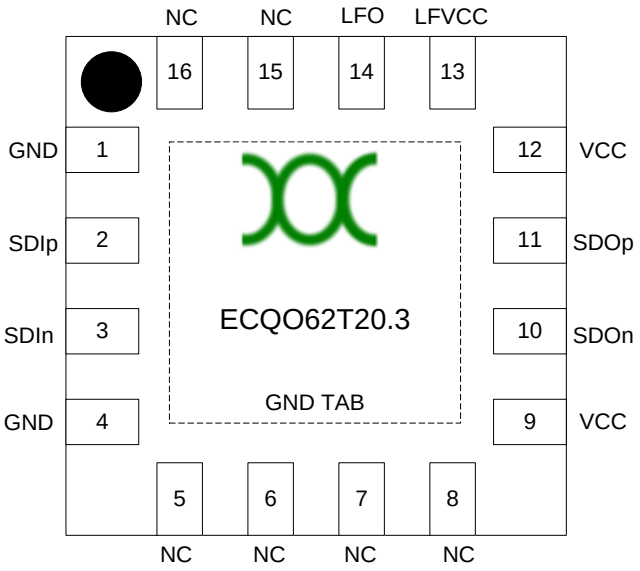

Figure 2: EQCO62T20.3 Pin Layout (viewed from top)

2.3 Pin Descriptions

Pin Number	Pin Name	Signal Type	Description
(TAB)	GND	Power	Connect to Ground
9,12	VCC	Power	Connect to +1.2V of power supply
1,4	GND	Power	Connect to ground of power supply
2,3	SDIp/SDIn	Differential Input	Serial Input Positive/Negative Differential serial input. Typical input swing is 2x300 mV. Minimal input swing is 2x250 mV. 2x50 Ω on-chip termination resistor
11,10	SDOp/SDOn	Differential Output	Differential serial output pair. On-chip 75 Ω termination resistors. SDOp is connected to the coax cable by a capacitor. SDOn needs to be connected to GND by 75 Ω termination resistor and capacitor. Swing is fixed to VCC/2
13	LFVCC	Power	Power supply for the uplink output. (between 1.2 V and 3.3 V)
14	LFO	Output	Low Frequency uplink Output. LVTTL with output swing equal to LFVCC. Supports capacitive loads up to 20 pF for 21 Mbps operation
5,6,7,8,15,16	NC		DO NOT CONNECT, leave these pins floating. Used for internal testing.

Table 2: EQCO62T20.3 Device Pin List

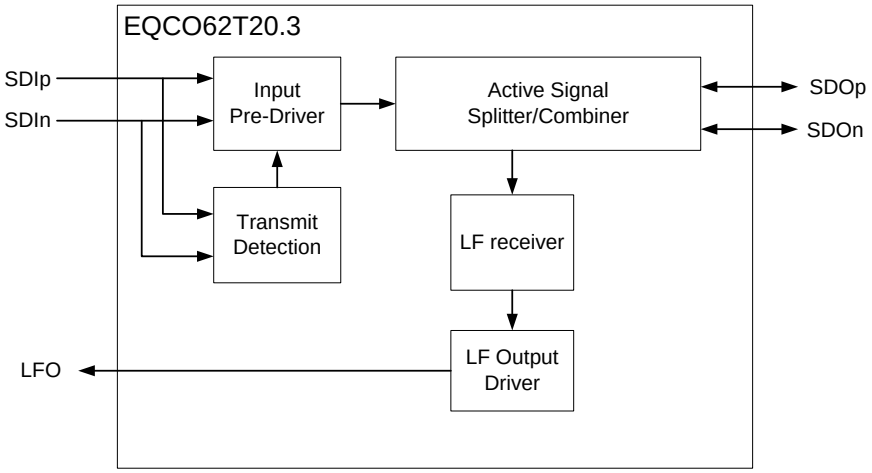

Figure 3: EQCO62T20.3 block diagram showing electrical connections

2.3.1 SDIp/SDIn

SDIp/SDIn together form a differential input pair. The serial data received on these pins will be transmitted on SDOp/SDOn. The Input Pre-Driver automatically corrects for variations in signal levels and different edge slew rates at these inputs before they go into the Active Splitter/Combiner for transmission over the coax.

Between SDIp and SDIn inputs there is a termination resistor of 100 Ω. The intention is to always use AC coupling.

A Transmit Wake-up detection circuit puts both the Input Pre-Driver and the output driver into a low power mode when no signal is detected on the SDIp/SDIn signal pair.

2.3.2 SDOp/SDOn

The signal at the inputs SDIp/SDIn is transmitted onto the cable by outputs SDOp/SDOn. Both outputs are internally terminated with 75 Ω.

The signal on the SDOp pin is the sum of the incoming signal (i.e. the signal transmitted by the EQCO62R20 on the far end side of the coax) and the outgoing signal (i.e. the signal created based on SDIp/SDIn). The far end signal is extracted by subtraction of the near end signal and the far end signal and is restored by the uplink receiver inside the EQCO62T20 chip. The SDOn signal carries a precise anti-phase signal to the transmitted signal on SDOp. SDOn must be connected directly to GND **at the connector** via a resistor precisely matched to the impedance of the coaxial cable used and an AC coupling capacitor.

2.3.3 LFO

LFO is the output of the uplink receiver inside the EQCO62T20. The maximum allowed capacitance at the output is 20 pF with rise and fall times of 5 ns. The maximum output current is 1mA when LFVCC is 3.3 V.

2.3.4 LFVCC

The output driver of the uplink receiver in the EQCO62T20 has a separate power supply pin. The power supply voltages can be 1.2 V up to 3.3 V. The output swing at LFO is equal to this power supply voltage. A filter capacitor must be placed close to the LFVVC pin of the EQCO62T20.

2.4 Circuit Operation

2.4.1 Pre-driver

The Pre-driver removes any dependency for the amplitude and rise time of the incoming signal on SDI.

2.4.2 Active signal splitter/combiner

The active splitter/combiner controls the amplitude and rise time of the outgoing coax signal and transmits it via a 75 Ω output termination resistor. The output resistor when balanced with the coax characteristic impedance also forms part of a hybrid splitter circuit which subtracts the TX output from the signal on the SDO output to give yield the far end TX signal.

2.4.3 Transmit detection

The transmit detection detects if an input signal is applied at SDI. The detection circuit looks at the signal amplitude of SDI. If no signal is detected the pre-driver and output driver are disabled. The LF receiver then continues to operate independently. At the moment the output driver is turned-on or off, there can be a bit error in the uplink channel, i.e. by the LF-receiver.

2.4.4 LF receiver

The uplink receiver removes unwanted crosstalk from the transmitted near end signal. Afterwards the uplink signal is restored by detecting edges coming from the uplink signal. At the moment the output driver is turned-ON or OFF, there can be a bit error in the uplink channel, i.e. by the LF-receiver. The initial output state of the LF receiver can be wrong, subsequent bits will be received correctly.

2.4.5 LF output driver

The uplink output driver converts the detected signal by the LF receiver to a LVTTL signal with a controlled rise and fall time. It is required to set the output signal amplitude of this LVTTL signal by connecting the LFVCC to the appropriate power supply voltage (max 3.3V).

3 Electrical Specifications

3.1 Absolute Maximum Ratings

Stresses beyond those listed under this section may cause permanent damage to the device. These are stress ratings only and are not tested. Functional operation of the device at these or any other conditions beyond those indicated in the operational sections are not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Parameter	Conditions	Min	Typ	Max	Units
Storage Temperature		-65		+150	°C
Ambient Temperature	Power Applied	-55		+125	°C
Operating Temperature	Normal Operation (VCC=1.2 V±5%)	-40		+85	°C
Supply Voltage to Ground		-0.5		+1.4	V
DC Input Voltage		-0.5		+1.6	V
DC Voltage to Outputs		-0.5		+1.6	V
Current into Outputs	Outputs Low			90	mA
Electro Static Discharge (ESD) HBM	JEDEC EIA/JESD-A114A	>2.2			kV
Electro Static Discharge (ESD) contact	IEC 61000-4-2	>8			kV
Latch-Up Current		>100			mA(DC)

Table 3: Absolute Maximum Ratings

3.2 Electrical Characteristics

Parameter	Description	Min	Typ	Max	Unit
Power supply					
V_{CC}	Supply Voltage	1.15	1.2	1.25	V
I_s	Supply Current, both transmitting and receiving		60		mA
I_{sr}	Supply Current when only receiving		30		mA
SDIp/SDIn Input					
ΔV_i	Input amplitude $V_{SDIp,n}$	2x250	2x300		mV
V_{turnon}	ΔV_i to turn on transmit function		2x150	2x250	mV
$V_{turnoff}$	ΔV_i to turn off transmit function	2x50	2x150		mV
R_{input}	Differential input termination		2x50		Ω
SDOp connection to Coax					
Z_{coax}	Coax Cable Characteristic Impedance		75		Ω
R_{SDOp}	Input impedance between SDOp and VCC/GND		75		Ω
R_{loss}	Coax Return Loss as seen on SDOp pin Frequency range = 5 MHz - 1 GHz			-15	dB
R_{loss}	Coax Return Loss as seen on SDOp pin Frequency range = 1 GHz-1.5 GHz			-10	dB
R_{loss}	Coax Return Loss as seen on SDOp pin Frequency range = 1.5 GHz – 3.2 GHz			-7	dB

Parameter	Description	Min	Typ	Max	Unit
ΔV_{TX}	Transmit Amplitude	500	600	700	mV
t_{rise_tx}	Rise /fall time 20% to 80% of ΔV_{TX}			80	ps
DCD	Duty cycle distortion on of V_{SDOp}		5		ps
LFO Output (LVTTL like)					
LFVCC	Uplink output driver power supply	1.2		3.3	V
t_{rise_LFO}	Rise /fall time 20% to 80% of V_{LFO} for 20 pF load LFVCC = 1.2 V		6		ns
	LFVCC = 3.3 V		5		ns

Table 4: Electrical Characteristics (Over the Operating VCC and -40 to 85 ^{o}C Range)

3.3 Jitter Numbers

Parameter	Conditions	Min	Typ	Max	Units
Additive peak to peak jitter on SDOp/SDOn For EQCO62T20	Downlink signal = 1.25 up to 6.25 Gbps, prbs7			30	ps
For EQCO31T20	Downlink signal = 1.25 up to 3.125 Gbps, prbs7			30	ps
Peak to peak jitter on LFO	0-130 m Belden1694A coax, over full Vcc and temperature range; low speed signal = 21 Mbps, 8B/10B, downlink signal= 1.25-6.25 Gbps,8B/10B			15	ns

Table 5: Jitter numbers

4 Package Drawing

A 16 pin Micro Lead frame Package (MLP) also known as Quad Flat No Lead (QFN) package is used. The package outline conforms to JEDEC MO-220.

Dimensions in Figure 4 are in millimeters.

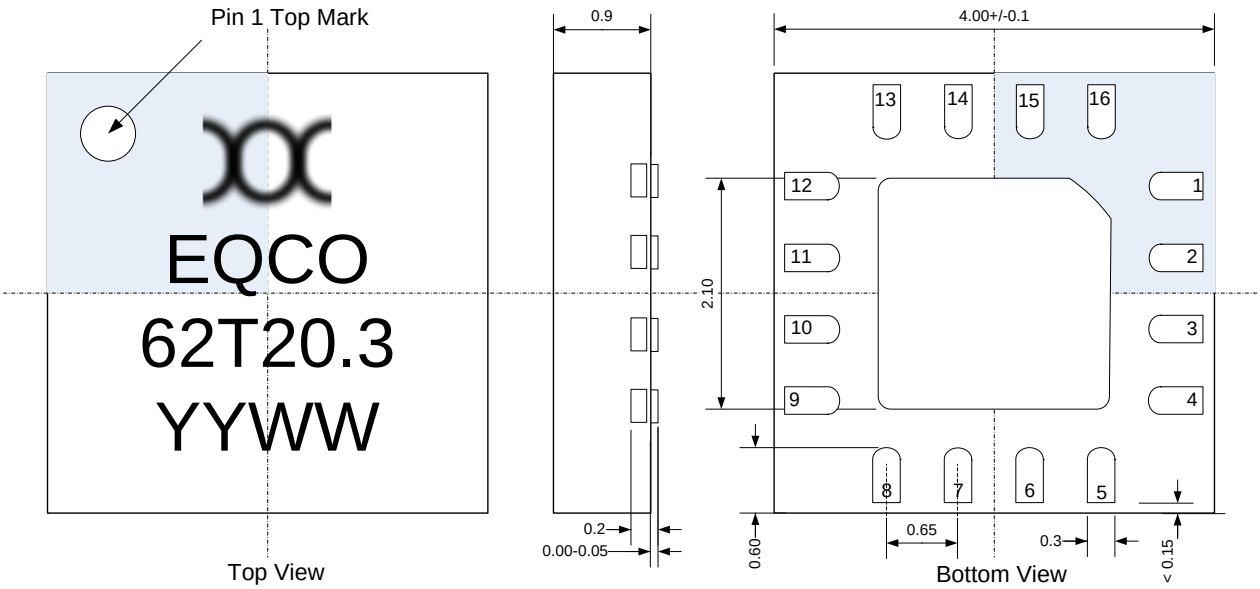

Figure 4: Package Drawing

5 Application Information

5.1 Typical Application Circuit

Figure 5 illustrates a typical schematic implementation:

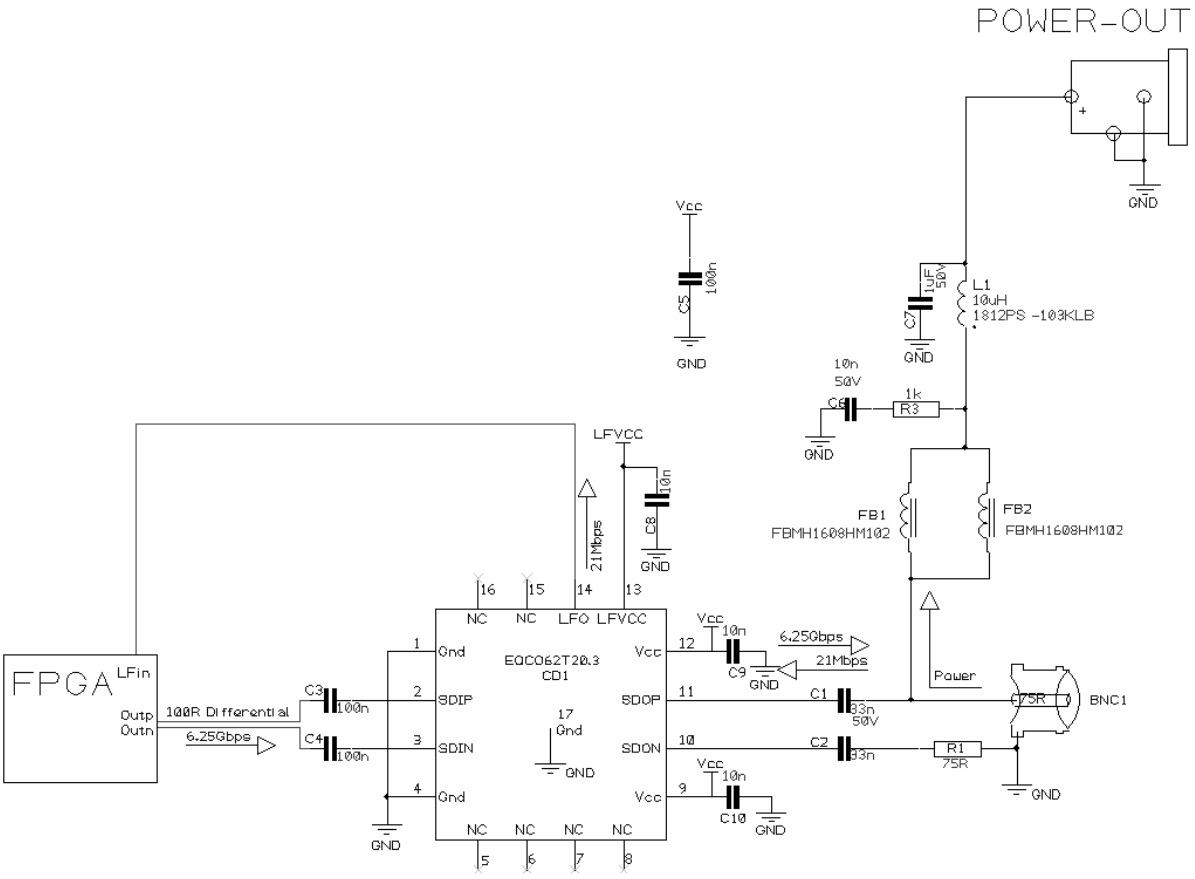

Figure 5: EQCO62T20.3 typical application circuit

5.2 Component recommendation

Element	Value	Size	Recommended component
Fb1, Fb2	1 kΩ @ 100 MHz ferrite bead	0603	FBMH1608HM102 from Taiyo Yuden (CRITICAL)
L1	10 µH	1812	1812PS_103 from Coilcraft (CRITICAL)
R1	75 Ω ±1 %	0402	
R3	1 kΩ	0402	

Element	Value	Size	Recommended component
C1	33 nF, 50V, X7R	0603	
C2	33 nF, X7R	0402/0603	
C3, C4, C5	100 nF, X7R	0402	
C6	10 nF, 50V, X7R	0402	
C7	1 µF, 50 V, X7R	0805	
C8,C9, C10	10 nF, X7R	0402	
BNC1	75 Ω right angle BNC connector		5413558-1from Tyco (Recommended)

Table 6: Component recommendation for the EQCO62T20.3 board layout

Ferrite Beads Fb1, Fb2 = FBMH1608HM102 from Taiyo Yuden and inductor L1 = 1812PS_103 from Coilcraft (10 µH) are recommended for CoaXPress. For other applications the inductor value can be larger leading to a physical larger inductor.

Connector BNC1 = 75 Ω right angle BNC connector 5413558-1 from Tyco, recommended for CoaXPress.

Other inductor/ferrite bead/BNC connector can possibly be used, however, they must be selected carefully for their RF-performance since performance can decrease significantly!

5.3 Guidelines for PCB layout

Important Guidance Note: Using the EQCO62X20 chipset at its full purpose, i.e. including low speed uplink and power-supply transmission it is important not to disturb the RF-performance of the high speed downlink channel. Implementing the circuit of Figure 5 with a different PCB layout will in first instance not deliver full data-sheet performance. The simplest way of meeting optimal performance (including jitter and return-loss requirements) is to precisely follow the component and layout recommendations. Note that at multi-Gigabit speeds, using "equivalent" components or small PCB layout changes (even moving a via) can have significant detrimental effects**For CoaXPress:** The easiest way for achieving the requirements of the CoaXPress 1.0 specification is to merely use the recommended circuits, components and layout of the PCB.For easy implementation EqcoLogic will provide the Gerber file, please ask for it by email[2]. Changes to the proposed PCB layout can be reviewed by EqcoLogic on request.

5.3.1 Right angle BNC

The Figure 6 below shows the 4 layers of the recommended footprint for the EQCO62T20.3 chip and the off-chip components that are critical for the RF-performance of the system.

[2] Email address: coaxpress@eqcologic.com

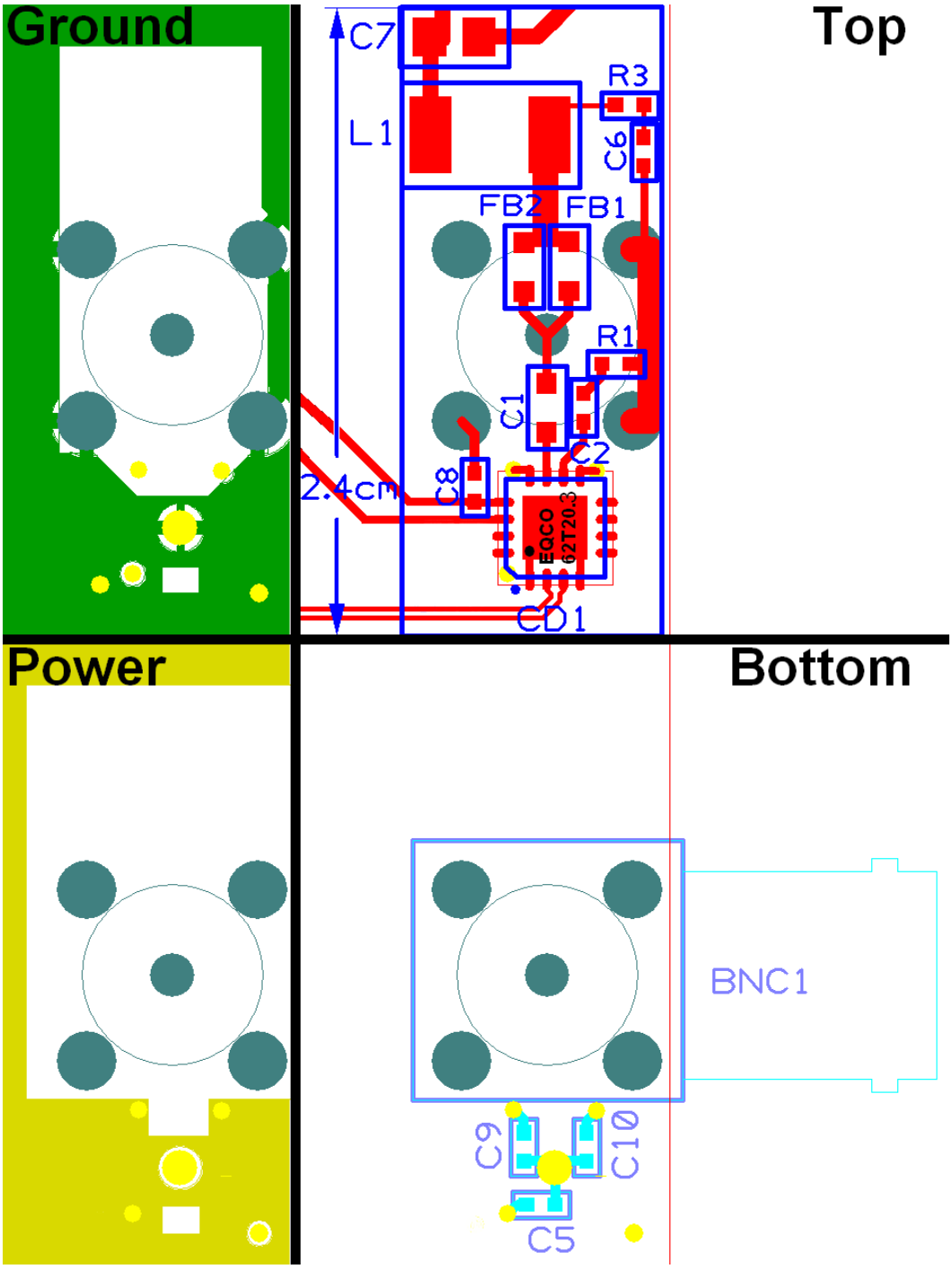

Figure 6: Recommended PCB layout for EQCO62T20.3

In this layout the size of the PCB area needed for the chip is minimized. Approximately the double of the BNC footprint area is required for the full bidirectional system including the necessary elements for the power transport.

The differential input of the chip must be a 100 Ω differential transmission line. To minimize the parasitic capacitance of the input pins a cut-out of the ground and power plane underneath the input pins is recommended. For best performance no via's should be used in this high speed signal path.

A large cut-out underneath the right angle BNC connector, the AC coupling capacitors, ferrite beads and inductor is needed for minimal parasitics.

This proposed layout is designed to be largely independent of the used PCB-layerstack. This will work as well for 4, 6 or even higher numbers of layers. Possible extra layers should have cut-outs as large as the full proposed footprint.

5.3.2 Multilane CoaXPress 4+1 layout with DIN1.0/2.3 Connectors

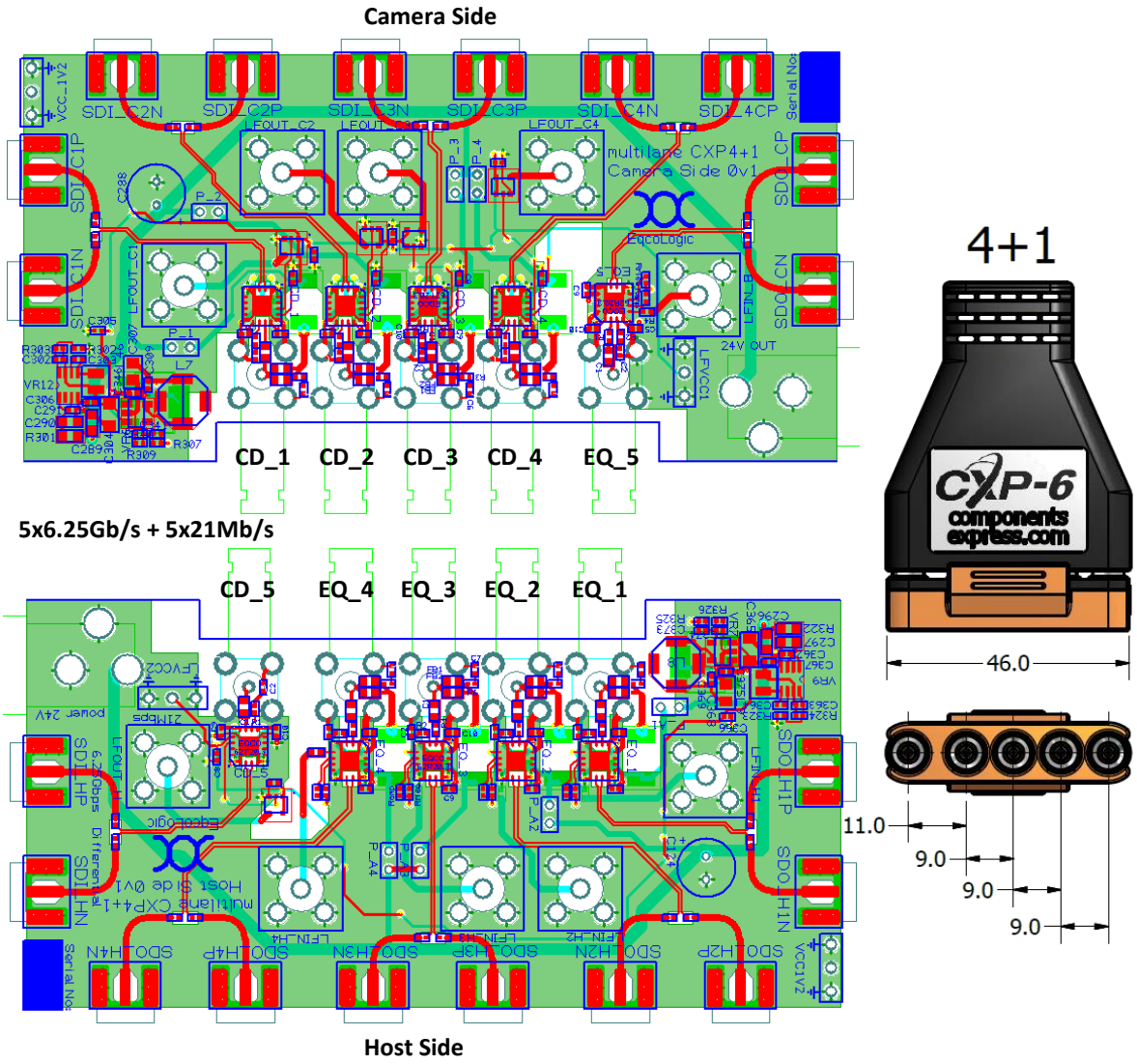

Figure 7: PCB layout of Multilane CoaXPress 0v1 demo board pair

Figure 7 shows an example of a Multilane CoaXPress 4+1setup. The recommended Din1.0/2.3 connector is the NPF 4076 from Cambridge Connectors. The cable example shows the pitches in mm. Figure 8 shows the 4 layers of the recommended footprints and off-chip components that are critical for RF-performance of the cable drivers CD_1 to CD_4 at the camera side, which have Power over CoaXPress (PoCXP). Figure 9 shows the variant without PoCXP used for CD_5 at the host side. The exact dimensions in mm are given in appendix4. It is recommended to copy these dimensions, especially the connection between the DIN1.0/2.3 connector and the chip, as this is a complex entity with coupled currents and compensated parasitic capacitances.

Despite the critical layout, this proposed layout is designed to be largely independent of the used PCB-layer stack, as the critical parts are mainly the top-layer only. This will work as well for 4, 6 or even higher numbers of layers. Possible extra layers should have cut-outs as large as the full proposed footprint.

In these layouts the size of the PCB area needed for the chip is minimized. This allows multiple lanes close together.

Only 2 of 4 connecter GND pins are connected to the GND plane to reduce the capacitance.

The differential CD inputs must be a 100 Ω differential transmission line. A cut-out of the ground and power plane underneath the input pins is recommended to minimize the parasitic capacitance. For best performance no via's should be used in this high speed signal path.

The Components Express 4+1 connector of Figure 7 is only shown as example. Other connector configurations are available with DIN1.0/2.3 connector such as 6+1, 2+1, 1+1, dual or single lane configurations.

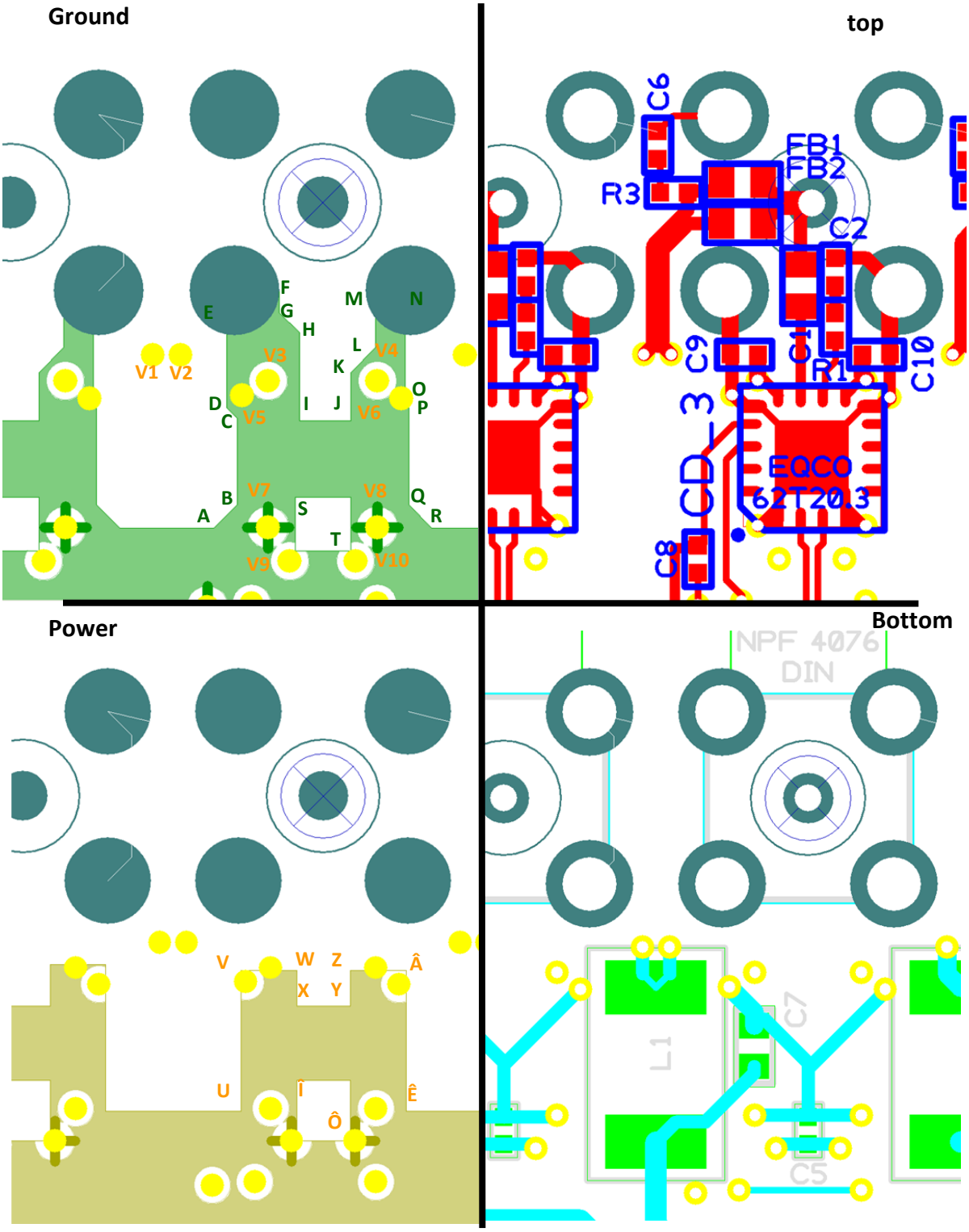

Figure 8: Recommended PCB layout for EQCO62T20.3 with DIN1.0/2.3 connector *with PoCXP*

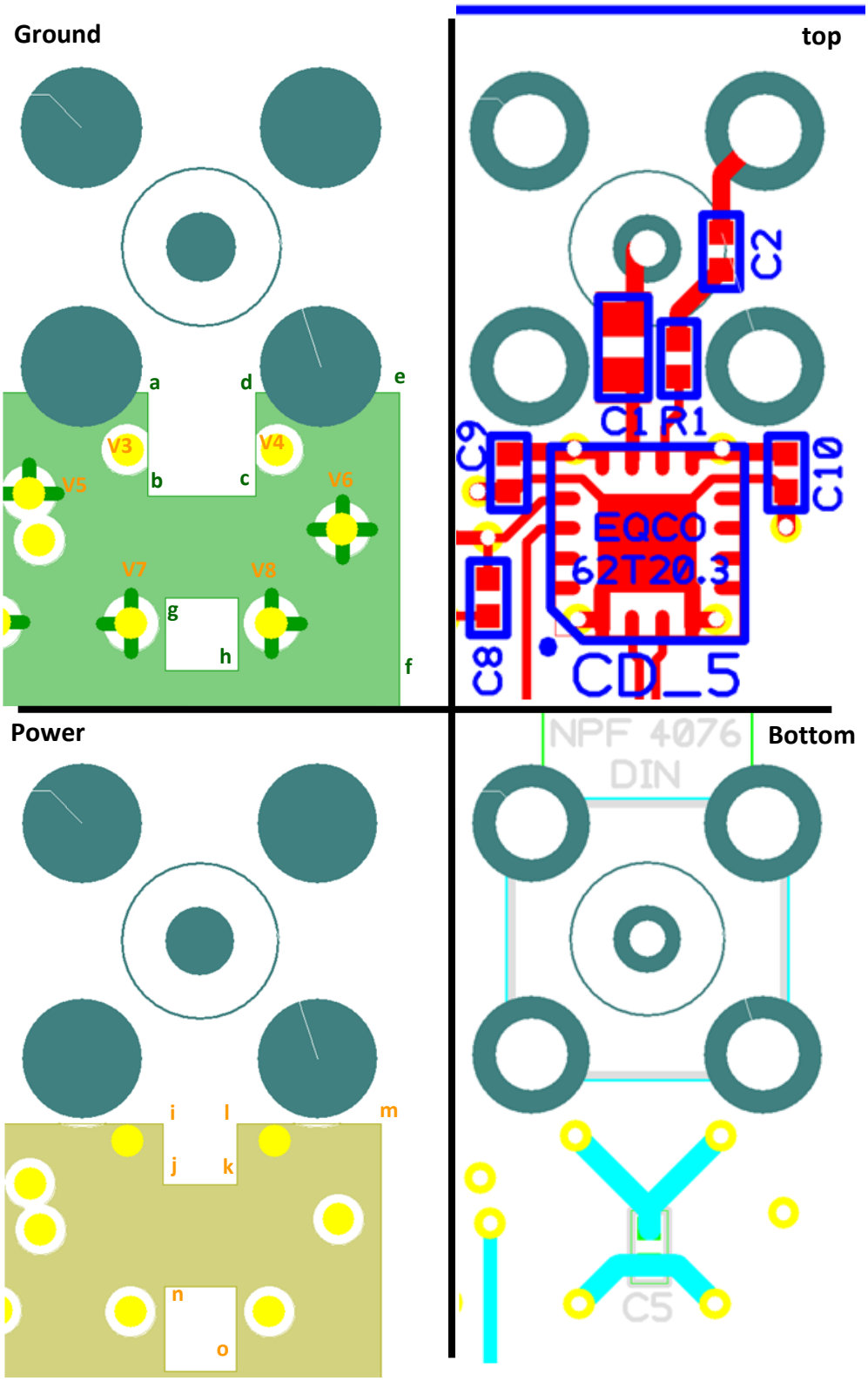

Figure 9: Recommended PCB layout for EQCO62T20.3 with DIN1.0/2.3 connector *without PoCXP*

5.4 Guidelines for Power Receive Unit

At the Power-OUT connection, the voltage supply for the camera (including the power supply for the EQCO62T20.3) is expected.

This load current should have low ripple. High frequency ripple will be rejected by C7/L1/FB1/FB2 filtering in the reference circuit. However, mid frequency ripple is to be avoided by the power supply itself.

In a typical application one could want to step-down from the 24 V supply to all supply voltages needed inside the camera. It is in this case preferred to use a DC-to-DC converter that has a high switching frequency (e.g. 2 MHz) above one that has lower switching frequency (200 kHz). The latter typically induces larger voltage spikes at the Power-OUT connection. These will only be partially filtered out by said filter, the remainder being cross-talk for the uplink channel.

When too much cross-talk remains on the uplink channel, additional power-supply filtering is required. This may be achieved by placing an extra filter network (not shown) in series with the Power-OUT node.

5.5 Power over CoaXPress

The EQCO62T20.3 is compatible with the power over CoaXPress system (PoCXP). Hence power can be switched ON and OFF by the host (e.g. frame grabber) through the 10-µH inductor specified by the CXP standard. This switching is supported through a relay and through an electronic switch.

Powering through a wide-band bias-T is also supported.

The EQCO62T20.3 is also protected against following events:

- Hot plugging by frame grabber: in case the frame grabber has already applied its 24V on the coax when connecting the cable, no damage will occur to the EQCO62T20.3 when connecting the powered coax cable.
- Fast turn-on and turn-off of power supply by frame grabber

Direct 24V application, i.e. not through a 10-µH inductor, is not supported since it causes permanent damage to the EQCO62T20 device.

6 Document Control

6.1 Version History

Version	Date	Author	Comments
1v5	27 Jan 2014	M. Kuijk	Added references
1v4	10 April 2012	X.Maillard	Added Multilane CoaXPress 4+1 layout with DIN1.0/2.3 connectors
1v3	4 Oct 2011	B.Devuyst	Section 5.5 on PoCXP was added.
1v2	29 Sep 2011	B.Devuyst	C1 and C2 in application circuit of Figure 5 have changed to 33 nF
1v1	31 Aug 2011	B.Devuyst	Quality review
1v0	30 Aug 2011	B.Devuyst	New document, taken from EQCO62T20.2 Most important changes with respect to EQCO62T20.2 1) LFsens pin removed 2) Reduced parasitic capacitance at output pin

6.2 References

[1] CoaXPress V1.1 standard. Free download from the JIIA website: http://jiia.org/en/standardization/list/
[2] Patents: US7894515B2 & EP2182688B1
[3] Patents & Patents Pending: EP2247047B1, US20110103267A1, EP12174398.3 & US20110103267A1
[4] Patents & Patents Pending: EP12153028.1, EP2648378A1 & US2013/301483A1

6.3 Disclaimer:

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Appendix 1: Typical Line Driver Characteristics

All measurements at VCC = 1.2 V, Temp = +25 ºC, data pattern = PRBS7, 2x300 mV input amplitude, measured into 75 Ω[3].

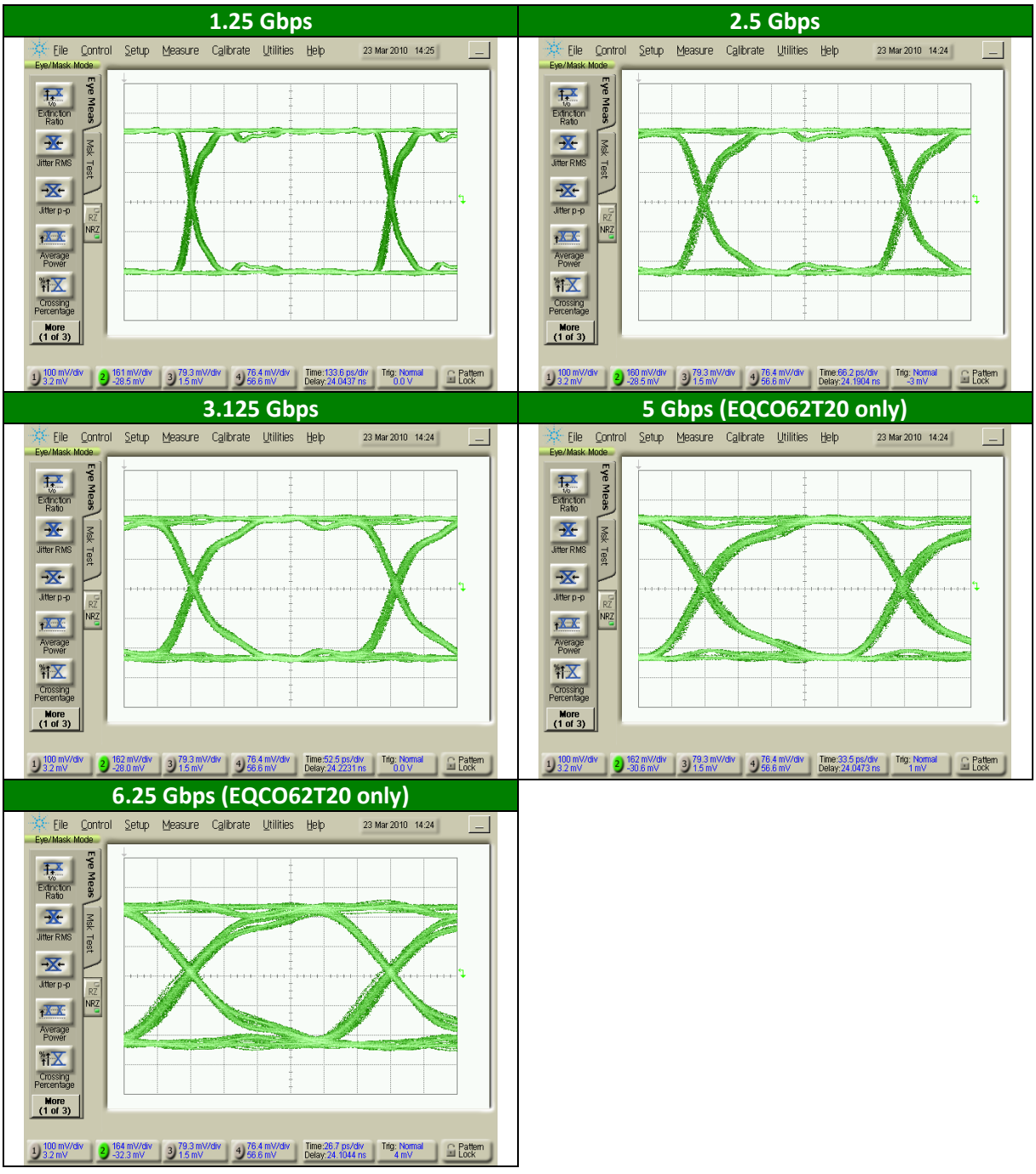

Figure 10: Typical output EYE-diagram of the downlink driver at room temperature for different speeds.

[3] The imperfections in the output eye are caused by the limited bandwidth of the 75 Ω to 50 Ω matching pad that was used in this set-up. The output amplitude is reduced due to this matching pad.

Appendix 2: Typical Uplink Characteristics

All measurements at VCC = 1.2 V, Temp = +25 ºC, data pattern = 8B/10B test pattern at 21 Mbps, 110 mV transmit amplitude. Measurements include power supply transmission; EQCO62T20 is power over the cable. Measured into 15 pF capacitive load.

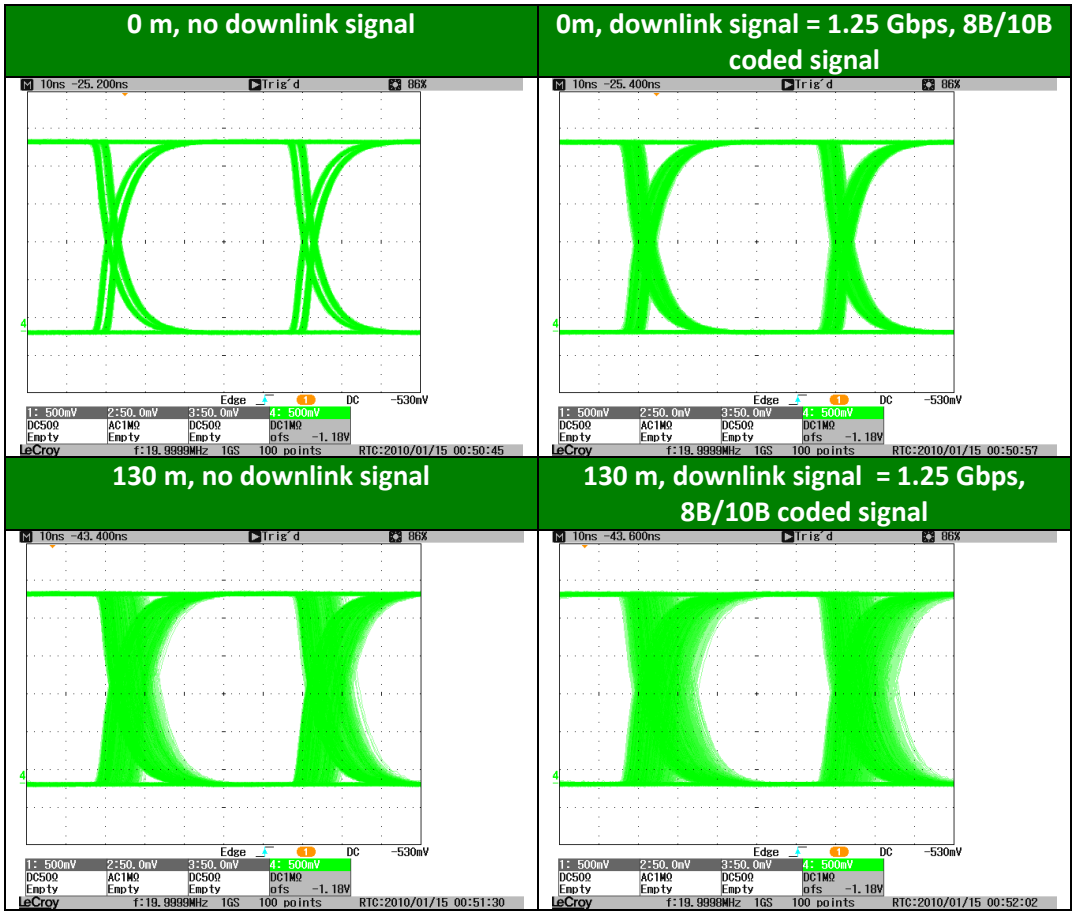

Figure 11: Typical output EYE-diagram of the uplink receiver at room temperature.

Appendix 3: Typical return-loss

Figure 12 shows the return-loss at the BNC connector of the EQCO62T20.3 evaluation board as shown in section 5.1 and 5.3 with supply current of 0 mA and 703 mA (maximum supply current for CoaXPress) through the inductor (L1) and the ferrite beads (Fb1 & Fb2) and compares it with the CoaXPress (Full Speed) return-loss specification.

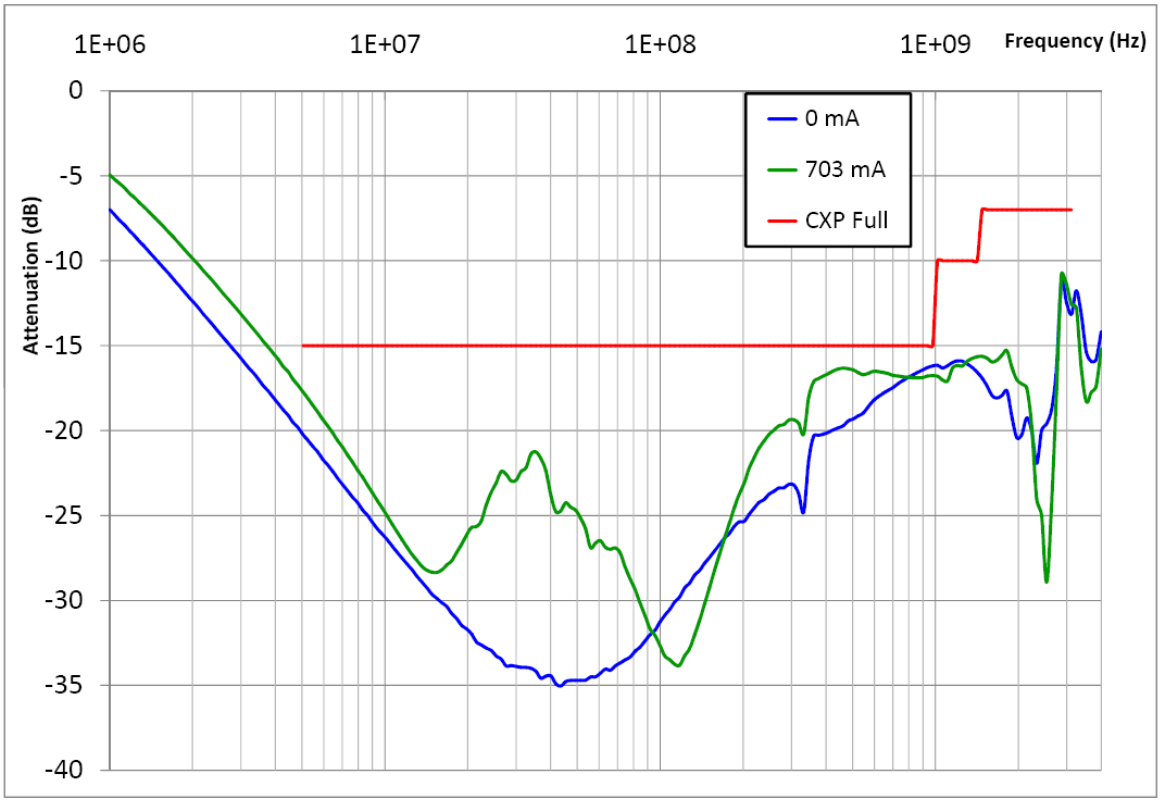

Figure 12 Return-loss of the EQCO62T20.3 BNC evaluation board with and without supply current

Appendix 4: Footprints used for the multilane CoaXPress layout

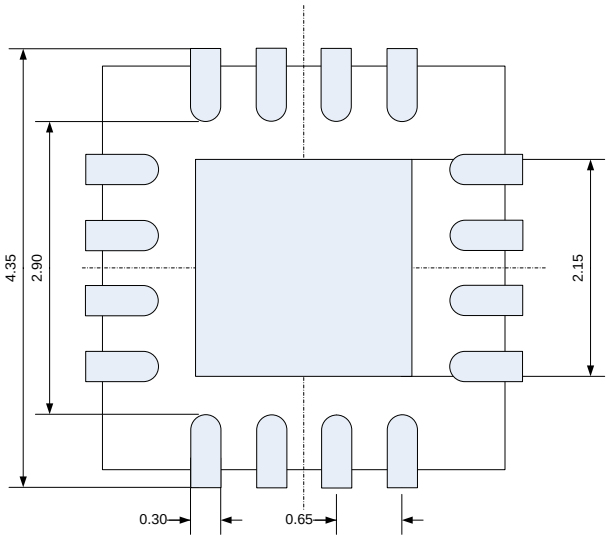

Figure 13: QFN footprint of EQCO62T20.3

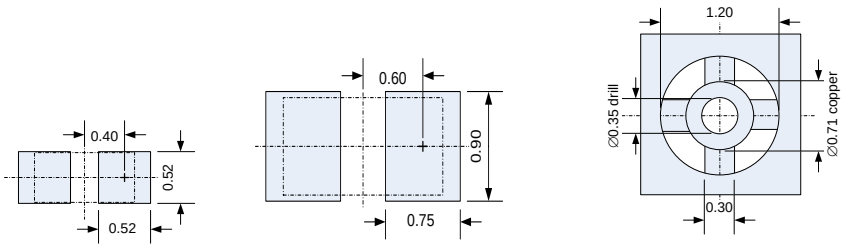

Figure 14: 0402, 0603 and VIA with thermal isolation footprints

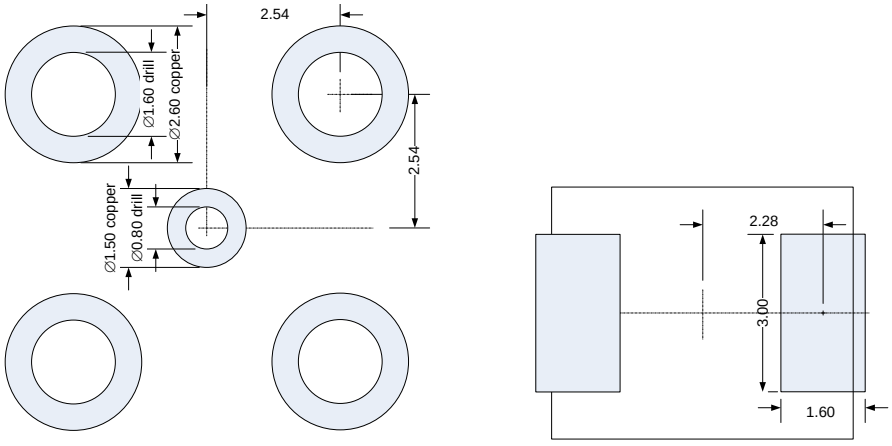

Figure 15: DIN1.0/2.3 and L1 inductor 1812 footprints

Component	Footprint	X	Y	Angle	
NPF 4076	DIN1.0/2.3	0	0		Bottom
EQCO62T20.3	QFN	0	-7.4		
C1 (50 V)	0603	-0.325	-2.4	90°	

Component	Footprint	X	Y	Angle	
C2	0402	0.675	-2	90°	
R1	0402	0.675	-3.6	90°	
FB1	0603	-2.025	0.6		
FB2	0603	-2.025	-0.6		
R3	0402	-4.025	0.3		
C6 (50 V)	0402	-4.5	1.675	90°	
C9	0402	-1.975	-4.4		
C10	0402	1.875	-4.4		
C8	0402	-3.325	-10.35	90°	
L1	1812	-4.5	-7.875	90°	Bottom
C7(50 V)	0603	-1.6	-7.325	90°	Bottom
C5	0402	0	-9.825	90°	Bottom

Table 6 component positions of Figure 8

VIA	Thermal	X	Y	Connected to
1		-4.9	-4.4	Top-bottom
2		-4.1	-4.4	Top-bottom
3	Not isolated	-1.575	-5.15	Top-power
4	Not isolated	1.575	-5.15	Top-power
5	Not isolated	-2.325	-5.575	Top-GND-bottom
6	Not isolated	2.275	-5.65	Top-GND-bottom
7	Isolated	-1.575	-9.375	Top-GND-bottom
8	Isolated	1.575	-9.375	Top-GND-bottom
9	Isolated	-0.95	-10.35	Power-bottom
10	Isolated	0.95	-10.35	Power-bottom

Table 7 via positions of Figure 8

GND plane Coordinates	X	Y	VCC plane Coordinates	X	Y
A	-3.15	-9.4	U	-2.475	-9.45
B	-2.475	-8.725	V	-2.475	-5.225
C	-2.475	-6.225	W	-0.8	-5.225
D	-2.775	-5.925	X	-0.8	-6.3
E	-2.775	-2.525	Y	0.8	-6.3
F	-1.25	-2.525	Z	0.8	-5.225
G	-1.25	-3.175	Â	2.475	-5.225
H	0.675	-3.75	Ê	2.475	-9.45
I	0.675	-6.3			
J	0.8	-6.3			
K	0.8	-4.9			
L	1.525	-4.175			
M	1.525	-2.525			
N	2.375	-2.525			
O	2.375	-5.7			
P	2.475	-5.7			
Q	2.475	-8.725			
R	3.15	-9.4			
S	-0.8	-8.5	Î	-0.8	-8.5
T	0.8	-10.05	Ô	0.8	-10.35

Table 8 Ground and VCC plane position of Figure 8

Track	Width	
1	0.3	QFN.1;QFN.4 (GND)
2	100Ω diff[4].	QFN.2-3 (SDIp-SDIn)
3	0.3	QFN.9;QFN.12 (VCC)
4	0.2	QFN.10 (SDOn)
5	0.3	QFN.11 (SDOp)
6	0.2	QFN.12 (LFVCC)
7	0.2	QFN.13 (LFO)
8	0.4/0.2	QFN.TAB to C9,C10
9	0.5	C9,C10 to DIN1.0/2.3
10	0.5	C9,C10 to V3,4
11	0.4	C1 to DIN1.0/2.3
12	0.4	C2
13	0.4/0.7	FB
14	0.2	C6
15	0.5	Bottom tracks

Table 9 Track dimensions of Figure 8

Component	Footprint	X	Y	Angle	
NPF 4076	DIN1.0/2.3	0	0		Bottom
EQCO62T20.3	QFN	0	-6.375		
C1 (50V)	0603	-0.525	-2.125	90°	
C2	0402	1.6	-0.05	90°	
R1	0402	0.675	-2.375	90°	
C9	0402	-3	-4.85	90°	
C10	0402	3	-4.85	90°	
C8	0402	-3.45	-7.55	90°	
C5	0402	0	-6.775	90°	Bottom

Table 10 component positions of Figure 9

VIA	Thermal	X	Y	Connected to
3	Not isolated	-1.6	-4.325	Top-power
4	Not isolated	1.6	-4.325	Top-power
5	isolated	-3.675	-5.25	Top-GND-bottom
6	isolated	3	-6.025	Top-GND-bottom
7	Isolated	-1.5	-8.025	Top-GND-bottom
8	Isolated	1.5	-8.025	Top-GND-bottom

Table 11 via positions of Figure 9

GND plane Coordinates	X	Y	VCC plane Coordinates	X	Y
a	-1.15	-3.1	h	-1.15	-3.95
b	-1.15	-5.3	i	-1.15	-5.3
c	1.15	-5.3	j	1.15	-5.3
d	1.15	-3.1	k	1.15	-3.95
e	4.225	**-3.1**	l	3.925	-3.95

[4] Width and spaces between lines needs to be calculated based on PCB layer stack. Impedance should be 100Ω differential.

GND plane Coordinates	X	Y	VCC plane Coordinates	X	Y
f	-0.8	-7.475	m	-0.8	-7.475
g	0.8	-9.025	n	0.8	-9.325

Table 12 Ground plane position Figure 9

Track	Width	
1	0.3	QFN.1;QFN.4 (GND)
2	100Ω diff	QFN.2-3 (SDIp-SDIn)
3	0.3	QFN.9;QFN.12 (VCC)
4	0.2	QFN.10 (SDOn)
5	0.3	QFN.11 (SDOp)
6	0.2	QFN.12 (LFVCC)
7	0.2	QFN.13 (LFO)
8	0.2	QFN.TAB to C9,C10
9	0.4	C9,C10 to V3,4
10	0.5	C9,C10 to V5,6
11	0.4	C1 to DIN1.0/2.3
12	0.4	C2
13	0.5	Bottom tracks

Table 13 Track widths of Figure 9

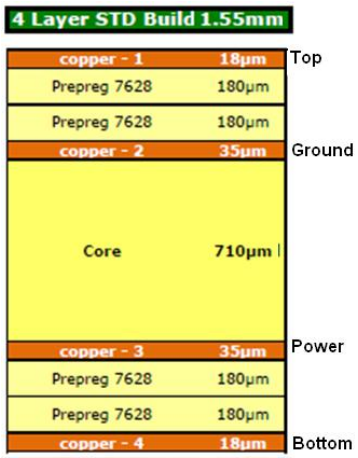

Figure 16: Used layer stack