Product Summary

Device	$V_{(BR)DSS}$	$R_{DS(ON)}$ Max	I_D Max T_C = +25°C (Note 10)
Q1 & Q2	30V	11.1mΩ @ V_{GS} = 10V	30A
		13.8mΩ @ V_{GS} = 4.5V	28A
		22.0mΩ @ V_{GS} = 3.8V	22A

Features and Benefits

- Low Gate Threshold Voltage
- **Totally Lead-Free & Fully RoHS Compliant (Notes 1 & 2)**
- **Halogen and Antimony Free. "Green" Device (Note 3)**

Description

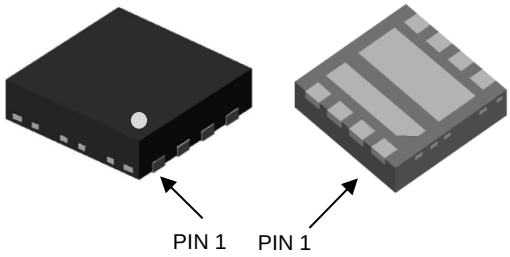
This new generation MOSFET is designed to minimize the on-state resistance ($R_{DS(ON)}$), yet maintain superior switching performance, making it ideal for high-efficiency power management applications.

Applications

- General Purpose Interfacing Switch
- Power Management Functions

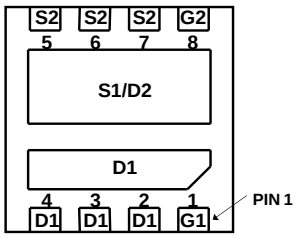
Mechanical Data

- Case: V-DFN3030-8 (Type K)
- Case Material: Molded Plastic, "Green" Molding Compound. UL Flammability Classification Rating 94V-0
- Moisture Sensitivity: Level 1 per J-STD-020
- Terminals: Finish – NiPdAu over Copper Leadframe. Solderable per MIL-STD-202, Method 208 e4
- Weight: 0.02 grams (Approximate)

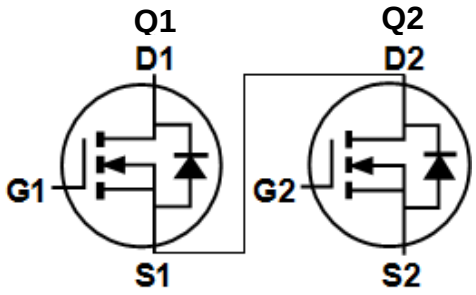


Top View Bottom View

V-DFN3030-8 (Type K)



Bottom View
Internal Schematic



Equivalent Circuit

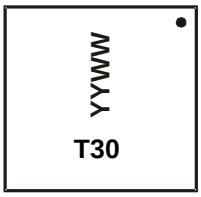
Ordering Information (Note 4)

Part Number	Case	Packaging
DMT3009LDT-7	V-DFN3030-8 (Type K)	3,000/Tape & Reel

Notes:
1. No purposely added lead. Fully EU Directive 2002/95/EC (RoHS) & 2011/65/EU (RoHS 2) compliant.
2. See http://www.diodes.com/quality/lead_free.html for more information about Diodes Incorporated's definitions of Halogen- and Antimony-free, "Green" and Lead-free.
3. Halogen- and Antimony-free "Green" products are defined as those which contain <900ppm bromine, <900ppm chlorine (<1500ppm total Br + Cl) and <1000ppm antimony compounds.
4. For packaging details, go to our website at http://www.diodes.com/products/packages.html.

Marking Information

V-DFN3030-8 (Type K)



T30= Product Type Marking Code
YYWW = Date Code Marking
YY = Last Two Digits of Year (ex: 16 = 2016)
WW = Week Code (01 to 53)

Maximum Ratings (@T_A = +25°C, unless otherwise specified.)

Characteristic			Symbol	Q1&Q2	Unit
Drain-Source Voltage			V_{DSS}	30	V
Gate-Source Voltage			V_{GSS}	+20, -16	V
Continuous Drain Current (Note 6) V_{GS} = 10V	Steady State (Note 10)	T_C = +25°C T_C = +70°C	I_D	30 25	A
	t<10s	T_A = +25°C T_A = +70°C	I_D	14 11	A
Maximum Body Diode Forward Current (Note 6)			I_S	2.1	A
Pulsed Drain Current (100µs Pulse, Duty Cycle = 1%)			I_{DM}	100	A
Avalanche Current (Note 7) L = 0.1mH			I_{AS}	19.3	A
Avalanche Energy (Note 7) L = 0.1mH			E_{AS}	18.6	mJ

Thermal Characteristics

Characteristic		Symbol	Value	Unit
Total Power Dissipation (Note 5)	T_A = +25°C	P_D	1.2	W
	T_A = +70°C		0.8	
Thermal Resistance, Junction to Ambient (Note 5)	Steady State	$R_{\theta JA}$	107	°C/W
	t<10s		63	
Total Power Dissipation (Note 6)	T_A = +25°C	P_D	2.0	W
	T_A = +70°C		1.2	
Thermal Resistance, Junction to Ambient (Note 6)	Steady State	$R_{\theta JA}$	64	°C/W
	t<10s		39	
Thermal Resistance, Junction to Case (Note 6)		$R_{\theta JC}$	7.6	
Operating and Storage Temperature Range		T_J, T_{STG}	-55 to +150	°C

Notes: 5. Device mounted on FR-4 substrate PC board, 2oz copper, with minimum recommended pad layout.
6. Device mounted on FR-4 substrate PC board, 2oz copper, with 1-inch square copper plate.
7. UIS in production with L = 0.1mH, starting T_A = +25°C.

Electrical Characteristics (@T_A = +25°C, unless otherwise specified.)

Characteristic	Symbol	Min	Typ	Max	Unit	Test Condition
OFF CHARACTERISTICS (Note 8)						
Drain-Source Breakdown Voltage	BV_{DSS}	30	—	—	V	V_{GS} = 0V, I_D = 250µA
Zero Gate Voltage Drain Current	I_{DSS}	—	—	1	µA	V_{DS} = 24V, V_{GS} = 0V
Zero Gate Voltage Drain Current T_J = +150°C (Note 9)	I_{DSS}	—	—	100	µA	V_{DS} = 24V, V_{GS} = 0V
Gate-Source Leakage	I_{GSS}	—	—	±100	nA	V_{GS} = 20V, V_{DS} = 0V V_{GS} =-16V, V_{DS} = 0V
ON CHARACTERISTICS (Note 8)						
Gate Threshold Voltage	$V_{GS(TH)}$	1	—	3	V	V_{DS} = V_{GS}, I_D = 250µA
Static Drain-Source On-Resistance	$R_{DS(ON)}$	—	7.2	11.1	mΩ	V_{GS} = 10V, I_D = 14.4A
		—	10.5	13.8		V_{GS} = 4.5V, I_D = 7A
		—	13	22.0		V_{GS} = 3.8V, I_D = 5A
Diode Forward Voltage	V_{SD}	—	—	1.2	V	V_{GS} = 0V, I_S = 10A
DYNAMIC CHARACTERISTICS (Note 9)						
Input Capacitance	C_{ISS}	—	748	1,500	pF	V_{DS} = 15V, V_{GS} = 0V, f = 1.0MHz
Output Capacitance	C_{OSS}	—	447	895		
Reverse Transfer Capacitance	C_{RSS}	—	43	90		
Gate Resistance	R_G	—	1.0	2.0	Ω	V_{DS} = 0V, V_{GS} = 0V, f = 1.0MHz
Total Gate Charge (V_{GS} = 10V)	Q_G	—	13.8	20	nC	V_{DS} = 15V, I_D = 14.4A
Total Gate Charge (V_{GS} = 4.5V)	Q_G	—	6.4	9		
Gate-Source Charge	Q_{GS}	—	2.2	5		
Gate-Drain Charge	Q_{GD}	—	2.2	5		
Turn-On Delay Time	$t_{D(ON)}$	—	3.5	7	ns	V_{GS} = 10V, V_{DD} = 15V, R_G = 1Ω, I_D = 10A
Turn-On Rise Time	t_R	—	5.0	10		
Turn-Off Delay Time	$t_{D(OFF)}$	—	8.6	17		
Turn-Off Fall Time	t_F	—	1.4	3		
Body Diode Reverse Recovery Time	t_{RR}	—	18	33	ns	I_F = 10A, di/dt = 100A/µs
Body Diode Reverse Recovery Charge	Q_{RR}	—	7.7	15	nC	I_F = 10A, di/dt = 100A/µs

Notes: 8. Short duration pulse test used to minimize self-heating effect.
9. Guaranteed by design. Not subject to product testing.
10. Package limited.

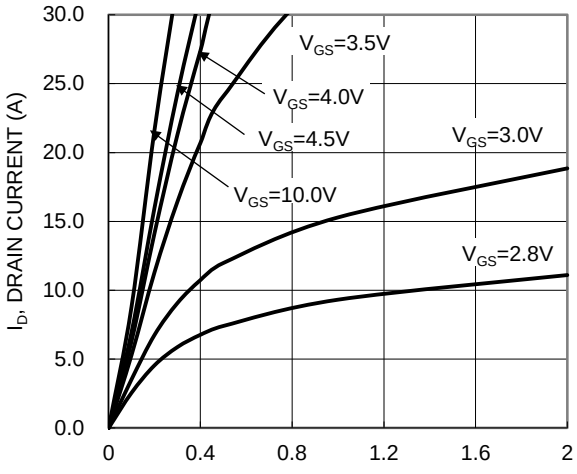


Figure 1. Typical Output Characteristic

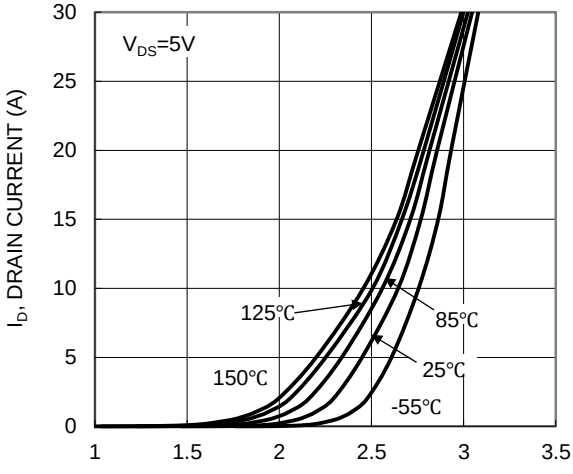


Figure 2. Typical Transfer Characteristic

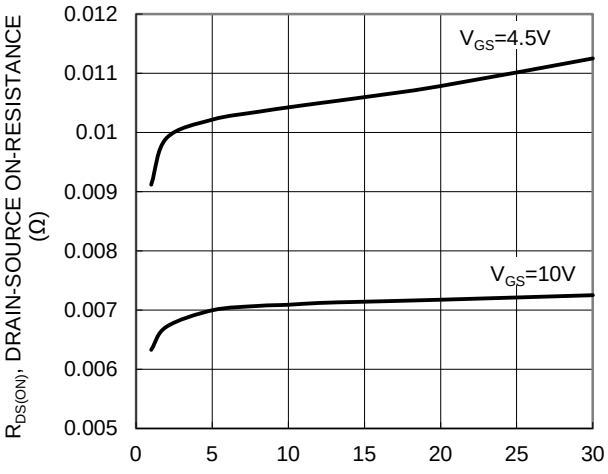


Figure 3. Typical On-Resistance vs Drain Current and Gate Voltage

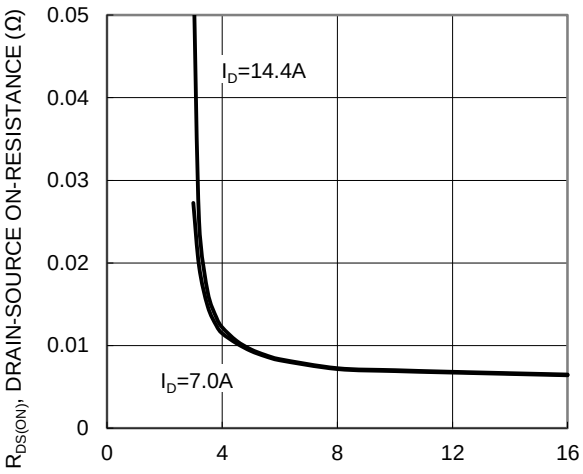


Figure 4. Typical Transfer Characteristic

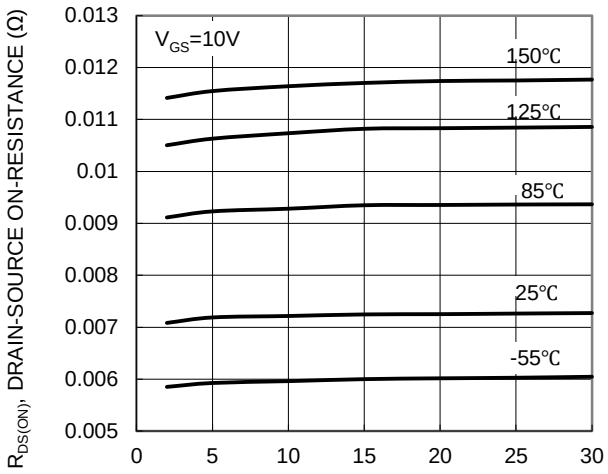


Figure 5. Typical On-Resistance vs. Drain Current and Junction Temperature

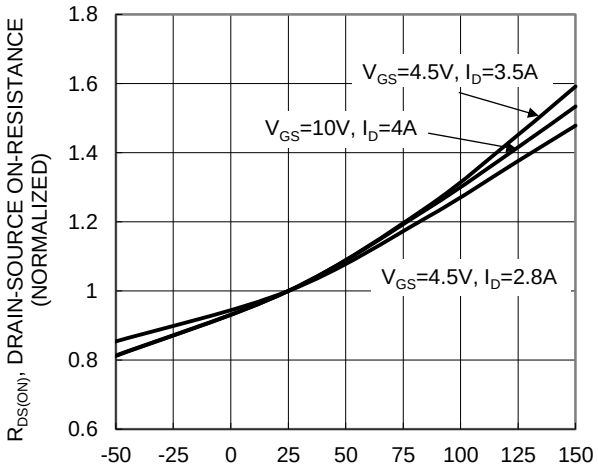


Figure 6. On-Resistance Variation with Junction Temperature

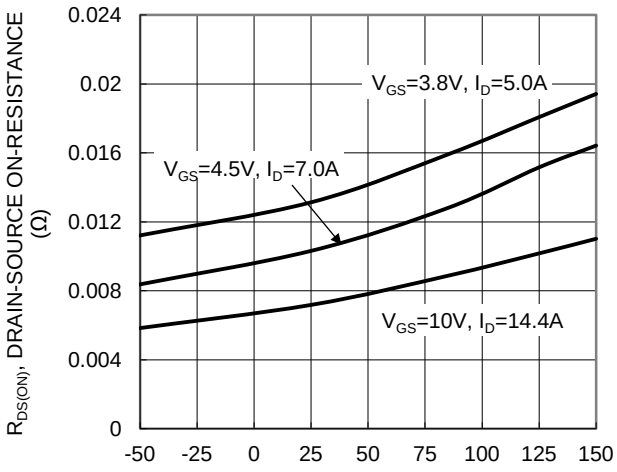


Figure 7. On-Resistance Variation with Junction Temperature

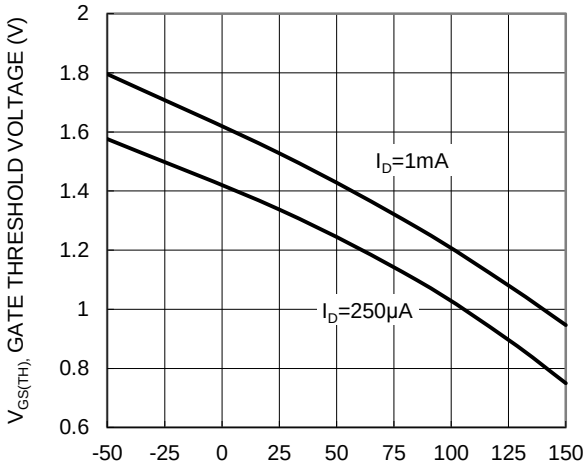


Figure 8. Gate Threshold Variation vs. Junction Temperature

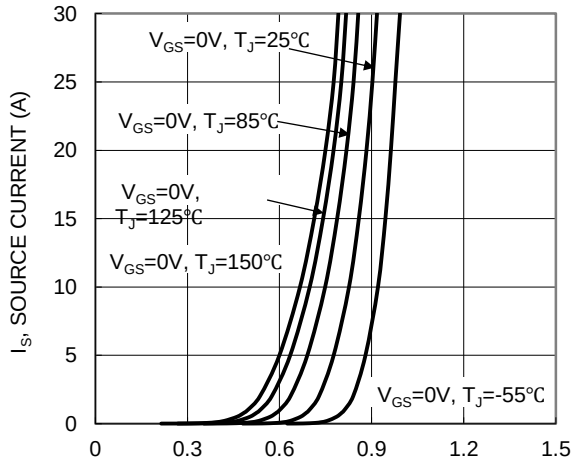


Figure 9. Diode Forward Voltage vs. Current

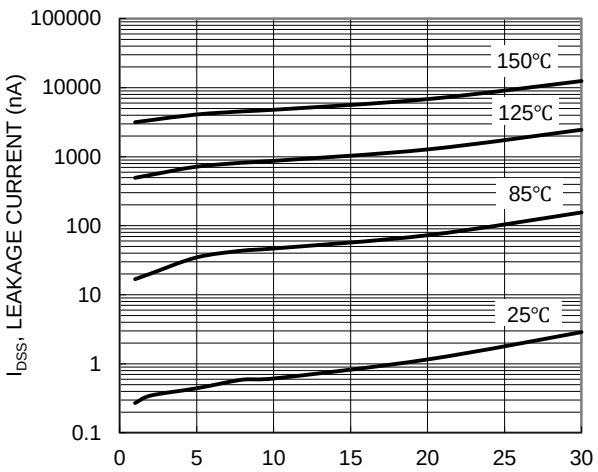


Figure 10. Typical Drain-Source Leakage Current vs. Voltage

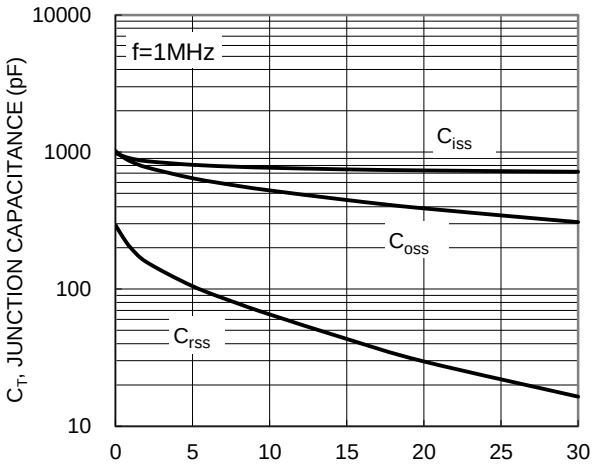


Figure 11. Typical Junction Capacitance

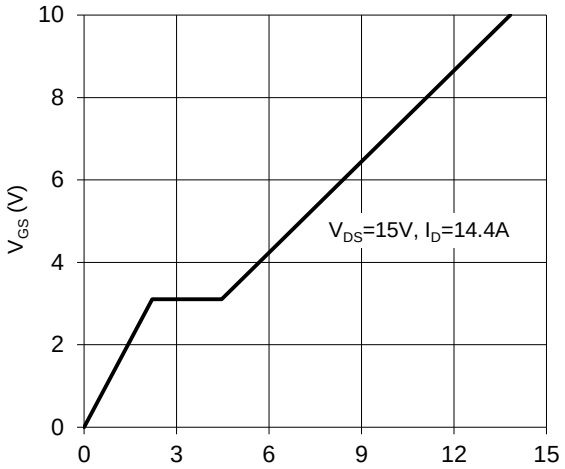


Figure 12. Gate Charge

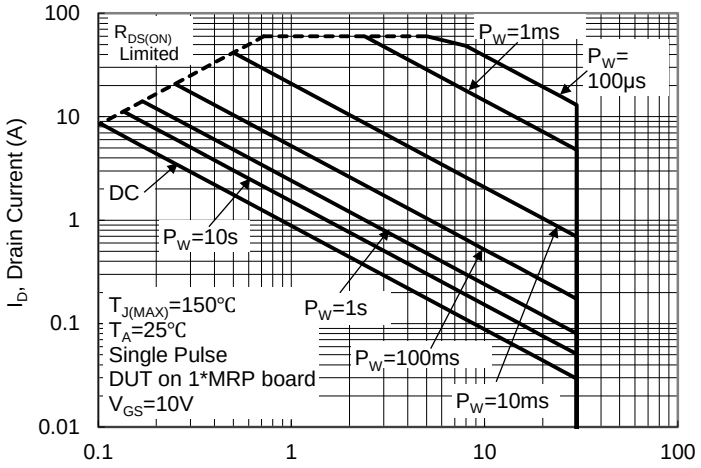


Figure 13. SOA, Safe Operation Area

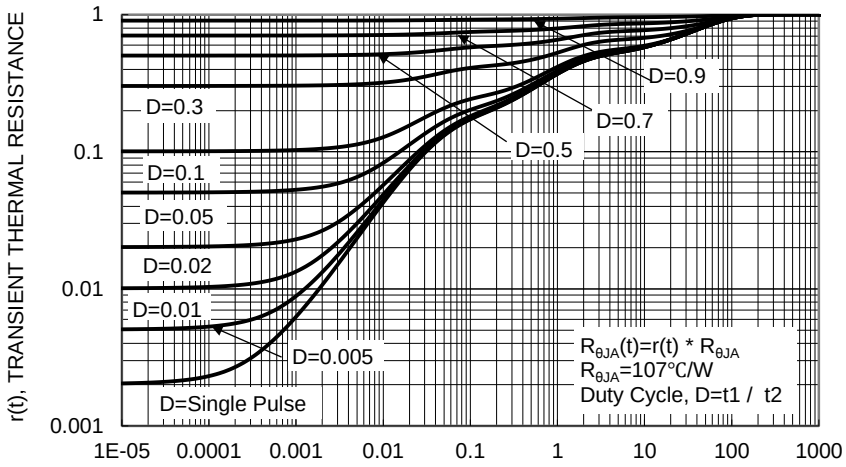
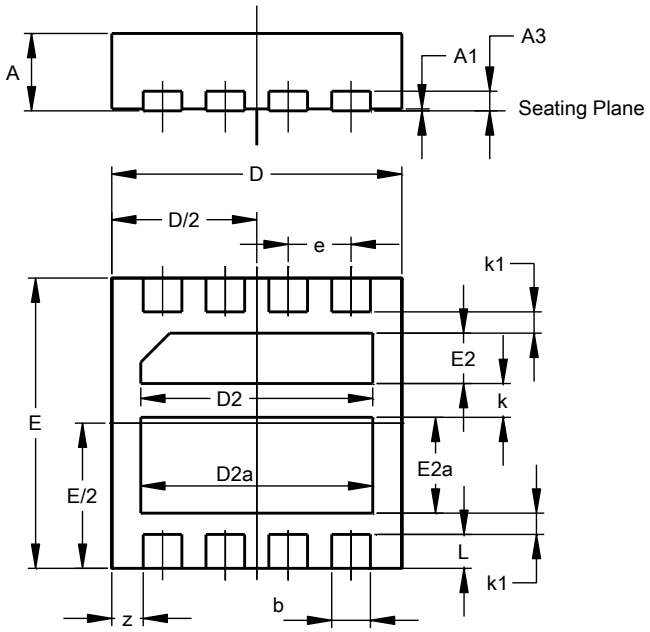


Figure 14. Transient Thermal Resistance

Package Outline Dimensions

Please see http://www.diodes.com/package-outlines.html for the latest version.

V-DFN3030-8 (Type K)

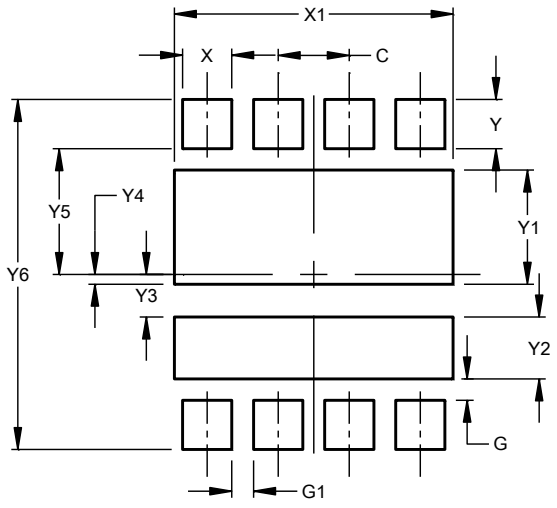


V-DFN3030-8 (Type K)			
Dim	**Min**	**Max**	**Typ**
A	0.77	0.85	0.80
A1	0.00	0.05	0.02
A3	0.20BSC		
b	0.35	0.45	0.40
D	2.95	3.050	3.00
D2	2.30	2.50	2.40
D2a	2.30	2.50	2.40
E	2.95	3.050	3.00
E2	0.42	0.62	0.52
E2a	0.89	1.09	0.99
e	0.65BSC		
k	-	-	0.35
k1	-	-	0.22
L	0.30	0.40	0.35
z	0.325BSC		
All Dimensions in mm			

Suggested Pad Layout

Please see http://www.diodes.com/package-outlines.html for the latest version.

V-DFN3030-8 (Type K)



Dimensions	Value (in mm)
C	0.650
G	0.195
G1	0.200
X	0.450
X1	2.550
Y	0.450
Y1	1.044
Y2	0.566
Y3	0.389
Y4	0.089
Y5	1.150
Y6	3.200

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