Evaluation Board for the Dual High Speed PECL Comparators

EVAL-ADCMP551/552/561/562/563/564

GENERAL DESCRIPTION

This document provides an overview of the evaluation board for the ADCMP551/ADCMP552 and ADCMP561/ADCMP562/ADCMP563/ADCMP564 comparator products that are available in either a 16-lead or 20-lead QSOP. The evaluation board provides an environment for engineers to make their own measurements. These products are released to production, and data sheets are available at www.analog.com.

EVALUATION BOARD DESCRIPTION

Figure 1 is a photograph of the evaluation board. The evaluation board provides access to all of the comparator inputs, outputs, and latches through the SMA connectors. All of the A-side comparator inputs and outputs are located on the COMP A portion of the board. The B-side comparator inputs and outputs are located on the COMP B portion of the board. The power for the comparators is brought in through the banana jacks on the left side of the evaluation board. Pin 1 of the 20-lead QSOP comparators is located next to the white dot. The 16-lead QSOP comparators are offset by one pin; therefore, Pin 1 is located on the 20-lead QSOP Pin 2 pad.

PACKAGE LIST

- Evaluation board with component installed
- Schematic

EVALUATION BOARD

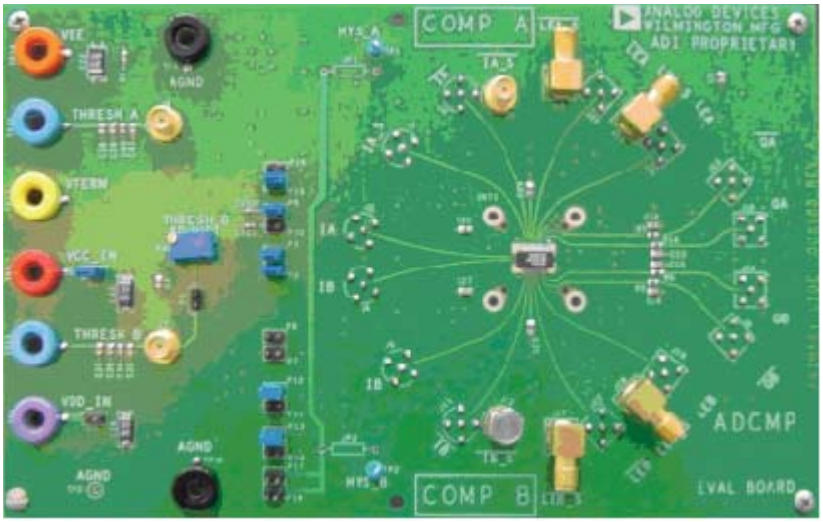

Figure 1. Evaluation Board Top Side Photo

Rev. 0

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REVISION HISTORY

1/06—Revision 0: Initial Version

USING THE EVALUATION BOARD

POWER

Six banana jacks on the evaluation board provide power for the part. V_{EE} is brought onto the board through the orange jack labeled VEE (TP14). V_{EE} is −5.2 V and is necessary for the ADCMP561/ADCMP562/ADCMP563/ADCMP564. V_{CC} is brought onto the board through the red jack labeled VCC_IN (TP5). V_{CC} is +5.0 V for the ADCMP561/ADCMP562/ ADCMP563/ADCMP564 and can be programmed from +3.3 V to +5.0 V (VCCI) for the ADCMP551/ADCMP552. V_{DD} is brought onto the board through the purple jack labeled VDD_IN (TP6). V_{DD} can be programmed from +2.5 V to +5.0 V for the ADCMP561/ADCMP562 and from +3.3 V to +5.0 V for the ADCMP551/ADCMP552.

VTERM is brought onto the board through the yellow jack (TP13). VTERM provides the termination voltage for the comparator outputs ECL or PECL. For the ADCMP563/ ADCMP564, the VTERM voltage is −4 V. For the ADCMP551/ ADCMP552 and ADCMP561/ADCMP562, the VTERM voltage is 2 × (VDD_IN − 2.0 V). The comparator output termination scheme on the evaluation board requires the termination voltage to be a factor of 2; this is explained in more detail in the Outputs section. The two black banana jacks, labeled AGND, provide the ground voltage for the board.

Table 1. Comparator Power Supply Voltages

	ADCMP551/ADCMP552	ADCMP561/ADCMP562	ADCMP563/ADCMP564
VCC_IN (red)	+3.3 V to +5.0 V	+5.0 V	+5.0 V
VEE (orange)	N/C	−5.2 V	−5.2 V
VDD_IN (purple)	+3.3 V to +5.0 V	+2.5 V to +5.0 V	N/C
VTERM (yellow)	2 × (VDD_IN − 2.0 V)	2 × (VDD_IN − 2.0 V)	−4.0 V

EVALUATION BOARD HARDWARE

DC THRESHOLDS

If the comparator is operated in single-ended mode, dc threshold inputs are made available through the THRESH A and THRESH B blue banana jacks. A dc voltage threshold is applied to the appropriate jack, filtered by the on-board capacitors, and made available on an SMA connector. The SMA connector can then be connected with a short cable to the desired input pin of the comparator. This option allows the board to maintain a clean 50 Ω environment on every comparator input.

The THRESH B SMA contains a connection to the THRESH B ADJUST, which is a potentiometer connected between VCC and VEE. With Jumper P5 installed, the THRESH B ADJUST can be used to program a desired threshold voltage on the THRESH B SMA. This allows for fewer supply voltages.

A dc threshold can also be applied directly to the comparator input through a coaxial cable.

INPUTS

The comparator inputs −INA, +INA, −INB, and +INB are accessed on the evaluation board through SMA connectors. Figure 2 shows the relationship between the SMA connectors and the comparator inputs. The input path for each comparator input pin is a 50 Ω trace that flies by the input pin and can be sampled on an SMA connector marked with an *_S for sample. The fly-by allows the user to monitor the signal that is applied to the comparator. If the fly-by path is not used, the proper termination for the incoming input signal should be installed. In most ac cases, this is a 50 Ω to GND connector; in dc cases, it should be left open.

Table 2. SMA Input Connections

Pin	SMA Input	SMA Fly-By
+INA	IA	IA_S
−INA	$\overline{\text{IA}}$	$\overline{\text{IA\_S}}$
+INB	IB	IB_S
−INB	$\overline{\text{IB}}$	$\overline{\text{IB\_S}}$

OUTPUTS

The comparator outputs QA, $\overline{\text{QA}}$, QB, and $\overline{\text{QB}}$ are made available on their respectively named SMA connectors. There is a resistor divider network in the output path that enables the outputs to be terminated 50 Ω to GND. The resistor network is shown in Figure 2.

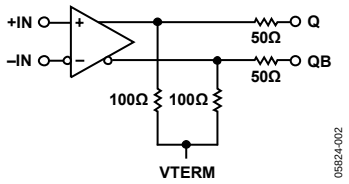

Figure 2. Evaluation Board Output Termination Scheme

The parallel combination of the resistors, when the output is terminated 50 Ω to GND, is equal to 50 Ω. The termination voltage is cut in half with this configuration, which is why it is doubled to maintain proper termination for an ECL or PECL output stage. The outputs can be connected directly to an oscilloscope that has a 50 Ω to GND termination. While this is convenient for measurements, it is also necessary to realize that the output levels are cut in half with this method.

LATCHES

The latch inputs on the evaluation board are set up in a similar method as the inputs. The latch inputs are accessed through the appropriately named SMA connectors. The corresponding fly-by SMA connectors are labeled with *_S. The latches can be driven with an ac source or left open. If the latches are left open, then the comparator defaults to the compare mode where the output tracks the input.

PROGRAMMABLE HYSTERESIS

If the comparator has programmable hysteresis, then it can be accessed through the HYS_A (TP1) and HYS_B (TP2) pins. A test point is available at these pins to connect a current source that can be used to drive the comparator's programmable hysteresis in accordance with the comparator's data sheet. The JP1 and JP2 spaces on the evaluation board allow users to apply an appropriately valued resistor to the hysteresis pin if they would prefer to use the resistance curve for hysteresis.

JUMPERS

The evaluation board is developed to enable the evaluation of six different comparators, the ADCMP551/ADCMP552 and the ADCMP561/ADCMP562/ADCMP563/ADCMP564. To accomplish this, there is a row of jumpers on the evaluation board that, when properly connected, route the correct power to each comparator product. When a comparator is mounted onto the board, the jumpers are set accordingly for that product. In most cases, the user does not have to adjust the jumpers. If the user has decided to use the evaluation board for a comparator product other than the one that was mounted on the board when first shipped, the jumpers should be removed and reinstalled. Table 3 gives the correct jumper settings for each of the comparator products.

Table 3. Jumper Connections

Jumper Number	ADCMP551/ ADCMP552	ADCMP561/ ADCMP562	ADCMP563/ ADCMP564
P2	Open	Open	Short
P3	Open	Open	Short
P4	Short	Short	Short
P6	Short	Short	Open
P7	Open	Open	Open
P8	Open	Open	Open
P9	Open	Short	Short
P10	Short	Open	Open
P11	Short	Open	Open
P12	Open	Short	Short
P13	Open	Short	Short
P14	Short	Open	Open
P15	Open	Open	Short
P16	Short	Short	Open
P17	Short	Open	Open
P18	Open	Short	Short

EVALUATION BOARD LAYOUT

SCHEMATICS

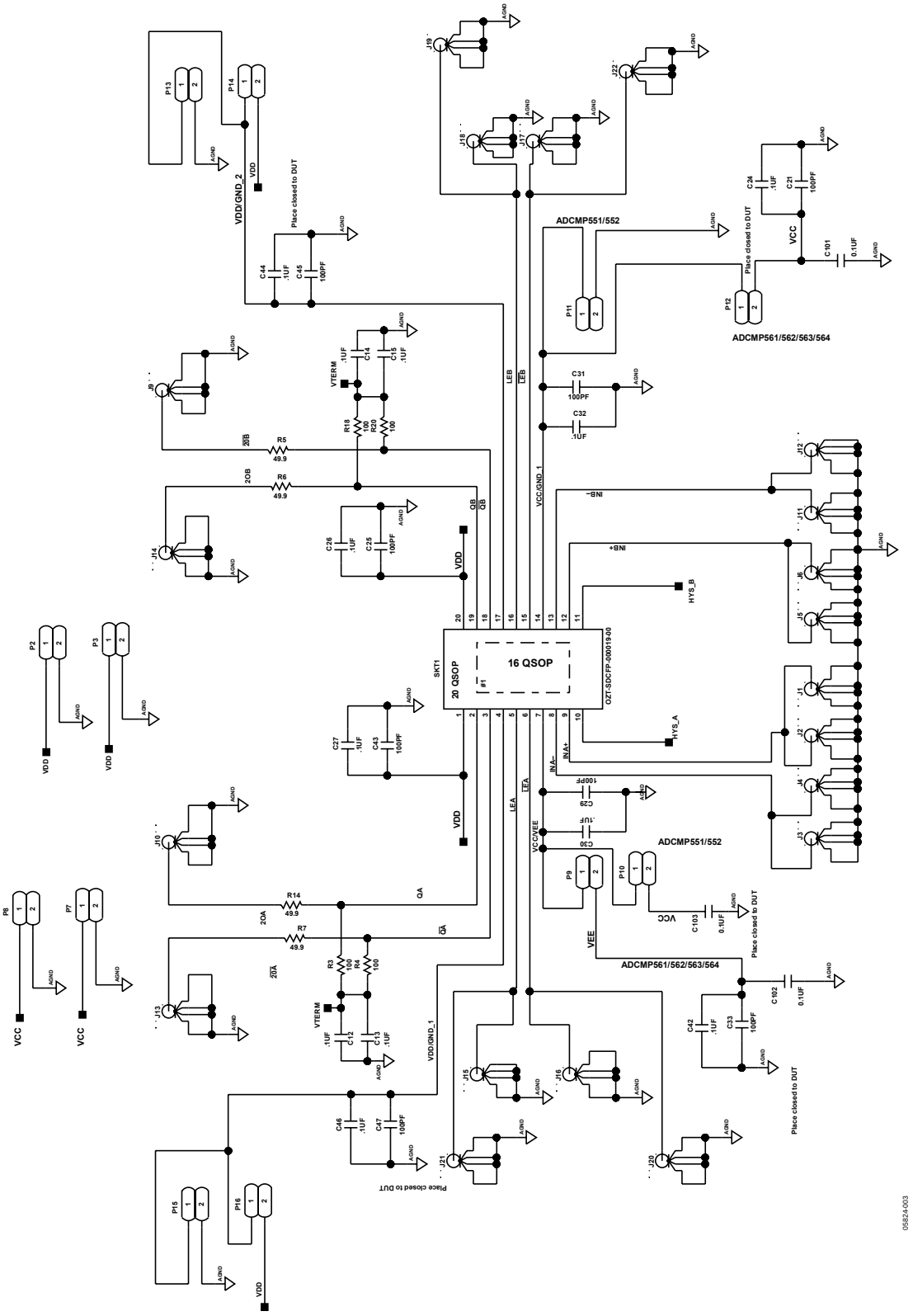

Figure 3. Evaluation Board Signal Schematic

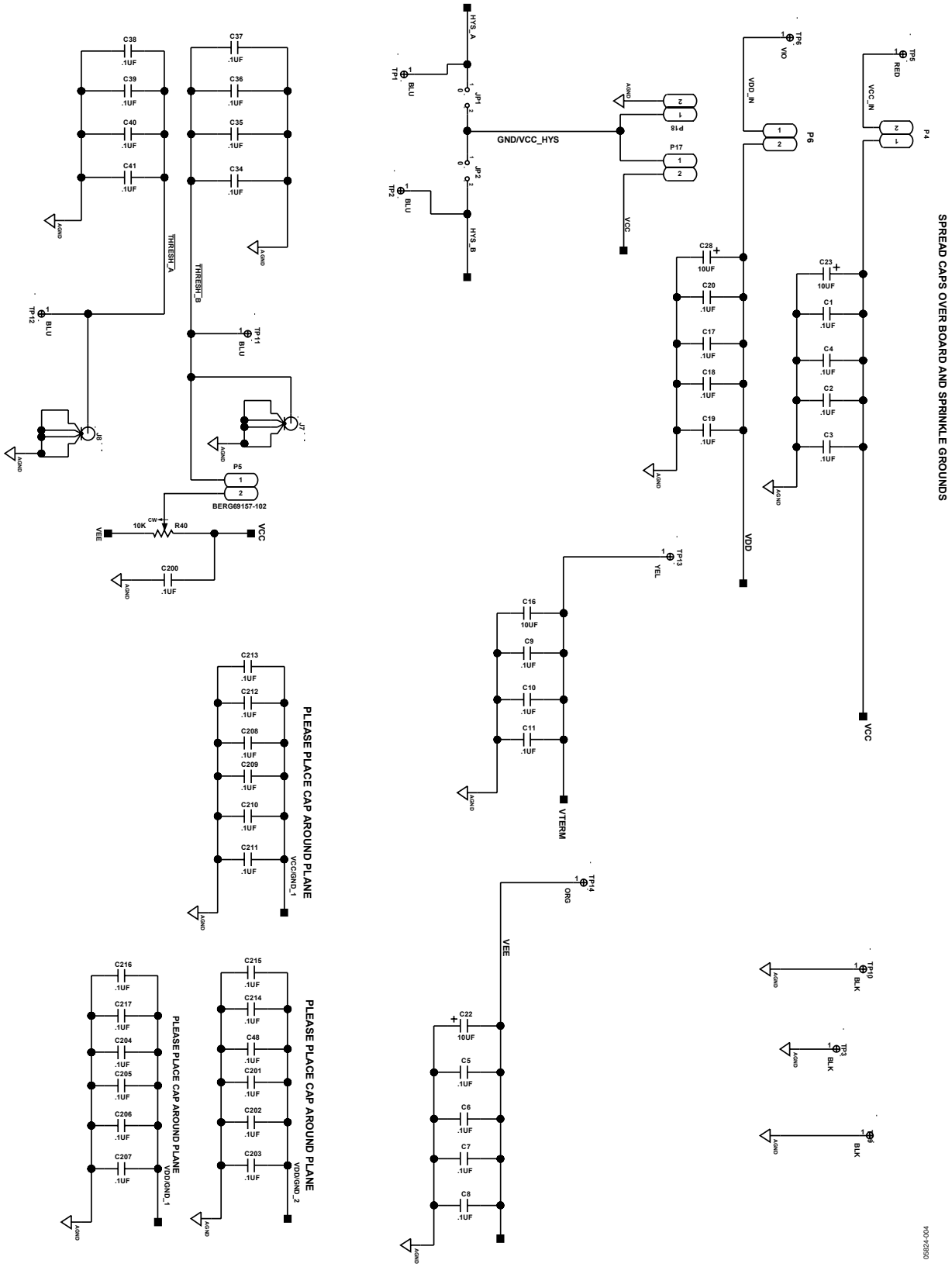

Figure 4. Evaluation Board Power Distribution and Bypassing

LAYERS

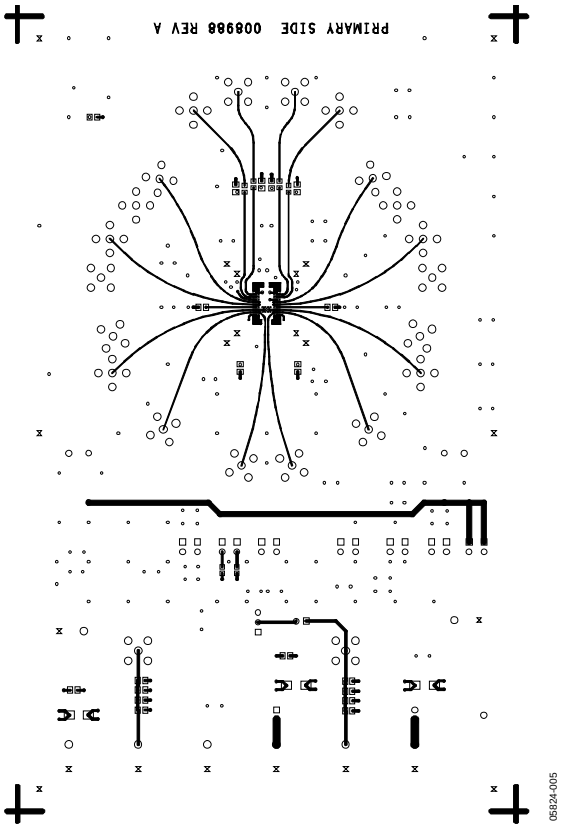

Figure 5. Top Signal Layer

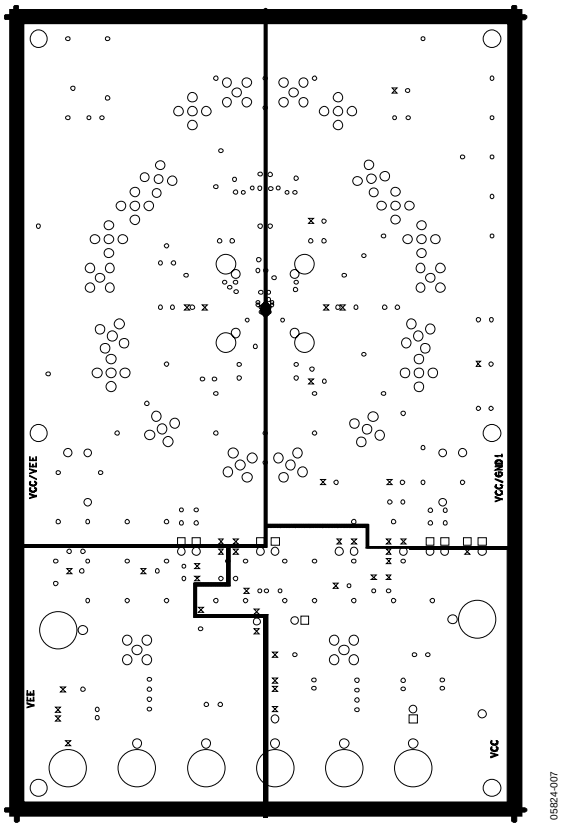

Figure 6. Buried Planes 1

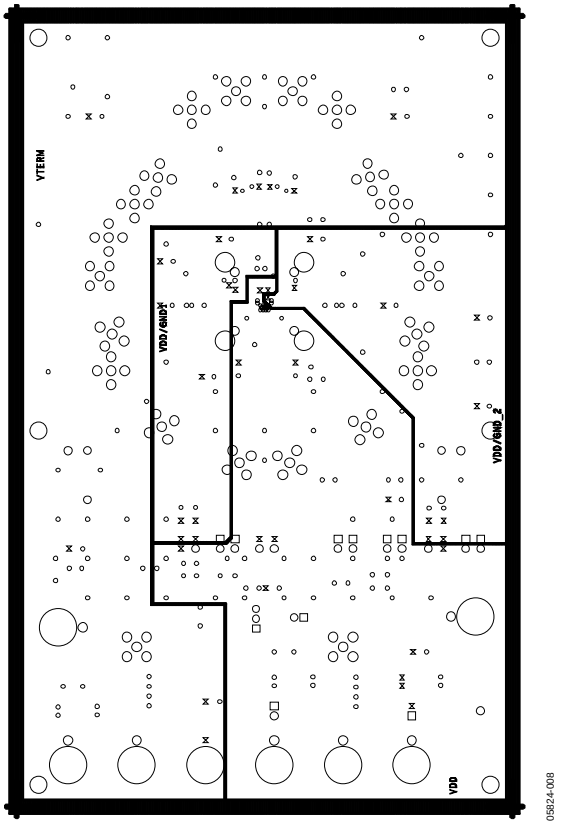

Figure 7. Buried Planes 2

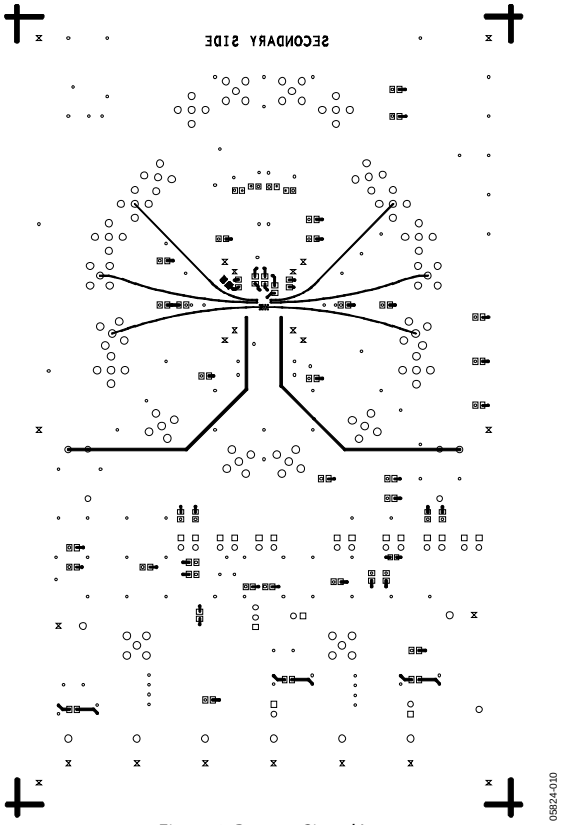

Figure 8. Bottom Signal Layer

SILKSCREENS

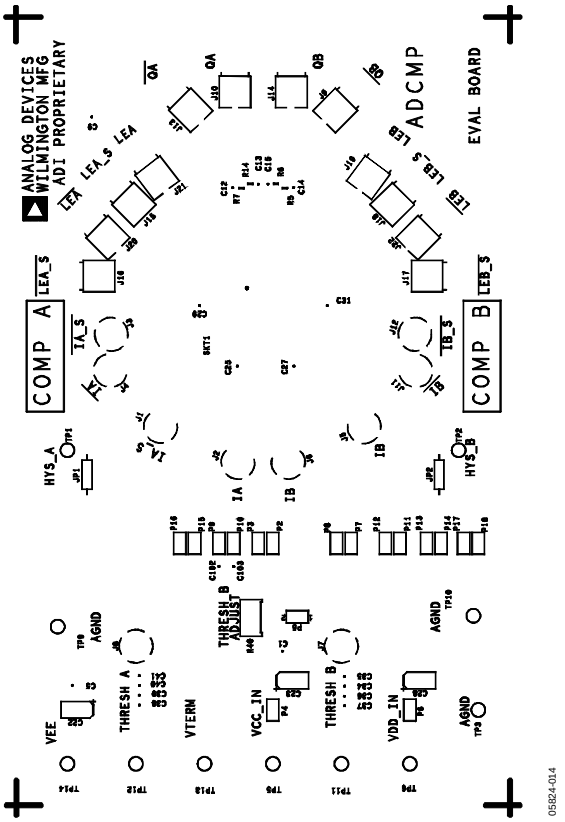

Figure 9. Top Silkscreen

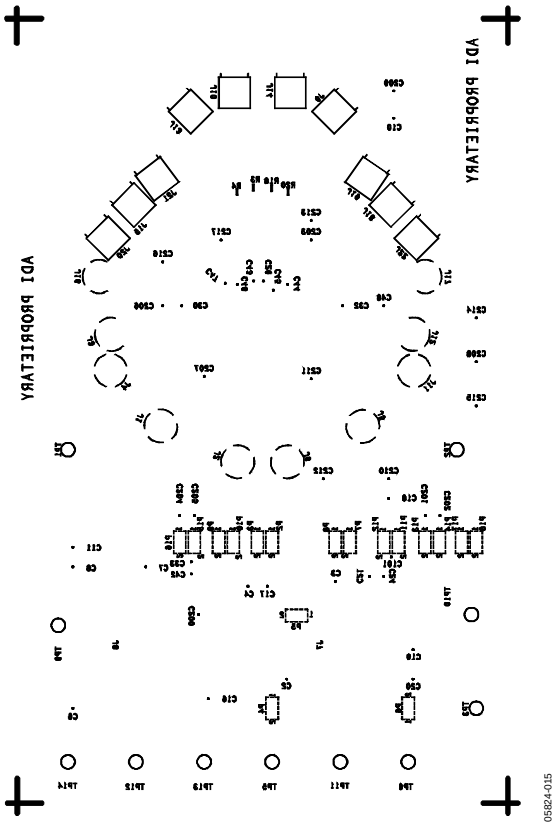

Figure 10. Bottom Silkscreen

COMPONENTS

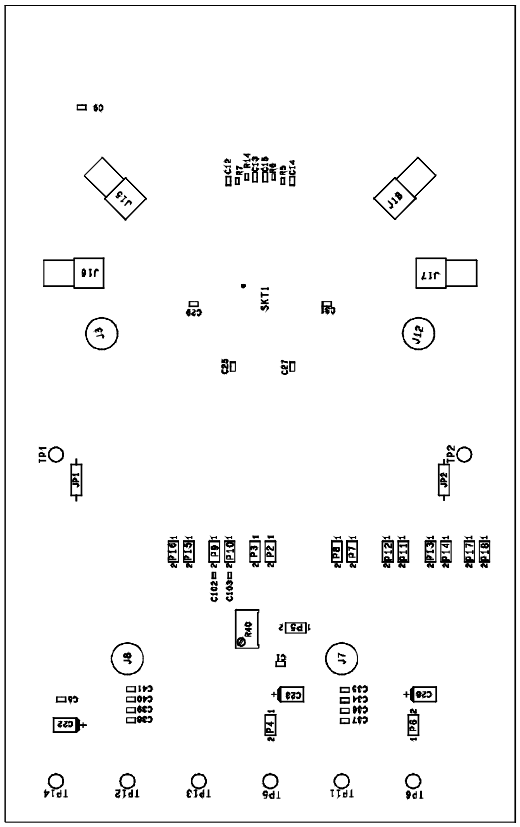

Figure 11. Top Side Components

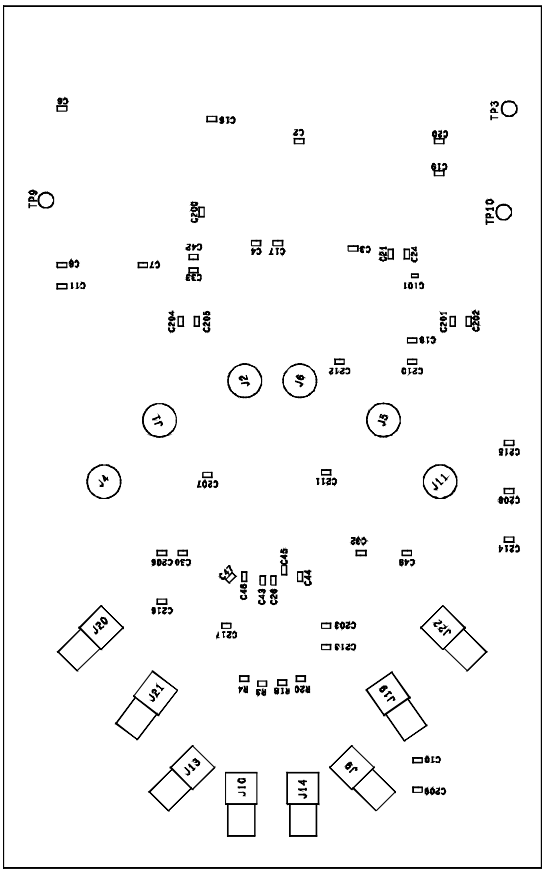

Figure 12. Bottom Side Components

ORDERING INFORMATION

ORDERING GUIDE

Model	Description
EVAL-ADCMP551BRQ	Evaluation Board
EVAL-ADCMP552BRQ	Evaluation Board
EVAL-ADCMP561BRQ	Evaluation Board
EVAL-ADCMP562BRQ	Evaluation Board
EVAL-ADCMP563BRQ	Evaluation Board
EVAL-ADCMP564BRQ	Evaluation Board

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although this product features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

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ANALOG DEVICES

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