

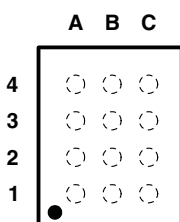
# 4-BIT BIDIRECTIONAL VOLTAGE-LEVEL TRANSLATOR WITH AUTOMATIC DIRECTION SENSING AND $\pm 15$ -kV ESD PROTECTION

Check for Samples: [TXB0104](#)

## FEATURES

- 1.2 V to 3.6 V on A Port and 1.65 V to 5.5 V on B Port ( $V_{CCA} \leq V_{CCB}$ )
- $V_{CC}$  Isolation Feature – If Either  $V_{CC}$  Input Is at GND, All Outputs Are in the High-Impedance State
- OE Input Circuit Referenced to  $V_{CCA}$
- Low Power Consumption, 5- $\mu$ A Max  $I_{CC}$
- $I_{off}$  Supports Partial-Power-Down Mode Operation
- Latch-Up Performance Exceeds 100 mA Per JESD 78, Class II
- ESD Protection Exceeds JESD 22
  - A Port
    - 2500-V Human-Body Model (A114-B)
    - 1500-V Charged-Device Model (C101)
  - B Port
    - $\pm 15$ -kV Human-Body Model (A114-B)
    - 1500-V Charged-Device Model (C101)

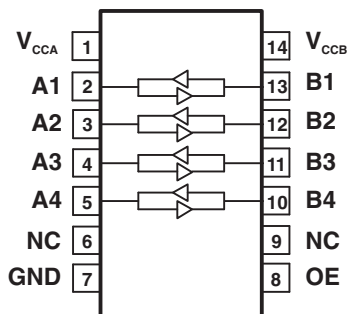
**GXU/ZXU PACKAGE  
(TOP VIEW)**



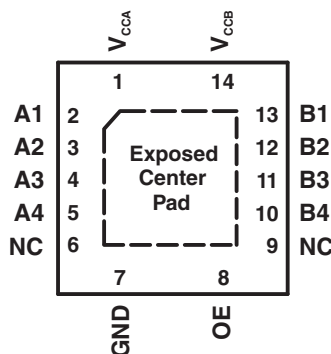
**TERMINAL ASSIGNMENTS  
(GXU/ZXU Package)**

	A	B	C
4	A4	GND	B4
3	A3	OE	B3
2	A2	$V_{CCA}$	B2
1	A1	$V_{CCB}$	B1

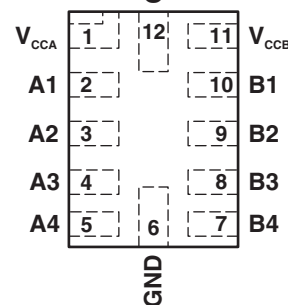
**D OR PW PACKAGE  
(TOP VIEW)**



**RGY PACKAGE  
(TOP VIEW)**



**RUT PACKAGE  
(TOP VIEW)**



- A. N.C. – No internal connection
- B. For RGY, if the exposed center pad is used, it must only be connected as a secondary ground or left electrically open.
- C. Pull up resistors are not required on both sides for Logic I/O.
- D. If pull up or pull down resistors are needed, the resistor value must be over 50 k $\Omega$ .
- E. 50 k $\Omega$  is a safe recommended value, if the customer can accept higher  $V_{ol}$  or lower  $V_{oh}$ , smaller pull up or pull down resistor is allowed, the draft estimation is  $V_{ol} = V_{ccout} \times 4.5k / (4.5k + R_{pu})$  and  $V_{oh} = V_{ccout} \times R_{dw} / (4.5k + R_{dw})$ .
- F. If pull up resistors are needed, please refer to the XTS0104 or contact TI.
- G. For detailed information, please refer to application note [SCEA043](#).



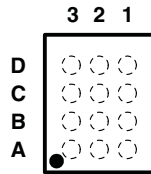
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NanoFree is a trademark of Texas Instruments.



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

**YZT PACKAGE  
(TOP VIEW)**



**TERMINAL ASSIGNMENTS  
(YZT Package)**

	3	2	1
D	A4	GND	B4
C	A3	OE	B3
B	A2	V <sub>CCA</sub>	B2
A	A1	V <sub>CCB</sub>	B1

## DESCRIPTION/ORDERING INFORMATION

This 4-bit noninverting translator uses two separate configurable power-supply rails. The A port is designed to track V<sub>CCA</sub>. V<sub>CCA</sub> accepts any supply voltage from 1.2 V to 3.6 V. The B port is designed to track V<sub>CCB</sub>. V<sub>CCB</sub> accepts any supply voltage from 1.65 V to 5.5 V. This allows for universal low-voltage bidirectional translation between any of the 1.2-V, 1.5-V, 1.8-V, 2.5-V, 3.3-V, and 5-V voltage nodes. V<sub>CCA</sub> should not exceed V<sub>CCB</sub>.

When the output-enable (OE) input is low, all outputs are placed in the high-impedance state. To ensure the high-impedance state during power up or power down, OE should be tied to GND through a pull-down resistor; the minimum value of the resistor is determined by the current-sourcing capability of the driver.

The TXB0104 is designed so that the OE input circuit is supplied by V<sub>CCA</sub>.

This device is fully specified for partial-power-down applications using I<sub>off</sub>. The I<sub>off</sub> circuitry disables the outputs, preventing damaging current backflow through the device when it is powered down.

## ORDERING INFORMATION<sup>(1)</sup>

T <sub>A</sub>	PACKAGE <sup>(2)</sup>		ORDERABLE PART NUMBER	TOP-SIDE MARKING <sup>(3)</sup>
-40°C to 85°C	NanoFree™ — WCSP (DSBGA) 0.23-mm Large Bump – YZT (Pb-free) 0.625-mm max height	Reel of 3000	TXB0104YZTR	_ _ _ 2 K _
	UFBGA – GXU	Reel of 2500	TXB0104GXUR	YE04
	UFBGA – ZXU (Pb-Free)	Reel of 2500	TXB0104ZXUR	YE04
	QFN – RGY	Reel of 1000	TXB0104RGYR	YE04
			TXB0104RGYRG4	
	uQFN – RUT	Reel of 3000	TXB0104RUTR	2KR
	SOIC – D	Tube of 50	TXB0104D	TXB0104
			TXB0104DG4	
		Reel of 2500	TXB0104DR	
			TXB0104DRG4	
TSSOP – PW	Reel of 2000	TXB0104PWR	YE04	
		TXB0104PWRG4		

(1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI web site at [www.ti.com](http://www.ti.com).

(2) Package drawings, thermal data, and symbolization are available at [www.ti.com/packaging](http://www.ti.com/packaging).

(3) YZT: The actual top-side marking has three preceding characters to denote year, month, and sequence code, and one following character to designate the wafer fab/assembly site. Pin 1 identifier indicates solder-bump composition (1 = SnPb, • = Pb-free).

**PIN DESCRIPTION**

PIN NO.		BALL NO.		NAME	FUNCTION
D, PW, OR RGY	RUT	GXU/ ZXU	YZT		
1	1	B2	B2	V <sub>CCA</sub>	A-port supply voltage $1.2\text{ V} \leq V_{CCA} \leq 3.6\text{ V}$ and $V_{CCA} \leq V_{CCB}$ .
2	2	A1	A3	A1	Input/output 1. Referenced to V <sub>CCA</sub> .
3	3	A2	B3	A2	Input/output 2. Referenced to V <sub>CCA</sub> .
4	4	A3	C3	A3	Input/output 3. Referenced to V <sub>CCA</sub> .
5	5	A4	D3	A4	Input/output 4. Referenced to V <sub>CCA</sub> .
6	–	–	–	NC	No connection. Not internally connected.
7	6	B4	D2	GND	Ground
8	12	B3	C2	OE	3-state output-mode enable. Pull OE low to place all outputs in 3-state mode. Referenced to V <sub>CCA</sub> .
9	–	–	–	NC	No connection. Not internally connected.
10	7	C4	D1	B4	Input/output 4. Referenced to V <sub>CCB</sub> .
11	8	C3	C1	B3	Input/output 3. Referenced to V <sub>CCB</sub> .
12	9	C2	B1	B2	Input/output 2. Referenced to V <sub>CCB</sub> .
13	10	C1	A1	B1	Input/output 1. Referenced to V <sub>CCB</sub> .
14	11	B1	A2	V <sub>CCB</sub>	B-port supply voltage $1.65\text{ V} \leq V_{CCB} \leq 5.5\text{ V}$ .

**ABSOLUTE MAXIMUM RATINGS<sup>(1)</sup>**

over operating free-air temperature range (unless otherwise noted)

			MIN	MAX	UNIT
V <sub>CCA</sub>	Supply voltage range		–0.5	4.6	V
V <sub>CCB</sub>			–0.5	6.5	
V <sub>I</sub>	Input voltage range	A port	–0.5	4.6	V
		B port	–0.5	6.5	
V <sub>O</sub>	Voltage range applied to any output in the high-impedance or power-off state	A port	–0.5	4.6	V
		B port	–0.5	6.5	
V <sub>O</sub>	Voltage range applied to any output in the high or low state <sup>(2)</sup>	A port	–0.5	V <sub>CCA</sub> + 0.5	V
		B port	–0.5	V <sub>CCB</sub> + 0.5	
I <sub>IK</sub>	Input clamp current	V <sub>I</sub> < 0		–50	mA
I <sub>OK</sub>	Output clamp current	V <sub>O</sub> < 0		–50	mA
I <sub>O</sub>	Continuous output current			±50	mA
	Continuous current through V <sub>CCA</sub> , V <sub>CCB</sub> , or GND			±100	mA
T <sub>stg</sub>	Storage temperature range		–65	150	°C

(1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

(2) The value of V<sub>CCA</sub> and V<sub>CCB</sub> are provided in the recommended operating conditions table.

**THERMAL IMPEDANCE RATINGS**

			UNIT	
$\theta_{JA}$	Package thermal impedance	D package <sup>(1)</sup>	86	°C/W
		GXU/ZXU package <sup>(1)</sup>	129	
		PW package <sup>(1)</sup>	113	
		RGY package <sup>(2)</sup>	47	
		RUT package	TBD	
		YZT package	90	

(1) The package thermal impedance is calculated in accordance with JESD 51-7.

(2) The package thermal impedance is calculated in accordance with JESD 51-5.

**RECOMMENDED OPERATING CONDITIONS<sup>(1) (2)</sup>**

			$V_{CCA}$	$V_{CCB}$	MIN	MAX	UNIT
$V_{CCA}$	Supply voltage				1.2	3.6	V
$V_{CCB}$					1.65	5.5	
$V_{IH}$	High-level input voltage	Data inputs	1.2 V to 3.6 V	1.65 V to 5.5 V	$V_{CCI} \times 0.65^{(3)}$	$V_{CCI}$	V
		OE	1.2 V to 3.6 V	1.65 V to 5.5 V	$V_{CCA} \times 0.65$	5.5	
$V_{IL}$	Low-level input voltage	Data inputs	1.2 V to 5.5 V	1.65 V to 5.5 V	0	$V_{CCI} \times 0.35^{(3)}$	V
		OE	1.2 V to 3.6 V	1.65 V to 5.5 V	0	$V_{CCA} \times 0.35$	
$V_O$	Voltage range applied to any output in the high-impedance or power-off state	A-port	1.2 V to 3.6 V	1.65 V to 5.5 V	0	3.6	V
		B-port			0	5.5	
$\Delta t/\Delta v$	Input transition rise or fall rate	A-port inputs	1.2 V to 3.6 V	1.65 V to 5.5 V		40	ns/V
		B-port inputs	1.2 V to 3.6 V	1.65 V to 3.6 V		40	
				4.5 V to 5.5 V		30	
$T_A$	Operating free-air temperature				-40	85	°C

(1) The A and B sides of an unused data I/O pair must be held in the same state, i.e., both at  $V_{CCI}$  or both at GND.

(2)  $V_{CCA}$  must be less than or equal to  $V_{CCB}$  and must not exceed 3.6 V.

(3)  $V_{CCI}$  is the supply voltage associated with the input port.

**ELECTRICAL CHARACTERISTICS<sup>(1) (2)</sup>**

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V <sub>CCA</sub>	V <sub>CCB</sub>	T <sub>A</sub> = 25°C			–40°C to 85°C		UNIT
					MIN	TYP	MAX	MIN	MAX	
V <sub>OHA</sub>		I <sub>OH</sub> = –20 μA	1.2 V		1.1			V <sub>CCA</sub> – 0.4		V
			1.4 V to 3.6 V							
V <sub>OLA</sub>		I <sub>OL</sub> = 20 μA	1.2 V		0.9			0.4		V
			1.4 V to 3.6 V							
V <sub>OHB</sub>		I <sub>OH</sub> = –20 μA		1.65 V to 5.5 V				V <sub>CCB</sub> – 0.4		V
V <sub>OLB</sub>		I <sub>OL</sub> = 20 μA		1.65 V to 5.5 V				0.4		V
I <sub>I</sub>	OE	V <sub>I</sub> = V <sub>CC1</sub> or GND	1.2 V to 3.6 V	1.65 V to 5.5 V	±1			±2		μA
I <sub>off</sub>	A port	V <sub>I</sub> or V <sub>O</sub> = 0 to 3.6 V	0 V	0 V to 5.5 V	±1			±2		μA
	B port	V <sub>I</sub> or V <sub>O</sub> = 0 to 5.5 V	0 V to 3.6 V	0 V	±1			±2		
I <sub>OZ</sub>	A or B port	OE = GND	1.2 V to 3.6 V	1.65 V to 5.5 V	±1			±2		μA
I <sub>CCA</sub>		V <sub>I</sub> = V <sub>CC1</sub> or GND, I <sub>O</sub> = 0	1.2 V	1.65 V to 5.5 V	0.06					μA
			1.4 V to 3.6 V	1.65 V to 5.5 V	5					
			3.6 V	0 V	2					
			0 V	5.5 V	–2					
I <sub>CCB</sub>		V <sub>I</sub> = V <sub>CC1</sub> or GND, I <sub>O</sub> = 0	1.2 V	1.65 V to 5.5 V	3.4					μA
			1.4 V to 3.6 V	1.65 V to 5.5 V	5					
			3.6 V	0 V	–2					
			0 V	5.5 V	2					
I <sub>CCA</sub> + I <sub>CCB</sub>		V <sub>I</sub> = V <sub>CC1</sub> or GND, I <sub>O</sub> = 0	1.2 V	1.65 V to 5.5 V	3.5					μA
			1.4 V to 3.6 V	1.65 V to 5.5 V	10					
I <sub>CCZA</sub>		V <sub>I</sub> = V <sub>CC1</sub> or GND, I <sub>O</sub> = 0, OE = GND	1.2 V	1.65 V to 5.5 V	0.05					μA
			1.4 V to 3.6 V	1.65 V to 5.5 V	5					
I <sub>CCZB</sub>		V <sub>I</sub> = V <sub>CC1</sub> or GND, I <sub>O</sub> = 0, OE = GND	1.2 V	1.65 V to 5.5 V	3.3					μA
			1.4 V to 3.6 V	1.65 V to 5.5 V	5					
C <sub>i</sub>	OE		1.2 V to 3.6 V	1.65 V to 5.5 V	3			4		pF
C <sub>io</sub>	A port		1.2 V to 3.6 V	1.65 V to 5.5 V	5			6		pF
	B port				11			14		

 (1) V<sub>CC1</sub> is the supply voltage associated with the input port.

 (2) V<sub>CC0</sub> is the supply voltage associated with the output port.

**TIMING REQUIREMENTS** $T_A = 25^\circ\text{C}$ ,  $V_{CCA} = 1.2\text{ V}$ 

		$V_{CCB} = 1.8\text{ V}$	$V_{CCB} = 2.5\text{ V}$	$V_{CCB} = 3.3\text{ V}$	$V_{CCB} = 5\text{ V}$	UNIT
		TYP	TYP	TYP	TYP	
Data rate		20	20	20	20	Mbps
$t_w$	Pulse duration	Data inputs	50	50	50	ns

**TIMING REQUIREMENTS**over recommended operating free-air temperature range,  $V_{CCA} = 1.5\text{ V} \pm 0.1\text{ V}$  (unless otherwise noted)

		$V_{CCB} = 1.8\text{ V} \pm 0.15\text{ V}$		$V_{CCB} = 2.5\text{ V} \pm 0.2\text{ V}$		$V_{CCB} = 3.3\text{ V} \pm 0.3\text{ V}$		$V_{CCB} = 5\text{ V} \pm 0.5\text{ V}$		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
Data rate		40		40		40		40		Mbps
$t_w$	Pulse duration	Data inputs	25	25	25	25	25	25	25	ns

**TIMING REQUIREMENTS**over recommended operating free-air temperature range,  $V_{CCA} = 1.8\text{ V} \pm 0.15\text{ V}$  (unless otherwise noted)

		$V_{CCB} = 1.8\text{ V} \pm 0.15\text{ V}$		$V_{CCB} = 2.5\text{ V} \pm 0.2\text{ V}$		$V_{CCB} = 3.3\text{ V} \pm 0.3\text{ V}$		$V_{CCB} = 5\text{ V} \pm 0.5\text{ V}$		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
Data rate		60		60		60		60		Mbps
$t_w$	Pulse duration	Data inputs	17	17	17	17	17	17	17	ns

**TIMING REQUIREMENTS**over recommended operating free-air temperature range,  $V_{CCA} = 2.5\text{ V} \pm 0.2\text{ V}$  (unless otherwise noted)

		$V_{CCB} = 2.5\text{ V} \pm 0.2\text{ V}$		$V_{CCB} = 3.3\text{ V} \pm 0.3\text{ V}$		$V_{CCB} = 5\text{ V} \pm 0.5\text{ V}$		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
Data rate		100		100		100		Mbps
$t_w$	Pulse duration	Data inputs	10	10	10	10	10	ns

**TIMING REQUIREMENTS**over recommended operating free-air temperature range,  $V_{CCA} = 3.3\text{ V} \pm 0.3\text{ V}$  (unless otherwise noted)

		$V_{CCB} = 3.3\text{ V} \pm 0.3\text{ V}$		$V_{CCB} = 5\text{ V} \pm 0.5\text{ V}$		UNIT
		MIN	MAX	MIN	MAX	
Data rate		100		100		Mbps
$t_w$	Pulse duration	Data inputs	10	10	10	ns

## SWITCHING CHARACTERISTICS

 $T_A = 25^\circ\text{C}$ ,  $V_{CCA} = 1.2\text{ V}$ 

PARAMETER	FROM (INPUT)	TO (OUTPUT)	$V_{CCB} = 1.8\text{ V}$	$V_{CCB} = 2.5\text{ V}$	$V_{CCB} = 3.3\text{ V}$	$V_{CCB} = 5\text{ V}$	UNIT
			TYP	TYP	TYP	TYP	
$t_{pd}$	A	B	6.9	5.7	5.3	5.5	ns
	B	A	7.4	6.4	6	5.8	
$t_{en}$	OE	A	1	1	1	1	$\mu\text{s}$
		B	1	1	1	1	
$t_{dis}$	OE	A	18	15	14	14	ns
		B	20	17	16	16	
$t_{rA}$ , $t_{fA}$	A-port rise and fall times		4.2	4.2	4.2	4.2	ns
$t_{rB}$ , $t_{fB}$	B-port rise and fall times		2.1	1.5	1.2	1.1	ns
$t_{SK(O)}$	Channel-to-channel skew		0.4	0.5	0.5	1.4	ns
Max data rate			20	20	20	20	Mbps

## SWITCHING CHARACTERISTICS

 over recommended operating free-air temperature range,  $V_{CCA} = 1.5\text{ V} \pm 0.1\text{ V}$  (unless otherwise noted)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	$V_{CCB} = 1.8\text{ V} \pm 0.15\text{ V}$		$V_{CCB} = 2.5\text{ V} \pm 0.2\text{ V}$		$V_{CCB} = 3.3\text{ V} \pm 0.3\text{ V}$		$V_{CCB} = 5\text{ V} \pm 0.5\text{ V}$		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
$t_{pd}$	A	B	1.4	12.9	1.2	10.1	1.1	10	0.8	9.9	ns
	B	A	0.9	14.2	0.7	12	0.4	11.7	0.3	13.7	
$t_{en}$	OE	A		1		1		1		1	$\mu\text{s}$
		B		1		1		1		1	
$t_{dis}$	OE	A	5.9	31	5.7	25.9	5.6	23	5.7	22.4	ns
		B	5.4	30.3	4.9	22.8	4.8	20	4.9	19.5	
$t_{rA}$ , $t_{fA}$	A-port rise and fall times		1.4	5.1	1.4	5.1	1.4	5.1	1.4	5.1	ns
$t_{rB}$ , $t_{fB}$	B-port rise and fall times		0.9	4.5	0.6	3.2	0.5	2.8	0.4	2.7	ns
$t_{SK(O)}$	Channel-to-channel skew			0.5		0.5		0.5		0.5	ns
Max data rate			40		40		40		40		Mbps

## SWITCHING CHARACTERISTICS

 over recommended operating free-air temperature range,  $V_{CCA} = 1.8\text{ V} \pm 0.15\text{ V}$  (unless otherwise noted)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	$V_{CCB} = 1.8\text{ V} \pm 0.15\text{ V}$		$V_{CCB} = 2.5\text{ V} \pm 0.2\text{ V}$		$V_{CCB} = 3.3\text{ V} \pm 0.3\text{ V}$		$V_{CCB} = 5\text{ V} \pm 0.5\text{ V}$		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
$t_{pd}$	A	B	1.6	11	1.4	7.7	1.3	6.8	1.2	6.5	ns
	B	A	1.5	12	1.3	8.4	1	7.6	0.9	7.1	
$t_{en}$	OE	A		1		1		1		1	$\mu\text{s}$
		B		1		1		1		1	
$t_{dis}$	OE	A	5.9	31	5.1	21.3	5	19.3	5	17.4	ns
		B	5.4	30.3	4.4	20.8	4.2	17.9	4.3	16.3	
$t_{rA}$ , $t_{fA}$	A-port rise and fall times		1	4.2	1.1	4.1	1.1	4.1	1.1	4.1	ns
$t_{rB}$ , $t_{fB}$	B-port rise and fall times		0.9	3.8	0.6	3.2	0.5	2.8	0.4	2.7	ns
$t_{SK(O)}$	Channel-to-channel skew			0.5		0.5		0.5		0.5	ns
Max data rate			60		60		60		60		Mbps

## SWITCHING CHARACTERISTICS

over recommended operating free-air temperature range,  $V_{CCA} = 2.5 \text{ V} \pm 0.2 \text{ V}$  (unless otherwise noted)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	$V_{CCB} = 2.5 \text{ V} \pm 0.2 \text{ V}$		$V_{CCB} = 3.3 \text{ V} \pm 0.3 \text{ V}$		$V_{CCB} = 5 \text{ V} \pm 0.5 \text{ V}$		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
$t_{pd}$	A	B	1.1	6.3	1	5.2	0.9	4.7	ns
	B	A	1.2	6.6	1.1	5.1	0.9	4.4	
$t_{en}$	OE	A	1		1		1		$\mu\text{s}$
		B	1		1		1		
$t_{dis}$	OE	A	5.1	21.3	4.6	15.2	4.6	13.2	ns
		B	4.4	20.8	3.8	16	3.9	13.9	
$t_{rA}, t_{fA}$	A-port rise and fall times		0.8	3	0.8	3	0.8	3	ns
$t_{rB}, t_{fB}$	B-port rise and fall times		0.7	2.6	0.5	2.8	0.4	2.7	ns
$t_{SK(O)}$	Channel-to-channel skew		0.5		0.5		0.5		ns
Max data rate			100		100		100		Mbps

## SWITCHING CHARACTERISTICS

over recommended operating free-air temperature range,  $V_{CCA} = 3.3 \text{ V} \pm 0.3 \text{ V}$  (unless otherwise noted)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	$V_{CCB} = 3.3 \text{ V} \pm 0.3 \text{ V}$		$V_{CCB} = 5 \text{ V} \pm 0.5 \text{ V}$		UNIT
			MIN	MAX	MIN	MAX	
$t_{pd}$	A	B	0.9	4.7	0.8	4	ns
	B	A	1	4.9	0.9	3.8	
$t_{en}$	OE	A	1		1		$\mu\text{s}$
		B	1		1		
$t_{dis}$	OE	A	4.6	15.2	4.3	12.1	ns
		B	3.8	16	3.4	13.2	
$t_{rA}, t_{fA}$	A-port rise and fall times		0.7	2.5	0.7	2.5	ns
$t_{rB}, t_{fB}$	B-port rise and fall times		0.5	2.1	0.4	2.7	ns
$t_{SK(O)}$	Channel-to-channel skew		0.5		0.5		ns
Max data rate			100		100		Mbps



**OPERATING CHARACTERISTICS**
 $T_A = 25^\circ\text{C}$ 

PARAMETER		TEST CONDITIONS	$V_{CCA}$						UNIT		
			1.2 V	1.2 V	1.5 V	1.8 V	2.5 V	2.5 V		3.3 V	
			$V_{CCB}$							3.3 V to 5 V	
			5 V	1.8 V	1.8 V	1.8 V	2.5 V	5 V			
				TYP	TYP	TYP	TYP	TYP	TYP	TYP	TYP
$C_{pdA}$	A-port input, B-port output	$C_L = 0$ , $f = 10$ MHz, $t_r = t_f = 1$ ns, OE = $V_{CCA}$ (outputs enabled)	7.8	10	9	8	8	8	8	9	pF
	B-port input, A-port output		12	11	11	11	11	11	11	11	
$C_{pdB}$	A-port input, B-port output		38.1	28	28	28	29	29	29	29	
	B-port input, A-port output		25.4	19	18	18	19	21	22	22	
$C_{pdA}$	A-port input, B-port output	$C_L = 0$ , $f = 10$ MHz, $t_r = t_f = 1$ ns, OE = GND (outputs disabled)	0.01	0.01	0.01	0.01	0.01	0.01	0.01	0.01	pF
	B-port input, A-port output		0.01	0.01	0.01	0.01	0.01	0.01	0.01	0.01	
$C_{pdB}$	A-port input, B-port output		0.01	0.01	0.01	0.01	0.01	0.01	0.01	0.03	
	B-port input, A-port output		0.01	0.01	0.01	0.01	0.01	0.01	0.01	0.04	

## PRINCIPLES OF OPERATION

### Applications

The TXB0104 can be used in level-translation applications for interfacing devices or systems operating at different interface voltages with one another.

### Architecture

The TXB0104 architecture (see [Figure 1](#)) does not require a direction-control signal to control the direction of data flow from A to B or from B to A. In a dc state, the output drivers of the TXB0104 can maintain a high or low, but are designed to be weak, so that they can be overdriven by an external driver when data on the bus starts flowing the opposite direction.

The output one shots detect rising or falling edges on the A or B ports. During a rising edge, the one shot turns on the PMOS transistors (T1, T3) for a short duration, which speeds up the low-to-high transition. Similarly, during a falling edge, the one shot turns on the NMOS transistors (T2, T4) for a short duration, which speeds up the high-to-low transition. The typical output impedance during output transition is 70  $\Omega$  at  $V_{CCO} = 1.2\text{ V to }1.8\text{ V}$ , 50  $\Omega$  at  $V_{CCO} = 1.8\text{ V to }3.3\text{ V}$ , and 40  $\Omega$  at  $V_{CCO} = 3.3\text{ V to }5\text{ V}$ .

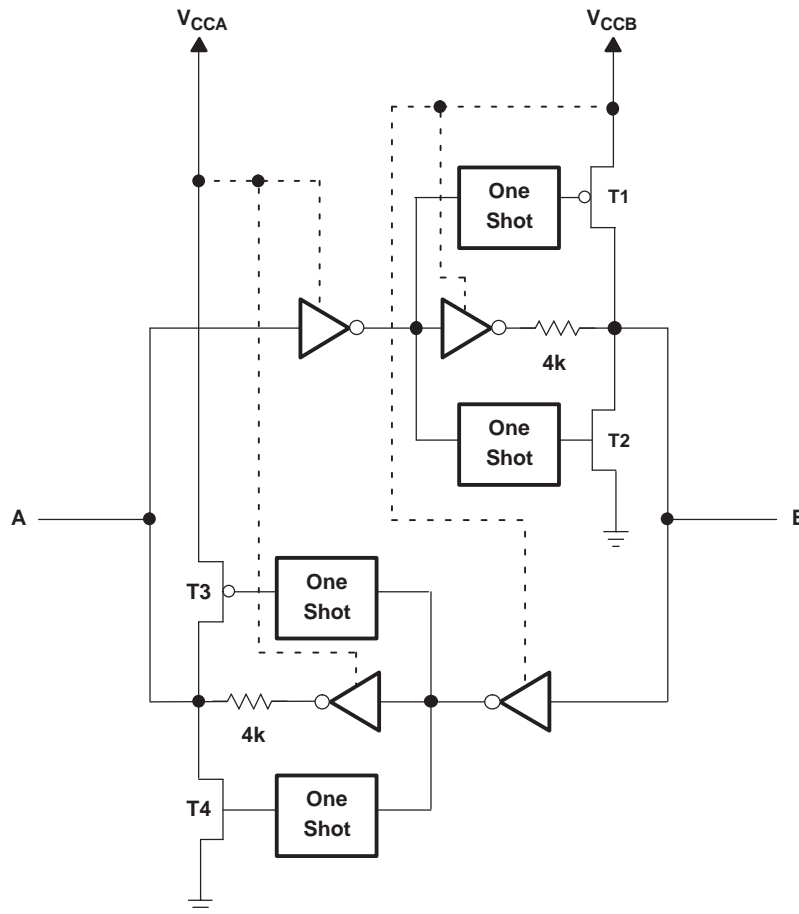
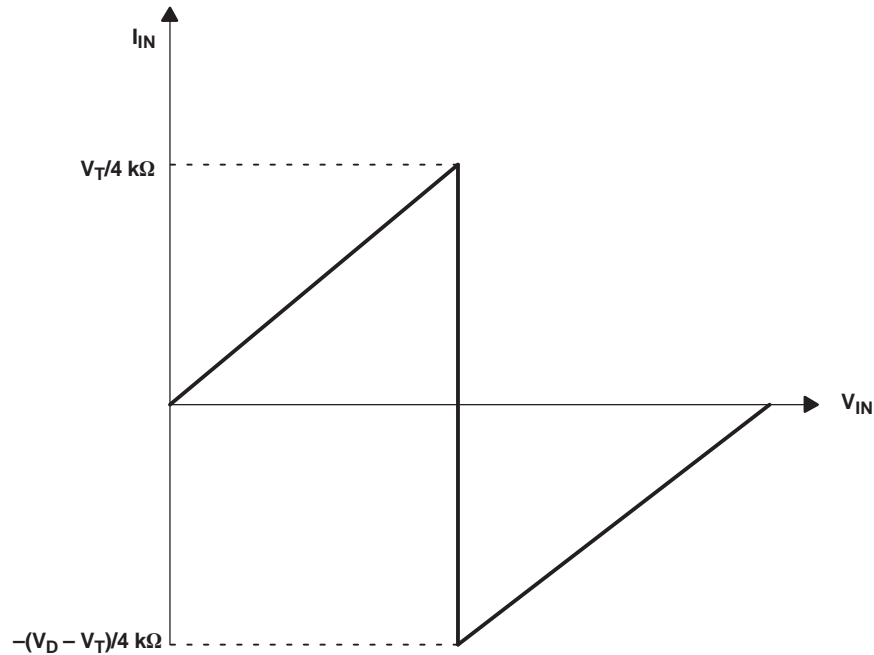


Figure 1. Architecture of TXB0104 I/O Cell

### Input Driver Requirements

Typical  $I_{IN}$  vs  $V_{IN}$  characteristics of the TXB0104 are shown in [Figure 2](#). For proper operation, the device driving the data I/Os of the TXB0104 must have drive strength of at least  $\pm 2\text{ mA}$ .



- A.  $V_T$  is the input threshold voltage of the TXB0104 (typically  $V_{CC}/2$ ).
- B.  $V_D$  is the supply voltage of the external driver.

**Figure 2. Typical  $I_{IN}$  vs  $V_{IN}$  Curve**

### Power Up

During operation, ensure that  $V_{CCA} \leq V_{CCB}$  at all times. During power-up sequencing,  $V_{CCA} \geq V_{CCB}$  does not damage the device, so any power supply can be ramped up first. The TXB0104 has circuitry that disables all output ports when either  $V_{CC}$  is switched off ( $V_{CCA/B} = 0 \text{ V}$ ).

### Enable and Disable

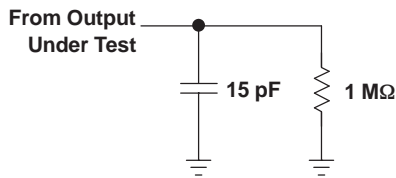
The TXB0104 has an OE input that is used to disable the device by setting OE = low, which places all I/Os in the high-impedance (Hi-Z) state. The disable time ( $t_{dis}$ ) indicates the delay between when OE goes low and when the outputs actually get disabled (Hi-Z). The enable time ( $t_{en}$ ) indicates the amount of time the user must allow for the one-shot circuitry to become operational after OE is taken high.

### Pullup or Pulldown Resistors on I/O Lines

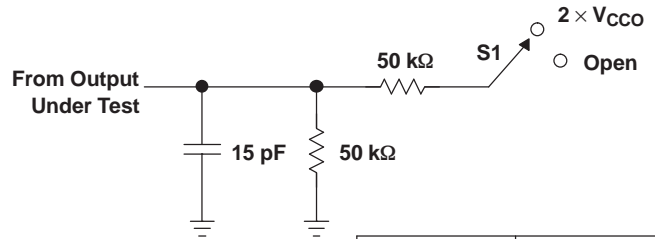
The TXB0104 is designed to drive capacitive loads of up to 70 pF. The output drivers of the TXB0104 have low dc drive strength. If pullup or pulldown resistors are connected externally to the data I/Os, their values must be kept higher than 50 k $\Omega$  to ensure that they do not contend with the output drivers of the TXB0104.

For the same reason, the TXB0104 should not be used in applications such as I<sup>2</sup>C or 1-Wire where an open-drain driver is connected on the bidirectional data I/O. For these applications, use a device from the TI TXS01xx series of level translators.

**PARAMETER MEASUREMENT INFORMATION**

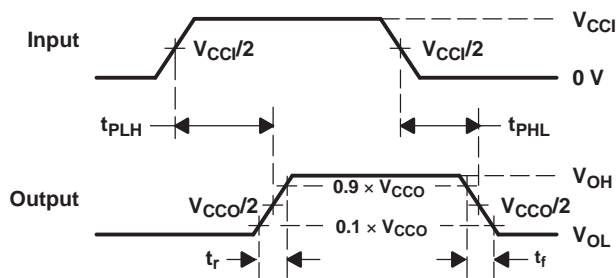


**LOAD CIRCUIT FOR MAX DATA RATE, PULSE DURATION PROPAGATION DELAY OUTPUT RISE AND FALL TIME MEASUREMENT**

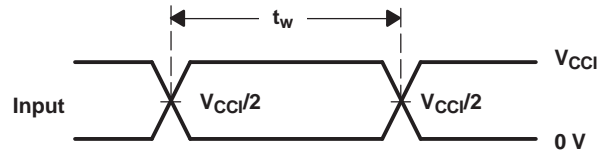


**LOAD CIRCUIT FOR ENABLE/DISABLE TIME MEASUREMENT**

TEST	S1
$t_{pZL}/t_{pLZ}$	$2 \times V_{CCO}$
$t_{pHZ}/t_{pZH}$	Open



**VOLTAGE WAVEFORMS PROPAGATION DELAY TIMES**



**VOLTAGE WAVEFORMS PULSE DURATION**

- A.  $C_L$  includes probe and jig capacitance.
- B. All input pulses are supplied by generators having the following characteristics:  $PRR \leq 10$  MHz,  $Z_O = 50 \Omega$ ,  $dv/dt \geq 1$  V/ns.
- C. The outputs are measured one at a time, with one transition per measurement.
- D.  $t_{PLH}$  and  $t_{PHL}$  are the same as  $t_{pd}$ .
- E.  $V_{CCI}$  is the  $V_{CC}$  associated with the input port.
- F.  $V_{CCO}$  is the  $V_{CC}$  associated with the output port.
- G. All parameters and waveforms are not applicable to all devices.

**Figure 3. Load Circuits and Voltage Waveforms**

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**REVISION HISTORY**

<b>Changes from Revision E (February 2010) to Revision F</b>	<b>Page</b>
<hr/> <ul style="list-style-type: none"><li>• Added notes to pin out graphics. ....</li></ul> <hr/>	<hr/> <b>1</b> <hr/>

**PACKAGING INFORMATION**

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TXB0104D	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	TXB0104	<a href="#">Samples</a>
TXB0104DG4	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	TXB0104	<a href="#">Samples</a>
TXB0104DR	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	TXB0104	<a href="#">Samples</a>
TXB0104DRG4	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	TXB0104	<a href="#">Samples</a>
TXB0104GXUR	ACTIVE	BGA MICROSTAR JUNIOR	GXU	12	2500	TBD	SNPB	Level-1-240C-UNLIM	-40 to 85	YE04	<a href="#">Samples</a>
TXB0104PWR	ACTIVE	TSSOP	PW	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	YE04	<a href="#">Samples</a>
TXB0104PWRG4	ACTIVE	TSSOP	PW	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	YE04	<a href="#">Samples</a>
TXB0104RGYR	ACTIVE	VQFN	RGY	14	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	YE04	<a href="#">Samples</a>
TXB0104RGYRG4	ACTIVE	VQFN	RGY	14	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	YE04	<a href="#">Samples</a>
TXB0104RUTR	ACTIVE	UQFN	RUT	12	3000	Green (RoHS & no Sb/Br)	CU NIPDAUAG	Level-1-260C-UNLIM	-40 to 85	2KR	<a href="#">Samples</a>
TXB0104YZTR	ACTIVE	DSBGA	YZT	12	3000	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM	-40 to 85	(2K ~ 2K7)	<a href="#">Samples</a>
TXB0104ZXUR	ACTIVE	BGA MICROSTAR JUNIOR	ZXU	12	2500	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM	-40 to 85	YE04	<a href="#">Samples</a>

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSELETE:** TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

**TBD:** The Pb-Free/Green conversion plan has not been defined.

**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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#### **OTHER QUALIFIED VERSIONS OF TXB0104 :**

- Automotive: [TXB0104-Q1](#)

NOTE: Qualified Version Definitions:

- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects

## TAPE AND REEL INFORMATION



### QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TXB0104DR	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
TXB0104GXUR	BGA MICROSTAR JUNIOR	GXU	12	2500	330.0	8.4	2.3	2.8	1.0	4.0	8.0	Q2
TXB0104PWR	TSSOP	PW	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
TXB0104RGYR	VQFN	RGY	14	3000	330.0	12.4	3.75	3.75	1.15	8.0	12.0	Q1
TXB0104RUTR	UQFN	RUT	12	3000	180.0	8.4	1.95	2.3	0.75	4.0	8.0	Q1
TXB0104YZTR	DSBGA	YZT	12	3000	180.0	8.4	1.49	1.99	0.75	4.0	8.0	Q2
TXB0104ZXUR	BGA MICROSTAR JUNIOR	ZXU	12	2500	330.0	8.4	2.3	2.8	1.0	4.0	8.0	Q2



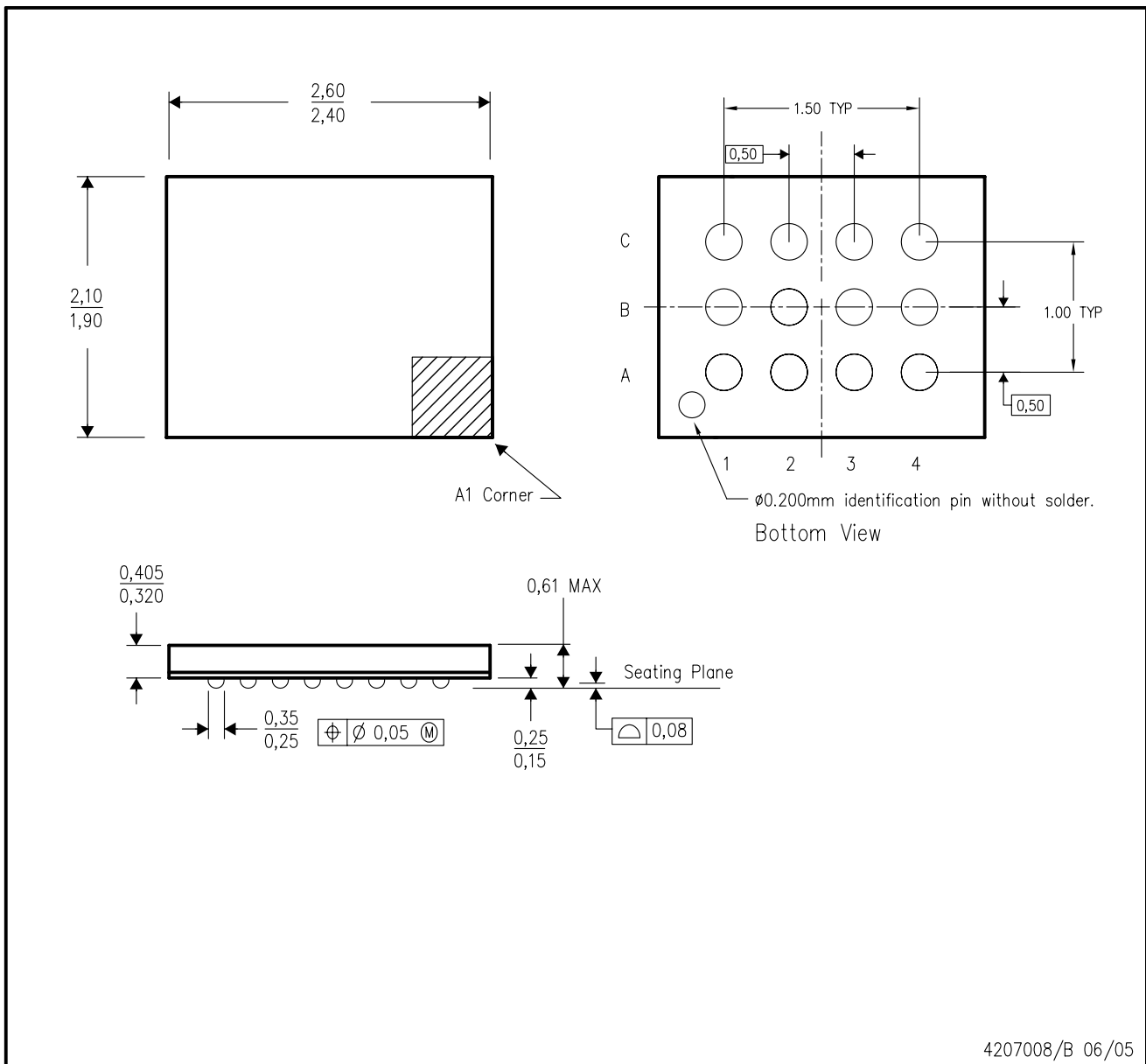
**TAPE AND REEL BOX DIMENSIONS**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TXB0104DR	SOIC	D	14	2500	367.0	367.0	38.0
TXB0104GXUR	BGA MICROSTAR JUNIOR	GXU	12	2500	338.1	338.1	20.6
TXB0104PWR	TSSOP	PW	14	2000	367.0	367.0	35.0
TXB0104RGYR	VQFN	RGY	14	3000	367.0	367.0	35.0
TXB0104RUTR	UQFN	RUT	12	3000	202.0	201.0	28.0
TXB0104YZTR	DSBGA	YZT	12	3000	182.0	182.0	17.0
TXB0104ZXUR	BGA MICROSTAR JUNIOR	ZXU	12	2500	338.1	338.1	20.6

GXU (S-PBGA-N12)

PLASTIC BALL GRID ARRAY

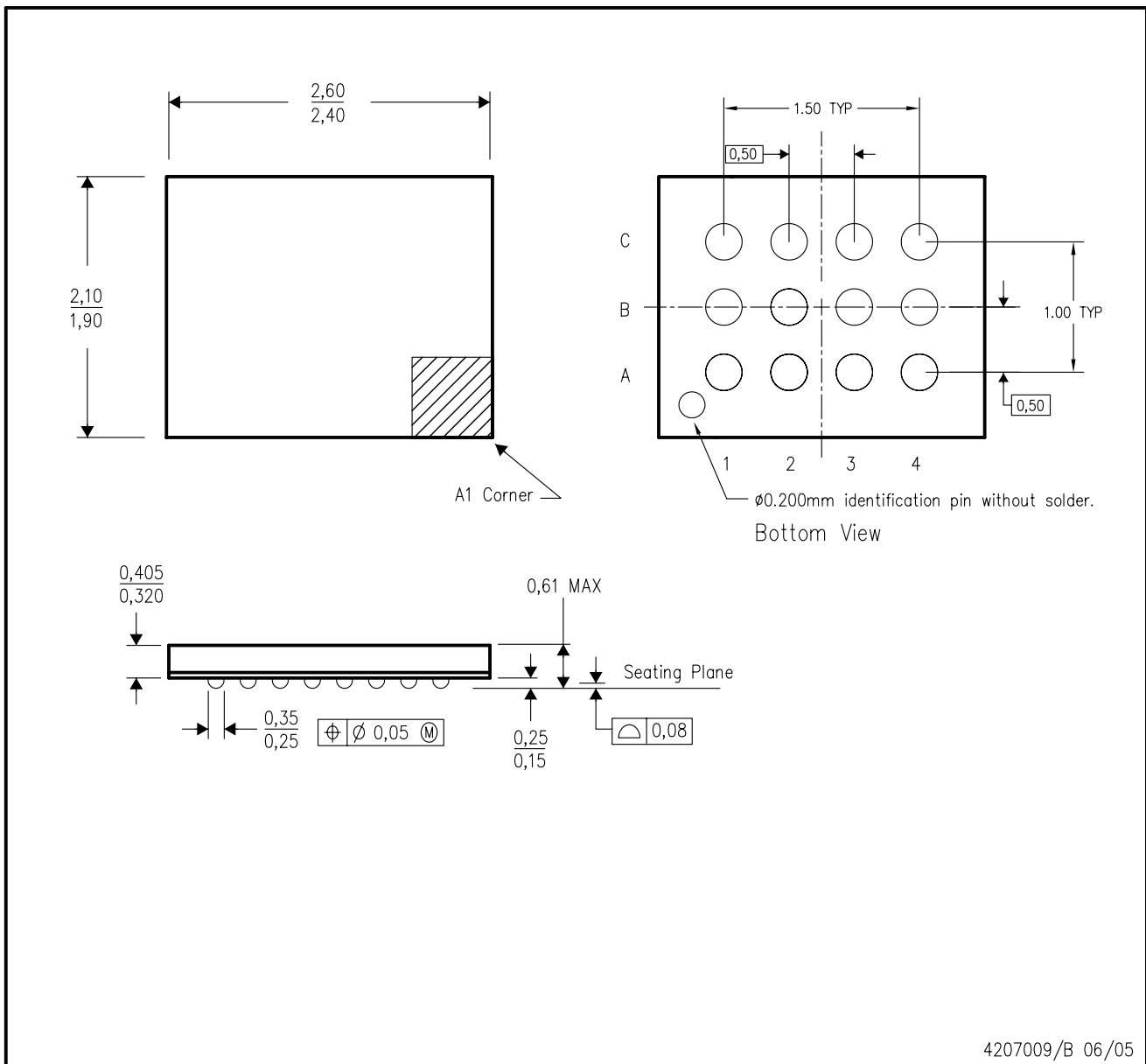


4207008/B 06/05

- NOTES:
- A. All linear dimensions are in millimeters.
  - B. This drawing is subject to change without notice.

ZXU (S-PBGA-N12)

PLASTIC BALL GRID ARRAY



- NOTES:
- A. All linear dimensions are in millimeters.
  - B. This drawing is subject to change without notice.
  - C. This package is a lead-free solder ball design.

D (R-PDSO-G14)

PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in inches (millimeters).
  - B. This drawing is subject to change without notice.
  -  Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
  -  Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
  - E. Reference JEDEC MS-012 variation AB.

D (R-PDSO-G14)

PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in millimeters.
  - B. This drawing is subject to change without notice.
  - C. Publication IPC-7351 is recommended for alternate designs.
  - D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
  - E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.



PW (R-PDSO-G14)

PLASTIC SMALL OUTLINE



- NOTES:
- All linear dimensions are in millimeters.
  - This drawing is subject to change without notice.
  - Publication IPC-7351 is recommended for alternate designs.
  - Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
  - Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

RGY (S-PVQFN-N14)

PLASTIC QUAD FLATPACK NO-LEAD



- NOTES:
- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
  - B. This drawing is subject to change without notice.
  - C. QFN (Quad Flatpack No-Lead) package configuration.
  - D. The package thermal pad must be soldered to the board for thermal and mechanical performance.
  - E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
  - F. Pin 1 identifiers are located on both top and bottom of the package and within the zone indicated. The Pin 1 identifiers are either a molded, marked, or metal feature.
  - G. Package complies to JEDEC MO-241 variation BA.



RGY (S-PVQFN-N14)

PLASTIC QUAD FLATPACK NO-LEAD

**THERMAL INFORMATION**

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No-Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at [www.ti.com](http://www.ti.com).

The exposed thermal pad dimensions for this package are shown in the following illustration.



Bottom View

Exposed Thermal Pad Dimensions

4206353-2/P 03/14

NOTE: All linear dimensions are in millimeters

RGY (S-PVQFN-N14)

PLASTIC QUAD FLATPACK NO-LEAD

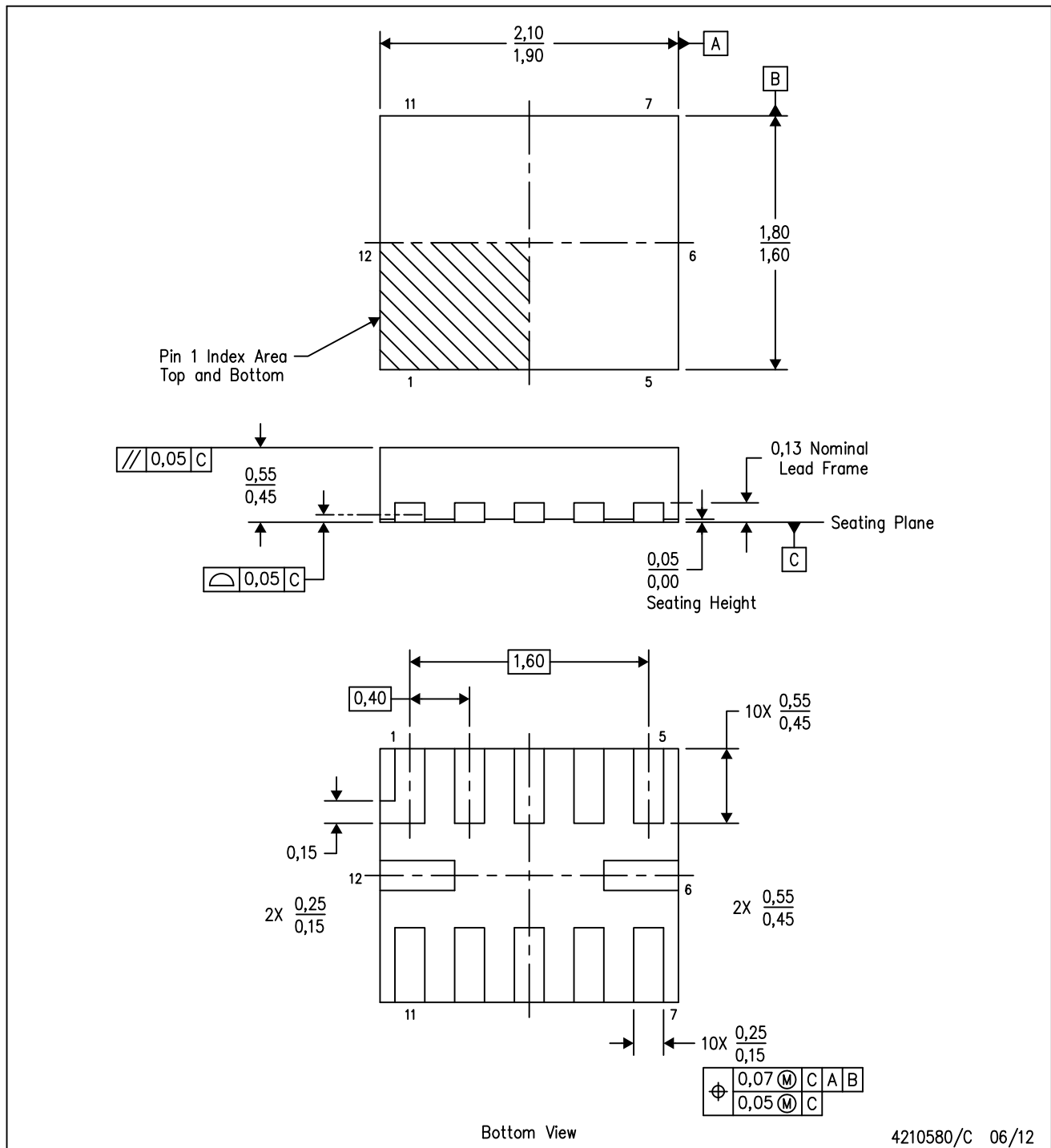


4208122-2/P 03/14

- NOTES:
- All linear dimensions are in millimeters.
  - This drawing is subject to change without notice.
  - Publication IPC-7351 is recommended for alternate designs.
  - This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, Quad Flat-Pack QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at [www.ti.com](http://www.ti.com) <<http://www.ti.com>>.
  - Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
  - Customers should contact their board fabrication site for minimum solder mask web tolerances between signal pads.

RUT (R-PUQFN-N12)

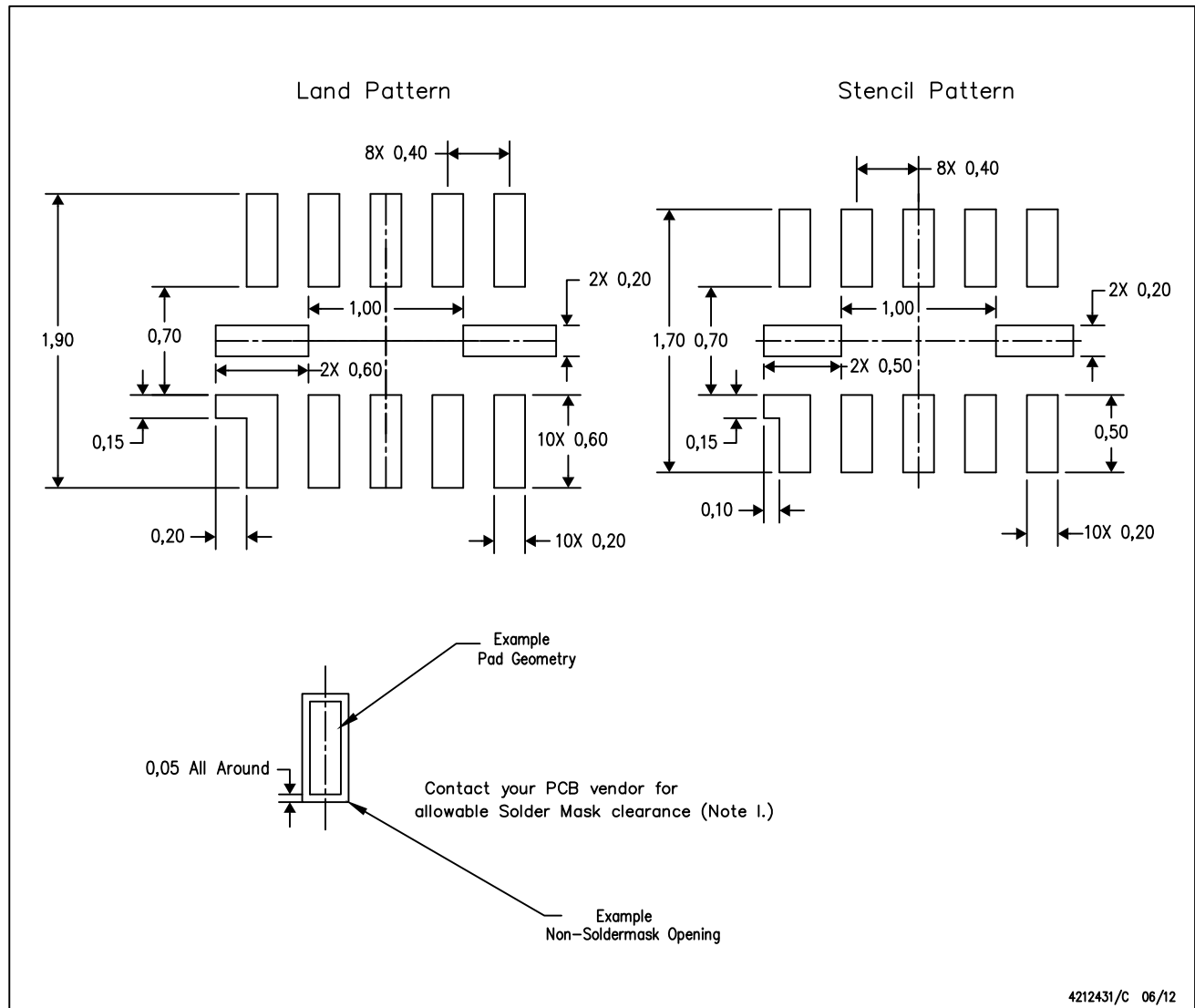
PLASTIC QUAD FLATPACK NO-LEAD



- NOTES:
- All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
  - This drawing is subject to change without notice.
  - QFN (Quad Flatpack No-Lead) package configuration.

RUT (R-PUQFN-N12)

PLASTIC QUAD FLATPACK NO-LEAD



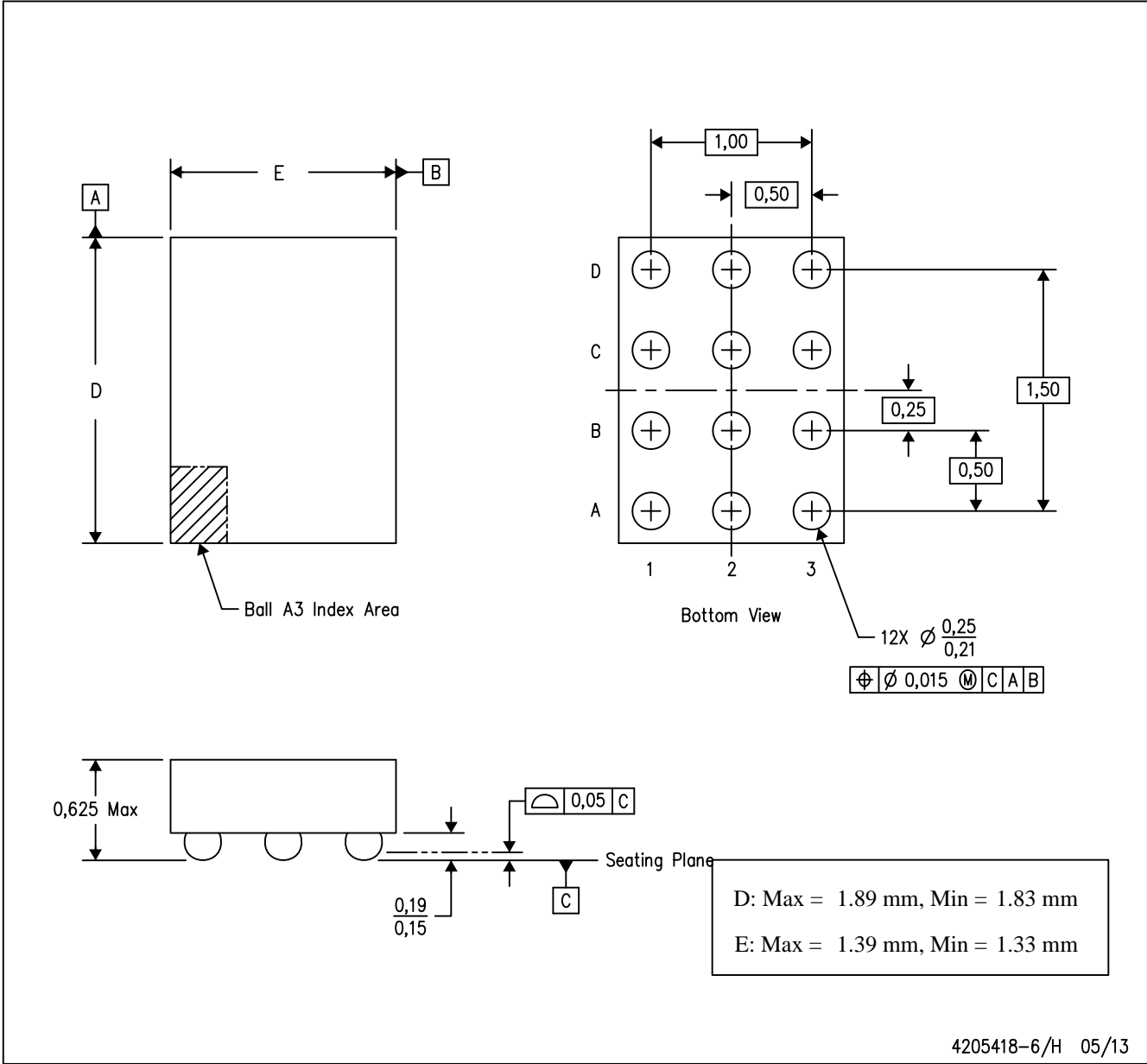
4212431/C 06/12

- NOTES:
- A. All linear dimensions are in millimeters.
  - B. This drawing is subject to change without notice.
  - C. Publication IPC-7351 is recommended for alternate designs.
  - D. Customers should contact their board fabrication site for minimum solder mask web tolerances between signal pads.
  - E. Maximum stencil thickness 0,1016 mm (4 mils). All linear dimensions are in millimeters.
  - F. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
  - G. Over-printing land for larger area ratio is not advised due to land width and bridging potential. Exercise extreme caution.
  - H. Suggest stencils cut with lasers such as Fiber Laser that produce the greatest positional accuracy.
  - I. Component placement force should be minimized to prevent excessive paste block deformation.

**MECHANICAL DATA**

YZT (R-XBGA-N12)

(CUSTOM) DIE-SIZE BALL GRID ARRAY



- NOTES:
- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
  - B. This drawing is subject to change without notice.
  - C. NanoFree™ package configuration.

NanoFree is a trademark of Texas Instruments.

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