# PIC32MK General Purpose and Motor Control (GP/MC) Silicon Errata and Data Sheet Clarification

The PIC32MK General Purpose and Motor Control (GP/MC) family of devices that you have received conform functionally to the current Device Data Sheet (DS60001402**D**), except for the anomalies described in this document.

The silicon issues discussed in the following pages are for silicon revisions with the Device and Revision IDs listed in Table 1. The silicon issues are summarized in Table 2.

The errata described in this document will be addressed in future revisions of the PIC32MK General Purpose and Motor Control (GP/MC) family silicon.

**Note:** This document summarizes all silicon errata issues from all revisions of silicon, previous and current. Only the issues indicated in the last column of Table 2 apply to the current silicon revision (**A2**).

Data Sheet clarifications and corrections (if applicable) start on page 15 following the discussion of silicon issues.

The silicon revision level can be identified using the current version of MPLAB® X IDE and Microchip's programmers, debuggers, and emulation tools, which are available at the Microchip corporate web site (www.microchip.com).

For example, to identify the silicon revision level using MPLAB X IDE in conjunction with a hardware debugger:

1. Using the appropriate interface, connect the device to the hardware debugger.
2. Open an MPLAB X IDE project.
3. Configure the MPLAB X IDE project for the appropriate device and hardware debugger.
4. Select *Window > Dashboard*, and then click the **Refresh Debug Tool Status** icon ( ).
5. The part number and the Device and Revision ID values appear in the **Output** window.

**Note:** If you are unable to extract the silicon revision level, please contact your local Microchip sales office for assistance.

The Device and Revision ID values for the various PIC32MK General Purpose and Motor Control (GP/MC) family silicon revisions are shown in Table 1.

| Part Number | Device ID(1) | Revision ID for Silicon Revision(1) | |
|---|---|---|---|
| | | A1 | A2 |
| PIC32MK1024MCF100 | 0x6201053 | 0x1 | 0x2 |
| PIC32MK1024MCF064 | 0x6202053 | | |
| PIC32MK0512MCF100 | 0x6204053 | | |
| PIC32MK0512MCF064 | 0x6205053 | | |
| PIC32MK1024GPE100 | 0x6207053 | | |
| PIC32MK1024GPE064 | 0x6208053 | | |
| PIC32MK0512GPE100 | 0x620A053 | | |
| PIC32MK0512GPE064 | 0x620B053 | | |
| PIC32MK1024GPD100 | 0x620D053 | | |
| PIC32MK1024GPD064 | 0x620E053 | | |
| PIC32MK0512GPD100 | 0x6210053 | | |
| PIC32MK0512GPD064 | 0x6211053 | | |

**Note 1:** Refer to the **"Memory Organization"** and **"Special Features"** chapters in the current Device Data Sheet (DS60001402**D**) for detailed information on Device and Revision IDs for your specific device.

| Module | Feature | Item | Issue Summary | Affected Revisions(1) | |
|---|---|---|---|---|---|
| | | | | A1 | A2 |
| Primary Oscillator | POSC | 1. | Crystal primary oscillator (POSC) supports reduced operating range with restrictions. | X | X |
| Secondary Oscillator | SOSC | 2. | The Secondary Oscillator (SOSC) does not support crystal operation. | X | X |
| Clocks | PBCLK6 | 3. | PBCLK6 defaults to 1:2 instead of 1:4. | X | X |
| FSCM | Clock Fail | 4. | Device falls back to LPRC instead of FRC on FSCM event. | X | X |
| VBAT | VBAT | 5. | VBAT is not functional. | X | X |
| VBAT | RTCC | 6. | RTCC may lose SOSC clocks momentarily during a VDD to VBAT switch over event. | X | X |
| ADC | Level Trigger | 7. | The ADC level trigger will not perform burst conversions in Debug mode. | X | X |
| ADC | Turbo Mode | 8. | Turbo mode is not functional when two channels are linked for the purpose of increasing effective throughput. | X | X |
| ADC | DNL | 9. | In Differential mode, DNL for code 3072 is not within specification. | X | X |
| ADC | AN26 | 10. | ADC input AN26 is not functional. | X | X |
| ADC | Scan | 11. | Scan list conversion will restart without finishing current scan list if new trigger occurs before scan completion with ADC7. | X | X |
| ADC | Scan | 12. | Shared ADC7 has high Offset and Gain Error in Scan mode. | X | X |
| Op amp | Op amp | 13. | Enabling an Op amp output control bit disables respective comparators output pin function if also enabled but comparator output status bit is still functional. | X | X |
| Op amp | Op amp | 14. | Op amp output is always enabled regardless of output enable control bit if OPAMP is enabled. | X | X |
| Op amp | Op amp PGA Mode | 15. | When used in PGA Unity Gain mode, an Op amp continues to function despite being disabled (i.e., AMPMOD = 0). | X | X |
| Op amp | Op amp PGA Mode | 16. | Op amps in Unity Gain mode (i.e., ENPGAx bit (CFGCON2<4, 2:0> = 1) are non-functional. | X | X |
| Op amp | PSRR | 17. | Op amp does not meet PSRR electrical specification. | X | X |
| Op amp | Common Mode | 18. | Op amps do not meet common mode voltage range (VCMR) specification. | X | X |
| Op amp | CMRR | 19. | Op amps do not meet CMRR specification. | X | X |
| Op amp | Gain Margin | 20. | Op amps do not meet gain margin specification. | X | X |
| DAC | INL | 21. | The DACs do not meet INL specification at AVDD less than 3V, and TA is greater than +85ºC. | X | X |
| DAC | DNL | 22. | The DACs do not meet DNL specification at AVDD less than 3V. | X | X |
| Timer1 | Counter Async | 23. | Timer1 in Asynchronous External Counter mode does not reflect the first count from an external ext T1CK input. | X | X |
| Timer1 | Sleep Async | 24. | TMR1 register of Timer1 in Asynchronous mode remains at initial set value of five external clock pulses after wake-up from Sleep mode. | X | X |
| Timer1 | Sleep Async | 25. | Back-to-back writes to the TMR1 register are not allowed for four PBCLK2 cycles. | X | X |

**Note 1:** Only those issues indicated in the last column apply to the current silicon revision.

| Module | Feature | Item | Issue Summary | Affected Revisions(1) | |
|---|---|---|---|---|---|
| | | | | A1 | A2 |
| I/O | RTCC | 26. | RTCC alarm output driver does not return to default/reset state on deep sleep wake-up through MCLR. | X | X |
| Deep Sleep | I/O | 27. | Deep Sleep mode is non functional. | X | X |
| RCON | Register | 28. | RCON status bits, VBPOR, PORIO, PORCORE, and VBAT, are inconsistent and cannot be used. | X | X |
| Sleep | IPD | 29. | 3 mA increase in sleep when PB5DIV is disabled. | X | X |
| Sleep | IPD | 30. | Increase in sleep IPD current if USB pins D+ and D- are floating. | X | X |
| PMP | Status Flags | 31. | PMP input buffer full flag IB0F and out buffer underflow OBUF are set as soon as PMP is turned ON in Slave mode, when TTLEN = 1. | X | X |
| PMP | Slave Mode | 32. | CS is deasserting before RD in Slave mode. | X | X |
| CTMU | Triggers | 33. | Edge Sequencing mode (EDGSEQEN (CTMUCON<2>)) triggers are not functional | X | X |
| CTMU | TGEN | 34. | When the TGEN bit is set, manual current sourcing (i.e., setting the EDG1STAT bit) from CTMU is not possible. | X | X |
| ICAP | Debug | 35. | Debug breakpoints are not supported when using Input Capture with DMA. | X | X |
| PWM | Time Base | 36. | Leading-edge Blanking (LED) in XPRES mode, XPRES bit (PWMCONx<2>) = 1, is not functional. | X | X |
| PWM | I/O | 37. | Alternate pin and I/O functions on unused PWM channels do not function when the PWM module is enabled. | X | X |
| PWM | LEB | 38. | Incorrect LEB trigger applied if dead time is enabled. | X | X |
| PWM | Interrupts | 39. | Multiple PWM Interrupts can occur for a single TRGIF, PWMLIF, and PWMHIF interrupt event, which causes the ISR to be re-executed multiple times if the PWM prescaler (i.e., PCLKDIV<2:0> bits (PTCON<6:4>)) or SCLKDIV<2:0> bits (STCON<6:4>) are greater than 5. | X | X |
| UART | TX/RX Interrupt | 40. | A UART Transmit Interrupt (UTXISEL<1:0> bits (UxSTA<15:14>) = ‘0b00) is generated and asserted while the transmit buffer contains at least one empty space and the UART Receiver Interrupt Flag bit (URXISEL<1:0> bits (UxSTA<7:6>) = ‘0b00) is asserted while the receive buffer is not empty and non-functional. | X | X |
| UART | TX Interrupt | 41. | A UART Transmit Interrupt (UTXISEL<1:0> bits = ‘0b01) is generated, but does not remain asserted when all of the characters have been transmitted. | X | X |
| UART | TX Interrupt | 42. | A UART Transmit Interrupt (UTXISEL<1:0> bits = ‘0b10) is generated but does not remain asserted while the transmit buffer is empty. | X | X |
| UART | RX Interrupt | 43. | The UART Receive Interrupt flag (URXISEL<1:0> bits = ‘0b01) is asserted only when the receive buffer equals one-half full and not when the receive buffer is greater than one-half full. | X | X |
| UART | RX Interrupt | 44. | The UART Receive Interrupt Flag bit (URXISEL<1:0> bits = ‘0b10) is asserted only when the receive buffer equals three-quarters full and not when the receive buffer is greater than three-quarters full. | X | X |

**Note 1:** Only those issues indicated in the last column apply to the current silicon revision.

| Module | Feature | Item | Issue Summary | Affected Revisions(1) | |
|---|---|---|---|---|---|
| | | | | A1 | A2 |
| UART | High Speed Mode | 45. | The UART Stop bit duration is shorter than expected in High-Speed mode (UxMODE.BRGH =1) for baud rates less than 7.5 MBPS. | X | X |
| CAN | Interrupt | 46. | The CAN Wake Interrupt Flag bit, WAKIF (CxINT<14>), is set even when the CAN module is disabled. | X | X |
| Deadman Timer (DMT) | Reset | 47. | The Deadman Timer module does not cause a Non-maskable Interrupt (NMI) on a BAD1, BAD2, or DMTEVENT. | X | X |
| Watchdog Timer (WDT) | WDT | 48. | Multiple valid key writes can be performed outside the Watchdog Timer window before a Reset occurs instead of the required single write. | X | X |
| ICSP | TDO | 49. | The TDO pin becomes an output and toggles while programming on any of the ICSP PGECx/PGEDx pair. | X | X |
| VIH | Input Specification | 50. | VIH(MIN) does not meet the electrical specification of (0.65 * VDD), but instead VIH(MIN) = (0.8 * VDD). | X | X |
| Cache | Exception | 51. | A Data Bus Error Exception can occur when prefetch cache is enabled (PREFEN<1:0> bits (CHECON<5:4>) = ‘0b01). | X | |
| BOR | POR | 52. | On a BOR event, and when the BORSEL bit (DEVCFG2<29>) = 0, the POR Status bit (RCON<1>) may also be erroneously set. | X | X |
| BOR | Reset | 53. | On a BOR event, VPOR < VDD < VBOR, a Reset is not generated when the BOR threshold is reached. System clocks will stop with all I/O pins function frozen in their present state until either VDD falls to VPOR or VDD returns to above VBOR. | X | |
| SPI2 | PPS | 54. | The SPI SS2R PPS register cannot be read nor used with bit instruction of the form SS2Rbits.SS2R as it is a read-modify-write command. | X | X |
| DMA | R/W access to a peripheral | 55. | The CPU and DMA controller must not be allowed to simultaneously attempt access to the same peripheral bus. | X | X |

**Note 1:** Only those issues indicated in the last column apply to the current silicon revision.

## Silicon Errata Issues

**Note 1:** This document summarizes all silicon errata issues from all revisions of silicon, previous as well as current. The table provided in each issue indicates which issues exist for a particular revision of silicon.

**2:** The following applies to the Affected Silicon Revision tables in each silicon issue:

- An 'X' indicates the issue is present in this revision of silicon.
- Shaded cells with an Em dash ('—') indicate that this silicon revision does not exist for this issue.
- Blank cells indicate an issue has been corrected or does not exist in this revision of silicon.

## 1. Module: Primary Oscillator

The POSC supports only specific crystal operation. as provided in Table 3.

**Work around 1**

The Primary Oscillator (POSC) has been characterized to operate at 8 MHz and 12 MHz when the circuit shown in Figure 1 is implemented and the operating conditions provided in Table 3 are met.

**FIGURE 1: POSC CRYSTAL CIRCUIT**

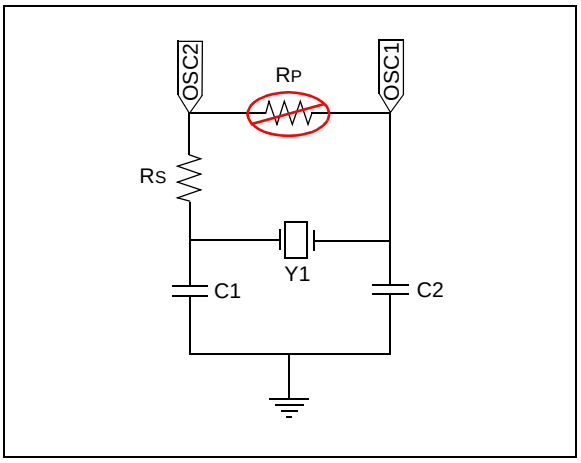


**TABLE 1: CRYSTAL SPECIFICATIONS**

| Crystal Frequency (see Note 1) | Series Resistor Rs | Posc Gain Setting POSCGAIN<1:0> (DEVCFG0<20:19> | Posc Boost Setting POSCBOOST (DEVCFG0<21> |
|---|---|---|---|
| 8 MHz | 2 kΩ | '0b00 (GAIN_0) | '0b1 |
| 12 MHz | 1 kΩ | '0b00 (GAIN_0) | '0b1 |
| 24 MHz(3) | 0 | '0b00 (GAIN_0) | '0b1 |

**Note 1:** Using any other crystal frequency will require special component selection and characterization.

**2:** A parallel resistor (RP) should not be used to increase the gain of the POSC.

**3:** Only 24 MHz crystals with a Mfg ESR ≤ 40Ω.

**Work around 2**

Alternatively, use an external clock or the Internal FRC Oscillator. Communication interfaces, such as CAN, USB, etc., with tighter clock accuracy requirements will not function with the FRC as clock source.

**Affected Silicon Revisions**

| A1 | A2 | | | | | | |
|---|---|---|---|---|---|---|---|
| X | X | | | | | | |

## 2. Module: Secondary Oscillator

A crystal oscillator cannot be used as the input to the Secondary Oscillator (SOSC) pins, SOSCI and SOSCO.

**Work around**

Use an external clock source (32,768 Hz) applied to the SOSCO pin with the FSOSCEN bit (DEVCFG1<6>) set to '0' (i.e., the SOSC pin is disabled through the Configuration Word) for a real-time clock base; otherwise, use the internal LPRC for non-precision requirements.

**Affected Silicon Revisions**

| A1 | A2 | | | | | | |
|---|---|---|---|---|---|---|---|
| X | X | | | | | | |

### 3. Module: Clocks

The PB6DIV<6:0> (i.e., PBDIV<6:0> bits), default to ‘0b0000001 (1:2) instead of ‘0b0000011 (1:4). The max clock rate supported for the PBCLK6 bus is 30 MHz.

**Work around**

Set the PBDIV<6:0> bits = ‘0b0000011 (i.e., 1:4) assuming a 120 MHz SYSCLK. This is a register that requires an unlock sequence.

**Affected Silicon Revisions**

| A1 | A2 | | | | | | |
|---|---|---|---|---|---|---|---|
| X | X | | | | | | |

### 4. Module: FSCM

When the FCKSM<1:0> bits (DEVCFG1<15:14>) = ‘0b1x, clock fail monitoring is enabled, and a clock fail is detected. The SYSCLK source switches to the LPRC instead of the FRC as intended.

**Work around**

If the user has clock software clock switching enabled, FCKSM<1:0> = ‘0b11, they can perform a software clock switch to the FRC instead.

**Affected Silicon Revisions**

| A1 | A2 | | | | | | |
|---|---|---|---|---|---|---|---|
| X | X | | | | | | |

### 5. Module: VBAT

The VBAT pin is non-functional and it must be connected to VDD.

**Work around**

None.

**Affected Silicon Revisions**

| A1 | A2 | | | | | | |
|---|---|---|---|---|---|---|---|
| X | X | | | | | | |

### 6. Module: VBAT

RTCC may lose Sosc clocks momentarily during a VDD to VBAT switch over event.

**Work around**

None.

**Affected Silicon Revisions**

| A1 | A2 | | | | | | |
|---|---|---|---|---|---|---|---|
| X | X | | | | | | |

### 7. Module: ADC

The ADC level trigger, ADCTRGx register = ‘0b00010, will not perform burst conversions in Debug mode.

**Work around**

Do not use Debug mode with the ADC level triggers.

**Affected Silicon Revisions**

| A1 | A2 | | | | | | |
|---|---|---|---|---|---|---|---|
| X | X | | | | | | |

### 8. Module: ADC

Turbo mode, TRBEN bit (ADCCON1<31>) = 1, is not functional when two channels are linked for increasing effective throughput.

**Work around**

The user can still increase the effective throughput rate by interleaving ADC cores and trigger sources by connecting multiple dedicated high-speed ADCs to the same analog input and staggering the respective ADCx core triggers appropriately.

**TABLE 2: INTERLEAVED ADC PERFORMANCE VDD > 2.5V**

| Number of Interleaved ADC (12-bit mode) | Minimum TAD Sampling Time (SAMC) | Maximum Effective Sampling Rate (in Msps) |
|---|---|---|
| 2 | 13 | 4.615 |
| 3 | 7 | 8.57 |
| 4 | 5 | 12 |
| 5 | 4 | 15 |
| 6 | 3 | 20 |

**Affected Silicon Revisions**

| A1 | A2 | | | | | | |
|---|---|---|---|---|---|---|---|
| X | X | | | | | | |

### 9. Module: ADC

In Differential mode, code 3072 has a DNL of +3.

**Work around**

None.

**Affected Silicon Revisions**

| A1 | A2 | | | | | | |
|---|---|---|---|---|---|---|---|
| X | X | | | | | | |

### 10. Module: ADC

ADC input AN26 is not functional.

**Work around**

None.

**Affected Silicon Revisions**

| A1 | A2 | | | | | | |
|---|---|---|---|---|---|---|---|
| X | X | | | | | | |

### 11. Module: ADC

Scan list conversions defined in the ADCCSS1 register will restart without finishing the current scan list and do not generate an EOSRDY bit (ADCCON2<29>) end of scan interrupt status if a new trigger event from the STRGSRC<4:0> bits (ADCCON1<20:16>) trigger source occurs before the scan list completion on the shared ADC7 core.

**Work around**

Ensure that the STRGSRC<4:0> bits trigger source repetition rate > (sample + conversion) times of the sum of all ANx inputs defined in the ADCCSS1/ADCCSS2 registers.

**Affected Silicon Revisions**

| A1 | A2 | | | | | | |
|---|---|---|---|---|---|---|---|
| X | X | | | | | | |

### 12. Module: ADC

Shared ADC7 has high Offset and Gain Error up to 38 Lsb in ADC7 Scan mode, as defined in the ADCCSS1/ADCCSS2 registers.

**Work around**

Increase the user-defined SAMC<9:0> bits (ADCCON2<25:16>) sample time register value by 4 TAD. This will reduce the ADC7 throughput that the user must consider, but it will reduce the gain and offset to less than 4 Lsb in 12-bit mode.

**Affected Silicon Revisions**

| A1 | A2 | | | | | | |
|---|---|---|---|---|---|---|---|
| X | X | | | | | | |

### 13. Module: Op amp

Enabling the Op amp Output Enable bit, OAO (CMxCON<11>) = 1, disables the respective Comparator's output pin function, CxOUT, on a different pin entirely if it was enabled, COE bit (CMxCON<14>); however, the Comparator Output Status is still functional.

**Work around**

None. The same Op amp/Comparator outputs cannot be enabled simultaneously.

**Affected Silicon Revisions**

| A1 | A2 | | | | | | |
|---|---|---|---|---|---|---|---|
| X | X | | | | | | |

### 14. Module: Op amp

When the AMPMOD bit (CMxCON<10>) = 1 (the Op amp is enabled), the Op amp output pin is active regardless of the state of the OAO bit (CMxCON<11>) Op amp output pin enable.

**Work around**

If the user does not want the Op amp output pin to be active, do not enable the Op amp until required.

**Affected Silicon Revisions**

| A1 | A2 | | | | | | |
|---|---|---|---|---|---|---|---|
| X | X | | | | | | |

### 15. Module: Op amp

When used in 1x Unity Gain Buffer mode, an Op amp continues to function despite being disabled, (i.e., AMPMOD bit (CMxCON<10>) = 0.

**Work around**

None.

**Affected Silicon Revisions**

| A1 | A2 | | | | | | |
|---|---|---|---|---|---|---|---|
| X | X | | | | | | |

### 16. Module: Op amp

Op amps in Unity Gain mode (i.e., ENPGAx bit (CFGCON2<20, 18, 17, 16>) = 1) are non-functional.

**Work around**

Do not use Op amp Unity Gain mode or use external 8x resistor signal attenuation network to Op amp input and then use op amp with 8x gain for net 1x signal gain.

**Affected Silicon Revisions**

| A1 | A2 | | | | | | |
|---|---|---|---|---|---|---|---|
| X | X | | | | | | |

### 17. Module: Op amp

Op amp minimum PSRR electrical spec is -39 db versus -75 db typical.

**Work around**

None.

**Affected Silicon Revisions**

| A1 | A2 | | | | | | |
|---|---|---|---|---|---|---|---|
| X | X | | | | | | |

### 18. Module: Op amp

Op amps do not meet common mode voltage range specification between 0.4V-0.9V, where CMRR is reduced to < 28 db.

**Work around**

None.

**Affected Silicon Revisions**

| A1 | A2 | | | | | | |
|---|---|---|---|---|---|---|---|
| X | X | | | | | | |

### 19. Module: Op amp

Op amps CMRR is < 28 db at input common mode voltages between 0.4V-0.9V, which is less than the electrical specification of 70 db minimum.

**Work around**

None.

**Affected Silicon Revisions**

| A1 | A2 | | | | | | |
|---|---|---|---|---|---|---|---|
| X | X | | | | | | |

### 20. Module: Op amp

Op amps do not meet the typical gain margin specification of 20, but are instead 15.

**Work around**

None.

**Affected Silicon Revisions**

| A1 | A2 | | | | | | |
|---|---|---|---|---|---|---|---|
| X | X | | | | | | |

### 21. Module: DAC

DACs when sourcing $I_{OUT(MAX)}$ = -1.5 mA, do not meet INL ±4 Lsb specification when $AV_{DD}$ < 3.0V. and $T_A$ > 85ºC.

**Work around**

Do not use DACs to source > -0.75 mA at 2.6V < $AV_{DD}$ < 3.0V.

**Affected Silicon Revisions**

| A1 | A2 | | | | | | |
|---|---|---|---|---|---|---|---|
| X | X | | | | | | |

### 22. Module: DAC

DACs do not meet DNL -1 Lsb min specification when $AV_{DD}$ < 3.0V. Worst case is -1.5 Lsb at 2.2V.

**Work around**

None.

**Affected Silicon Revisions**

| A1 | A2 | | | | | | |
|---|---|---|---|---|---|---|---|
| X | X | | | | | | |

### 23. Module: Timer1

Timer1 in Asynchronous External Counter mode, (i.e., TCS bit (T1CON<1> = 1, TSYNC bit (T1CON<2> = 0, and TECS<1:0> bits (T1CON<9:8>) are greater than '0b01) does not reflect the first count from an external T1CK input.

**Work around**

None.

**Affected Silicon Revisions**

| A1 | A2 | | | | | | |
|---|---|---|---|---|---|---|---|
| X | X | | | | | | |

### 24. Module: Timer1

The TMR1 register of Timer1 in Asynchronous mode (i.e., TCS bit (T1CON<1> = 1, TSYNC bit (T1CON<2> = 0, and TECS<1:0> bits (T1CON<9:8>) are greater than '0b01), remains at initial set value for 5 external clock pulses after wake up from Sleep mode

**Work around**

None.

**Affected Silicon Revisions**

| A1 | A2 | | | | | | |
|---|---|---|---|---|---|---|---|
| X | X | | | | | | |

### 25. Module: Timer1

Back-to-back writes to the TMR1 register are not allowed for four PBCLK2 cycles.

**Work around**

Wait for four PBCLK2 cycles before attempting a second write to the TMR1 register.

**Affected Silicon Revisions**

| A1 | A2 | | | | | | |
|---|---|---|---|---|---|---|---|
| X | X | | | | | | |

### 26. Module: I/O

If the I/O function is configured for RTCC alarm output driver, it does not return to default/Reset input high–Z state on wake-up from Deep Sleep mode through MCLR.

**Work around**

None.

**Affected Silicon Revisions**

| A1 | A2 | | | | | | |
|---|---|---|---|---|---|---|---|
| X | X | | | | | | |

### 27. Module: Deep Sleep

Deep-Sleep mode is non-functional.

**Work around**

None.

**Affected Silicon Revisions**

| A1 | A2 | | | | | | |
|---|---|---|---|---|---|---|---|
| X | X | | | | | | |

### 28. Module: RCON

The RCON register status bits, VBPOR, PORIO, PORCORE, and VBAT, are inconsistent and cannot be used.

**Work around**

None.

**Affected Silicon Revisions**

| A1 | A2 | | | | | | |
|---|---|---|---|---|---|---|---|
| X | X | | | | | | |

### 29. Module: Sleep

If the ON bit (PB5DIV<15>) = 0, and PBCLK5 is disabled, there is a 3 mA increase in Sleep $I_{PD}$ current.

**Work around**

Do not disable PBCLK5 before entering Sleep mode.

**Affected Silicon Revisions**

| A1 | A2 | | | | | | |
|---|---|---|---|---|---|---|---|
| X | X | | | | | | |

### 30. Module: Sleep

There is a 170 µA increase in Sleep $I_{PD}$ current if USB pins D+ and D- are unused and left floating.

**Work around**

Add 50k pull-downs on D+ and D-, and tie $V_{USB3V3}$ to $V_{DD}$.

**Affected Silicon Revisions**

| A1 | A2 | | | | | | |
|---|---|---|---|---|---|---|---|
| X | X | | | | | | |

### 31. Module: PMP

The PMP Input Buffer 'x' Status Full bit, IB0F (PMSTAT<8>), and Output Buffer Underflow Status bit, OBUF (PMSTAT<6>), are set as soon as the PMP is turned ON in Slave mode, when TTLEN = 1.

**Work around**

After PMP initial initialization is complete, and before PMP and interrupts are enabled, clear these bits in user software.

**Affected Silicon Revisions**

| A1 | A2 | | | | | | |
|---|---|---|---|---|---|---|---|
| X | X | | | | | | |

### 32. Module: PMP

CS is deasserting before RD in Slave mode. Slave mode is defeatured.

**Work around**

None.

**Affected Silicon Revisions**

| A1 | A2 | | | | | | |
|---|---|---|---|---|---|---|---|
| X | X | | | | | | |

### 33. Module: CTMU

Edge Sequencing mode, (EDGSEQEN bit (CTMUCON<2>)), and Edge mode are not functional.

**Work around**

Use level modes.

**Affected Silicon Revisions**

| A1 | A2 | | | | | | |
|---|---|---|---|---|---|---|---|
| X | X | | | | | | |

### 34. Module: CTMU

When the TGEN bit is set, manual current sourcing (i.e., setting the EDG1STAT bit) from the CTMU is not possible.

**Work around**

None.

**Affected Silicon Revisions**

| A1 | A2 | | | | | | |
|---|---|---|---|---|---|---|---|
| X | X | | | | | | |

### 35. Module: ICAP

Debug breakpoints are not supported when using Input Capture with DMA.

**Work around**

None.

**Affected Silicon Revisions**

| A1 | A2 | | | | | | |
|---|---|---|---|---|---|---|---|
| X | X | | | | | | |

### 36. Module: PWM

Leading edge blanking in XPRES mode, XPRES bit (PWMCONx<2>) = 1, is not functional.

**Work around**

None.

**Affected Silicon Revisions**

| A1 | A2 | | | | | | |
|---|---|---|---|---|---|---|---|
| X | X | | | | | | |

### 37. Module: PWM

The PWM module does not relinquish control of the PWM pins even if they are not enabled, (i.e., PENH bit (IOCONx<15>) = 0 and PENL bit (IOCON<14>) = 0).

**Work around**

Disable corresponding unused user PWM channels by setting the appropriate PWMxMD bit in the PMD4 register = 1.

**Affected Silicon Revisions**

| A1 | A2 | | | | | | |
|---|---|---|---|---|---|---|---|
| X | X | | | | | | |

### 38. Module: PWM

Leading-edge Blanking (LEB) trigger is not applied at the correct time if dead time is enabled. The trigger is applied before the dead time when it should be applied after the dead time to coincide with the actual dead time delayed PWM signal transition.

**Work around**

Make the leading edge blanking time LEBDLYx<11:0> (i.e., LED<11:0> bits) equal to the desired leading edge blanking time, and the respective dead time value

**Affected Silicon Revisions**

| A1 | A2 | | | | | | |
|---|---|---|---|---|---|---|---|
| X | X | | | | | | |

### 39. Module: PWM

Multiple PWM Interrupts occur for single TRGIF, PWMLIF, and PWMHIF interrupt events. The ISR is re-executed multiple times if the PWM prescaler bits (PTCON<6:4>) (i.e., PCLKDIV<2:0>) or SCLKDIV<2:0> bits (i.e. STCON<6:4>) are greater than 5.

**Work around**

Insure that the PCLKDIV<2:0> bits and the STCON< 2:0> bits are less than 5.

**Affected Silicon Revisions**

| A1 | A2 | | | | | | |
|---|---|---|---|---|---|---|---|
| X | X | | | | | | |

### 40. Module: UART

A UART Transmit Interrupt (UTXISEL<1:0> bits (UxSTA<15:14>) = ‘0b00) is generated and asserted while the transmit buffer contains at least one empty space and the UART Receiver Interrupt Flag bit (URXISEL<1:0> bits (UxSTA<7:6>) = ‘0b00) is asserted while the receive buffer is not empty and non-functional.

**Work around**

None.

**Affected Silicon Revisions**

| A1 | A2 | | | | | | |
|---|---|---|---|---|---|---|---|
| X | X | | | | | | |

### 41. Module: UART

A UART Transmit Interrupt (UTXISEL<1:0> bits = ‘0b01) is generated but does not remain asserted when all of the characters have been transmitted. Once the IFSx bit is cleared by the user, it does not remain asserted even while all characters have been transmitted. This behavior compounded with finite interrupt latency can create a race condition amongst subsequent TX interrupts.

**Work around**

To avoid the race condition, clear the UARTx IFSx flag before writing a new value to the TX Buffer, UxTXREG, in the ISR.

**Affected Silicon Revisions**

| A1 | A2 | | | | | | |
|---|---|---|---|---|---|---|---|
| X | X | | | | | | |

### 42. Module: UART

UART Transmit UTXISEL<1:0> bits = ‘0b10 Interrupt is generated but does not remain asserted while the transmit buffer is empty. Once the IFS bit is cleared by the user, it does not remain asserted even while transmit buffer is empty. This behavior compounded with finite interrupt latency can create a race condition amongst subsequent TX interrupts.

**Work around**

To avoid the race condition, clear the UARTx IFS flag before writing a new value to the TX Buffer, UxTXREG, in the ISR.

**Affected Silicon Revisions**

| A1 | A2 | | | | | | |
|---|---|---|---|---|---|---|---|
| X | X | | | | | | |

### 43. Module: UART

The UART Receive Interrupt Flag (URXISEL<1:0> bits = ‘0b01) is asserted only when the receive buffer equals one-half full and not when the receive buffer is greater than one-half full.

**Work around**

Before exiting the UART RX ISR, ensure all the contents of the RX Buffer have been read, by reading the contents of the RX Buffer in the ISR until the URXDA bit (UxSTA<0>) is cleared.

**Affected Silicon Revisions**

| A1 | A2 | | | | | | |
|---|---|---|---|---|---|---|---|
| X | X | | | | | | |

### 44. Module: UART

The UART Receive Interrupt Flag bit (URXISEL<1:0> bits = ‘0b10) is asserted only when the receive buffer equals three-quarters full and not when the receive buffer is greater than three-quarters full.

**Work around**

Before exiting the UART RX ISR, ensure the entire contents of the RX Buffer have been read by reading the contents of RX Buffer in the ISR until the URXDA bit (UxSTA<10>) bit is cleared.

**Affected Silicon Revisions**

| A1 | A2 | | | | | | |
|---|---|---|---|---|---|---|---|
| X | X | | | | | | |

### 45. Module: UART

The UART TX Stop bit duration is shorter than the expected in High-Speed mode (BRGH (UxMODE<3>) = 1) for baud rates less than 7.5 MBPS.

**Work around**

For baud rates less than 7.5 MBPS, operate the UART in Standard-Speed mode, that is, BRGH (UxMODE<3>) =0. For baud rates greater than 7.5 MBPS operate the UART in High-Speed mode, that is. BRGH (UxMODE<3>) =1.

**Affected Silicon Revisions**

| A1 | A2 | | | | | | |
|---|---|---|---|---|---|---|---|
| X | X | | | | | | |

### 46. Module: CAN

The CAN Wake Interrupt Flag bit, WAKIF (CxINT<14>), is set even when the CAN module is disabled.

**Work around**

During CAN initialization, and before enabling the CAN peripheral, clear the WAKIF bit in user code.

**Affected Silicon Revisions**

| A1 | A2 | | | | | | |
|---|---|---|---|---|---|---|---|
| X | X | | | | | | |

### 47. Module: Deadman Timer (DMT)

The Deadman Timer module does not cause a Non-maskable Interrupt (NMI) on a BAD1, BAD2, or DMTEVENT.

**Work around**

None.

**Affected Silicon Revisions**

| A1 | A2 | | | | | | |
|---|---|---|---|---|---|---|---|
| X | X | | | | | | |

### 48. Module: Watchdog Timer (WDT)

Multiple valid key writes can be performed outside the Watchdog Timer window before a Reset occurs instead of the required single write.

**Work around**

None.

**Affected Silicon Revisions**

| A1 | A2 | | | | | | |
|---|---|---|---|---|---|---|---|
| X | X | | | | | | |

### 49. Module: ICSP

Regardless of other functions shared on the TDO pin, the TDO function becomes an active output and toggles while programming on any ICSP PGECx/PGEDx pair.

**Work around**

None.

**Affected Silicon Revisions**

| A1 | A2 | | | | | | |
|---|---|---|---|---|---|---|---|
| X | X | | | | | | |

### 50. Module: $V_{IH}$

$V_{IH(MIN)}$ does not meet the electrical specification of (0.65 * $V_{DD}$), but is instead $V_{IH(MIN)}$ = (0.8 * $V_{DD}$).

**Work around**

Although $V_{IH}$ is greater than $V_{OH(MIN)}$ = 2.4V, $V_{OH(MIN)}$ is a function of $I_{OH(MAX)}$. If the application does not load the $V_{IH}$ input source signal by more than $I_{OH(MAX)}$ by 50%, there should be no issues.

**Affected Silicon Revisions**

| A1 | A2 | | | | | | |
|---|---|---|---|---|---|---|---|
| X | X | | | | | | |

### 51. Module: Cache

A Data Bus Error Exception can occur when prefetch cache is enabled, (PREFEN<1:0>) bits (CHECON<5:4> = `'0b01`).

**Work around**

Users must ensure that predictive prefetch cache is disabled by setting the PREFEN<1:0> bits = `'0b00`.

**Affected Silicon Revisions**

| A1 | A2 | | | | | | |
|---|---|---|---|---|---|---|---|
| X | | | | | | | |

### 52. Module: BOR

On a BOR event, and when the BORSEL bit (DEVCFG2<29>) = `0`, the POR Status bit (RCON<0>) may also be erroneously set.

**Work around**

None.

**Affected Silicon Revisions**

| A1 | A2 | | | | | | |
|---|---|---|---|---|---|---|---|
| X | X | | | | | | |

## 53. Module: BOR

On a BOR event, $V_{POR} < V_{DD} < V_{BOR}$, a Reset is not generated when the BOR threshold is reached. System clocks will stop with all I/O pins functions frozen in their present state until either $V_{DD}$ falls to $V_{POR}$ or $V_{DD}$ returns to above $V_{BOR}$. The user must assess if this $V_{DD}$ brown-out condition and the resulting frozen I/O pin state has an adverse effect on their application (UART, PWM, I/O, OC, etc.).

**Work around 1**

Use an external Reset supervisor/monitor (see Figure 2). Some LDO regulators, as listed in Table 6, have an embedded reset supervisor included. The required minimum reset trip voltage of the supervisor should be at least ($V_{BOR}$ + 0.5V) with the SMCLR bit (DEVCFG0<15>) = 0 and the BORSEL bit (DEVCFG2<29>) = 1 in the Configuration Words. This means that the minimum $V_{DD}$ operating voltage of the application needs to be above the reset supervisor maximum trip voltage at [Reset Trip (max) + 0.2V], (i.e. Application $V_{DD(MIN)}$ = ~($V_{BOR}$ + 0.5V + 0.2V). The reset supervisor should have an open drain output so as not to interfere with the MPLAB programming/debug tools. This workaround assures that MCLR will generate an internal POR and reset the I/O pins before the $V_{BOR}$ trip point.

| **Note:** | For Motor Control applications utilizing the PWM module, **only Work around 1 is recommended**. |
|---|---|

**Work around 2**

If the application can sustain frozen I/O states for ~2.1 ms (UART, CAN, I/O, etc.), the application must enable the Deep Sleep Watchdog Timer and Clock Fail Monitor, based on the details provided in Table 5 and Table 6. If implemented correctly, after ~2.1 ms, a valid internal reset state is entered and the I/O pins are set to the device default Reset state.

**FIGURE 2: RESET SUPERVISOR CIRCUIT**

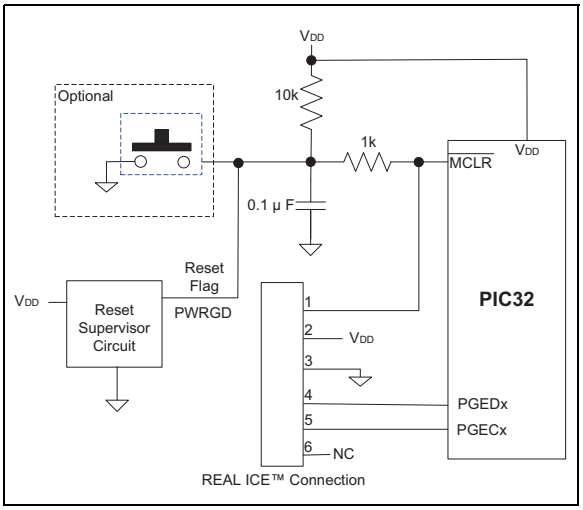


**TABLE 3: RESET SUPERVISOR/ VOLTAGE MONITOR**

| Part Number | Reset Trip | CPU $\overline{\text{MCLR}}$ Source |
|---|---|---|
| MIC803-26D2VC3 | 2.63v | Reset pin (Open Drain) |

**TABLE 4: LDO REGULATORS WITH EMBEDDED RESET SUPERVISOR**

| Part Number | Topology | $V_{IN(MAX)}$ | $V_{OUT}$ | $I_{OUT}$ | Reset Trip | CPU $\overline{\text{MCLR}}$ Source |
|---|---|---|---|---|---|---|
| MIC5239-3.3YM | LDO | 30V | 3.3V | 500mA | 3.3V-5% | FLG pin (Open Drain) |
| MIC5239-3.3YMM | | | | | | |
| MCP1725-3302E/MC | LDO | 6V | 3.3V | 500mA | 3.3V-10% | PWRGD pin (Open Drain) |
| MCP1727-3302E/MF | LDO | 6V | 3.3V | 1500mA | 3.3V-10% | PWRGD pin (Open Drain) |

**Affected Silicon Revisions**

| A1 | A2 | | | | | | |
|---|---|---|---|---|---|---|---|
| X | | | | | | | |

### 54. Module: SPI2

Reading the SPI2 SS2R PPS register will return indeterminate results. Therefore, also avoid using bit instruction of the form SS2Rbits.SS2R, as it is a read-modify-write command, which will corrupt the register value. Writes to the register or bit SET, CLR, or INV will function as expected.

**Work around**

Only use register write instruction forms to this register.

**Affected Silicon Revisions**

| A1 | A2 | | | | | | |
|---|---|---|---|---|---|---|---|
| X | X | | | | | | |

### 55. Module: DMA

A simultaneous access by the CPU and the DMA controller to the same peripheral bus may result in bus conflict and cause the CPU to stall indefinitely until a Reset. For example, if the CPU is accessing the TMR2 which is located on peripheral bus 2, then a DMA access to any peripheral on peripheral bus 2, such as UART1, may result in a bus conflict and cause the CPU to stall indefinitely until a Reset. See Figure 1-1 “PIC32MK GP/MC Family Block Diagram” in the data sheet to determine which peripherals share the same peripheral bus.

This issue is limited to the CPU and the DMA controller accessing the same peripheral bus only. There are no bus conflict issues when the CPU and the DMA controller are simultaneously accessing SRAM memory. Furthermore, peripherals such as, ADC, CAN and USB OTG which have their independent DMA capabilities are not impacted by this issue as long as the destination is SRAM memory.

**Work around**

Avoid simultaneous CPU and DMA access to the same peripheral bus. If there is a possibility of an ongoing DMA transfer, ensure that the DMA transfers on that peripheral bus are disabled before the CPU attempts to access that peripheral bus. This includes interrupt service routines during which the CPU is attempting access to the interrupting peripheral on the same peripheral bus where there is a possibility of an ongoing DMA transfer.

**Affected Silicon Revisions**

| A1 | A2 | | | | | | |
|---|---|---|---|---|---|---|---|
| X | X | | | | | | |

## Data Sheet Clarifications

The following typographic corrections and clarifications are to be noted for the latest version of the device data sheet (DS60001402**D**):

| | |
|---|---|
| **Note:** | Corrections are shown in **bold**. Where possible, the original bold text formatting has been removed for clarity. |

### 1. Module: BOR Event Voltage

The minimum BOR event on VDD transition high-to-low voltage value, defined in parameter BO1a for OPAxMD bit (PMD2) = 0 in **Table 36-5 Electrical Characteristics: BOR** was incorrectly stated. The correct value is shown in the following table.

**TABLE 36-5: ELECTRICAL CHARACTERISTICS: BOR**

| DC CHARACTERISTICS | | | Standard Operating Conditions: 2.2V to 3.6V (unless otherwise stated)<br>Operating temperature -40°C ≤ TA ≤ +85°C for Industrial<br>-40°C ≤ TA ≤ +125°C for Extended | | | | |
|---|---|---|---|---|---|---|---|
| Param. No. | Symbol | Characteristics | Min. | Typ. | Max. | Units | Conditions |
| BO10a | VBOR | BOR Event on VDD transition high-to-low (Note 2) | **2.735** | — | 2.880 | V | If any OPAxMD bit (PMD2) = 0 (OPAMPx Enb) |
| | | | 2.010 | — | 2.129 | V | If all OPAxMD bits (PMD2) = 1 (By default, all OP amps are disabled on any reset) |

**Note 1:** Parameters are for design guidance only and are not testing in manufacturing.

**2:** Overall functional device operation at VBORMIN < VDD < VDDMIN is tested, but not characterized. All device Analog modules, such as ADC and so on., will function but with degraded performance below VDDMIN.

## APPENDIX A: REVISION HISTORY

Rev A Document (3/2017)

Initial release of this document issued for Revision A1 silicon, which includes silicon issues 1. (Primary Oscillator), 2. (Secondary Oscillator), 3. (Clocks), 4. (FSCM), 5. (VBAT), 6. (VBAT), 7. (ADC), 8. (ADC), 9. (ADC), 10. (ADC), 11. (ADC), 12. (ADC), 13. (Op amp), 14. (Op amp), 15. (Op amp), 16. (Op amp), 17. (Op amp), 18. (Op amp), 19. (Op amp), 20. (Op amp), 21. (DAC), 22. (DAC), 23. (Timer1), 24. (Timer1), 25. (Timer1), 26. (I/O), 27. (Deep Sleep), 28. (RCON), 29. (Sleep), 30. (Sleep), 31. (PMP), 32. (PMP), 33. (CTMU), 34. (CTMU), 35. (ICAP), 36. (PWM), 37. (PWM), 38. (PWM), 39. (PWM), 40. (UART), 41. (UART), 42. (UART), 43. (UART), 44. (UART), 45. (Temperature Sensor), 46. (CAN), 47. (Deadman Timer (DMT)), 48. (WDT), 49. (ICSP), 50. (VIH), 51. (Cache), 52. (BOR), 53. (BOR).

Rev B Document (7/2017)

Updated silicon issue 45. to Reserved.

Added Data Sheet Clarifications: 1. (BOR Event Voltage), 2. (Deep Sleep Max Current), 3. (CTMU Temperature Sensor Graph), (The minimum BOR event on VDD transition high-to-low voltage value, defined in parameter BO1a for).

Rev C Document (9/2017)

Updated for Revision A2 silicon.

Added silicon issue 54. (SPI2).

Rev D Document (4/2018)

Add Silicon Issues 45. (UART) and 55. (DMA).

Added Data Sheet Clarifications: (The minimum BOR event on VDD transition high-to-low voltage value, defined in parameter BO1a for).

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