

LTC2500-32/LTC2508-32/LTC2512-24: 32-Bit/24-Bit Oversampling ADCs with Configurable Digital Filter

DESCRIPTION

Demonstration circuit 2222A features the [LTC®2500-32](#), [LTC2508-32](#) and [LTC2512-24](#) ADCs. The LTC2500-32, LTC2508-32 and LTC2512-24 are low power, low noise, high speed, 32-bit/24-bit SAR ADCs with an integrated configurable digital averaging filter that operate from a single 2.5V supply. The following text refers to the LTC2508-32 but applies to all parts, the only difference being sample rate and number of bits. The DC2222A demonstrates the DC and AC performance of the LTC2508-32 in conjunction with the DC590 or DC2026 QuikEval™ and DC890 PScope™ data collection boards. Use the DC590 or DC2026 to demonstrate DC performance such as peak-to-peak noise

and DC linearity. Use the DC890 if precise sampling rates are required or to demonstrate AC performance such as SNR, THD, SINAD and SFDR. The DC2222A is intended to show recommended grounding, component placement and selection, routing and bypassing for this ADC.

Design files for this circuit board including the schematic, BOM and layout are available at <http://www.linear.com/demo/DC2222A> or scan the QR code on the back of the board.

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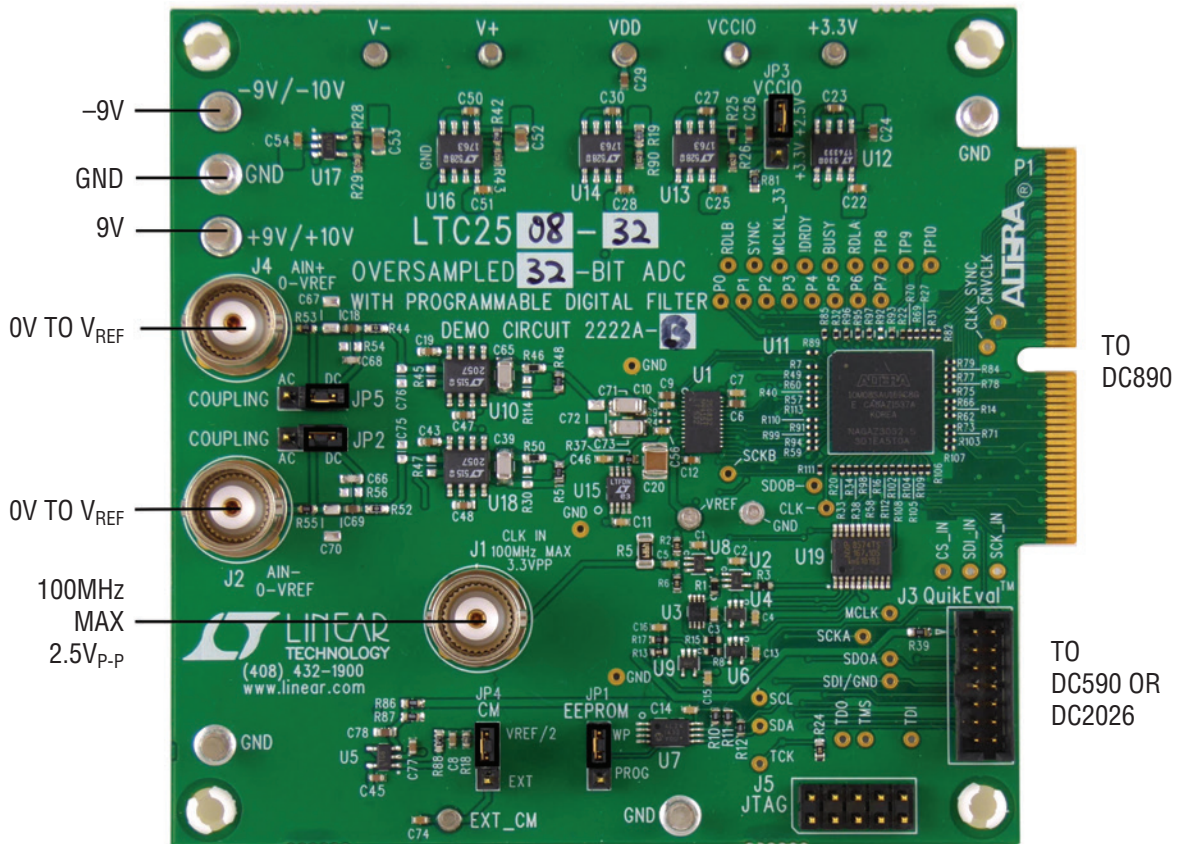


Figure 1. DC2222A Connection Diagram

QUICK START PROCEDURE

Table 1. DC2222A Assembly and Clock Options

ASSEMBLY VERSION	U1 PART NUMBER	MAX OUTPUT DATA RATE	DF	BITS	MAX CLK IN FREQ	OUTPUT	MODE	DIVIDER
DC2222A-A	LTC2500IDKD-32	175ksps	4	32	70MHz	A	No Verify	100
		173ksps	4	32	70MHz	A	Verify	101
		250ksps	4	32	43MHz	A	Distributed Read	43
		250ksps	4	32	45MHz	A	Verify + Dis. Read	45
		800ksps	1	24	80MHz	B		100
DC2222A-B	LTC2508IDKD-32	3.472ksps	256	32	80MHz	A	No Verify	90
		2.900ksps	256	32	75MHz	A	Verify	101
		3.906ksps	256	32	43MHz	A	Distributed Read	43
		3.906ksps	256	32	45MHz	A	Verify + Dis. Read	45
		900ksps	1	14	90MHz	B		100
DC2222A-C	LTC2512IDKD-24	350.877ksps	4	24	80MHz	A	No Verify	57
		303.03ksps	4	24	80MHz	A	Verify	66
		400ksps	4	24	62.4MHz	A	Distributed Read	39
		400ksps	4	24	70.4MHz	A	Verify + Dis. Read	44
		1.5Msps	1	14	85.5MHz	B		57

Check to make sure that all jumpers are set as described in the DC2222A Jumpers section. In particular, make sure that VCCIO (JP3) is set to the 2.5V position. Controlling the DC2222A with the DC890 while JP3 of the DC2222A is in the 3.3V position will cause noticeable performance degradation in SNR and THD. The default jumper connections configure the ADC to use the onboard reference and regulators. The analog input is DC coupled by default. Connect the DC2222A to a DC890 USB High Speed Data Collection Board using connector P1. (Do not connect a PScope controller and QuikEval controller at the same time.) Next, connect the DC890 to a host PC with a standard USB A/B cable. Apply $\pm 9V$ to the indicated terminals. Next apply a low jitter differential sine source to J2 and J4. Connect a low jitter 2.5V_{P-P} sine wave or square wave to connector J1, using Table 1 as a guide for the appropriate clock frequency. Note that J1 has a 49.9 Ω termination resistor to ground.

Run the PScope software (PScope.exe version K86 or later) supplied with the DC890 or download it from www.linear.com/software.

Complete software documentation is available from the Help menu. Updates can be downloaded from the Tools menu. Check for updates periodically as new features may be added.

The PScope software should recognize the DC2222A and configure itself automatically. The default setup is to read the filtered output with Verify and Distributed Read not selected and the Down Sampling Factor (DF) set to the smallest possible value. To change this, click on the Set Demo Bd Options setting of the PScope Tool Bar as shown in Figure 2. The Configuration Options box shown in Figures 3a, 3b and 3c allows the ADC output, DF, Verify and Distributed Read to be set. In the case of the LTC2500 it is also possible to select the filter type, gain compression and gain expansion. If Verify is not selected then the

QUICK START PROCEDURE

minimum number of bits will be clocked out. If Verify is selected the number of bits clocked out is increased by eight which includes the number of samples taken for the current output. Distributed Read allows a slower clock to be used by spreading the data clocked out over a number of samples. DF can be set over a wide range which is determined by the device in use. Increasing DF will improve the SNR. Theoretically, SNR will improve by

6dB if the down sampling factor is increased by a factor of four. In practice, reference noise will eventually limit the SNR improvement. Increasing the REF bypass capacitor (C20) or using a lower noise external reference will extend this limit.

Click the Collect button (See Figure 4) to begin acquiring data. The Collect button then changes to Pause, which can be clicked to stop data acquisition.



Figure 2. PScope Toolbar

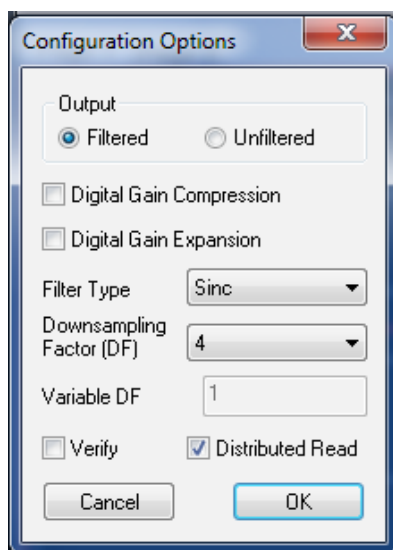


Figure 3a. LTC2500 Configuration Options Menu

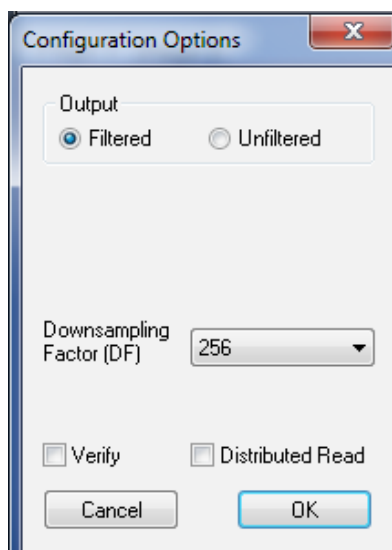


Figure 3b. LTC2508 Configuration Options Menu

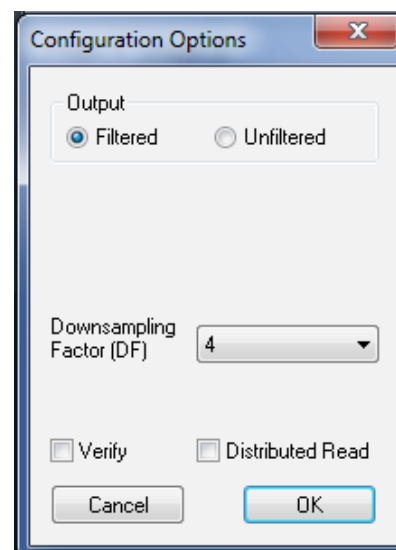


Figure 3c. LTC2512 Configuration Options Menu

QUICK START PROCEDURE

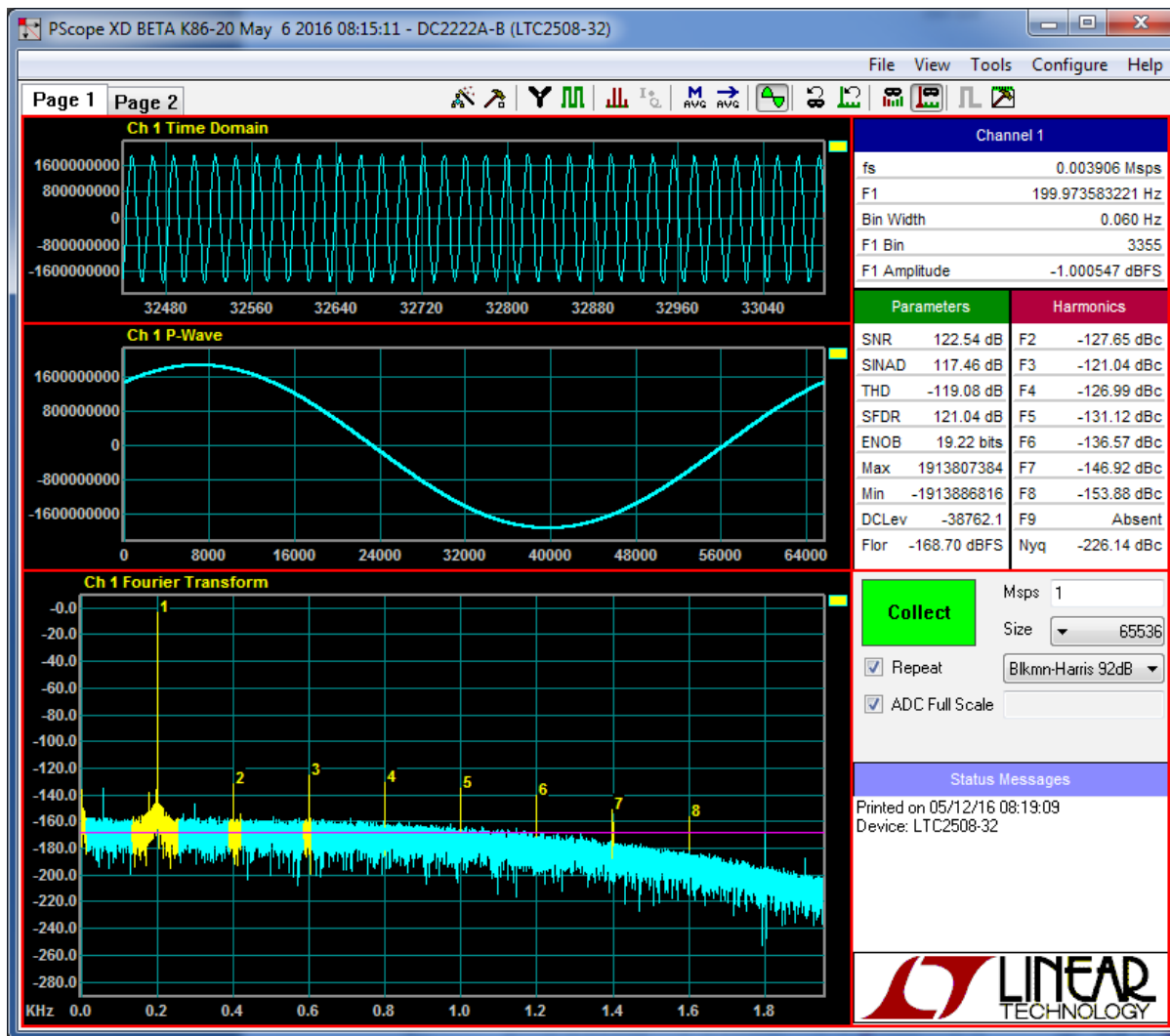


Figure 4. PScope Screen Shot

DC590 OR DC2026 QUICK START PROCEDURE

IMPORTANT! To avoid damage to the DC2222A, make sure that JP6 of the DC590 or JP3 of the DC2026 is set to 3.3V before connecting to the DC2222A.

VCCIO (JP3) of the DC2222A should be in the 3.3V position for DC590 or DC2026 (QuikEval) operation. To use a QuikEval controller with the DC2222A, it is necessary to apply -9V and ground to the -9V and GND terminals. 9V for the DC2222A is provided by the QuikEval controller. Connect the QuikEval controller to a host PC with a

standard USB A/B cable. Connect the DC2222A to a QuikEval controller using the supplied 14-conductor ribbon cable. (Do not connect both a QuikEval and PScope controller at the same time.) Apply a signal source to J4 and J2. No clock signal is necessary at J1 when using a QuikEval controller. The clock signal is provided through the QuikEval connector (J3).

Run the QuikEval software (version K109 or later) supplied with the QuikEval controller or download it from

DC590 OR DC2026 QUICK START PROCEDURE

<http://www.linear.com/software>. The correct control panel will be loaded automatically. Click the Collect button (See Figure 5) to begin reading the ADC.

Pressing the Configuration button will bring up a Configurations Options menu similar to the one shown for PScope except that only the filtered output is available

and there are no options for verify and distributed read. Increasing DF will reduce the noise as shown in the histogram of Figure 6. The noise will be reduced by the square root of the number of times the number of samples is increased. In practice, as input voltage is increased reference noise will eventually limit the noise improvement.

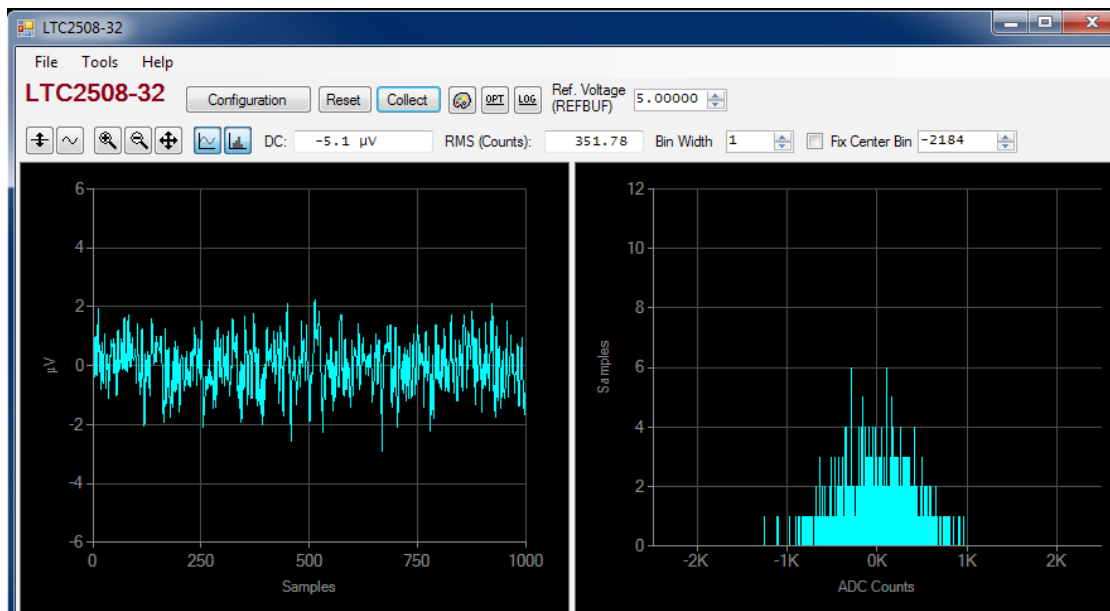


Figure 5. QuikEval Histogram with DF = 256

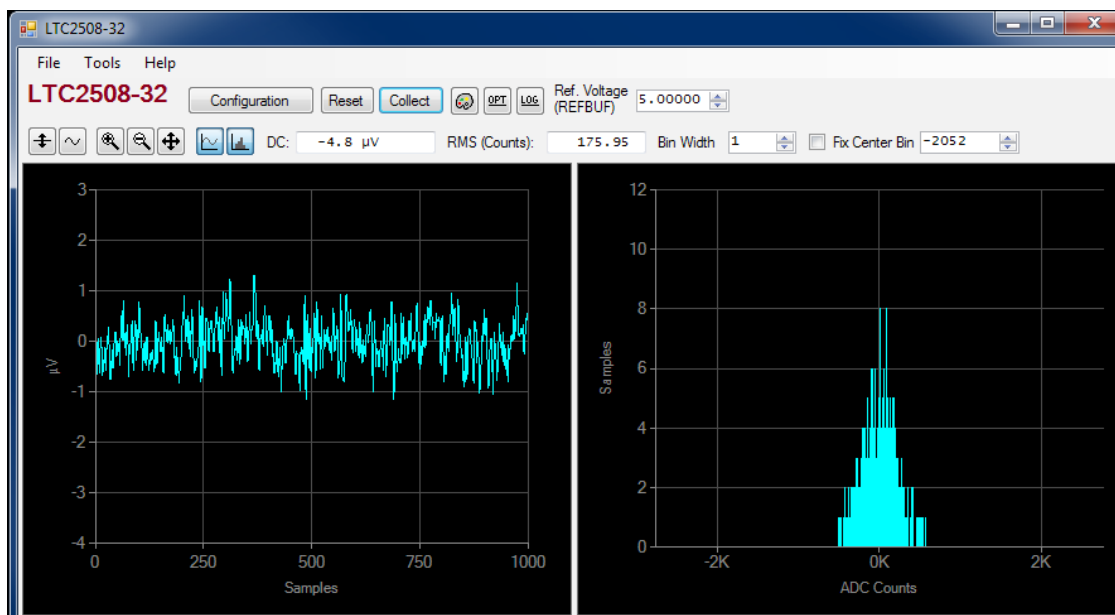


Figure 6. QuikEval Histogram with DF = 1024

DC2222A SETUP

DC Power

The DC2222A requires $\pm 9\text{VDC}$ and draws approximately $115\text{mA}/-18\text{mA}$ when operating with a 90MHz clock. Most of the supply current is consumed by the FPGA, op amps, regulators and discrete logic on the board. The 9VDC input voltage powers the ADC through LT1763 regulators which provide protection against accidental reverse bias. Additional regulators provide power for the FPGA and op amps. See Figure 1 for connection details.

Clock Source

When using the DC890 controller it is necessary to provide a low jitter $2.5\text{V}_{\text{P-P}}$ (If VCCIO is in the 3.3V position, the clock amplitude should be $3.3\text{V}_{\text{P-P}}$.) sine or square wave to J1. The clock input is AC coupled so the DC level of the clock signal is not important. A clock generator like the Rohde & Schwarz SMB100A is recommended. Even a good clock generator can start to produce noticeable jitter at low frequencies. Therefore it is recommended for lower sample rates to divide down a higher frequency clock to the desired input frequency. The ratio of clock frequency to conversion rate is shown in Table 1. If the clock input is to be driven with logic, it is recommended that the 49.9Ω terminator (R5) be removed. Slow rising edges may compromise the SNR of the converter in the presence of high amplitude higher frequency input signals.

Data Output

Parallel data output from this board (0V to 2.5V by default), if not connected to the DC890, can be acquired by a logic analyzer, and subsequently imported into a spreadsheet, or mathematical package depending on what form of digital signal processing is desired. Alternatively, the data can be fed directly into an application circuit. Use pin 50 of P1 to latch the data. The data can be latched using the falling edge of this signal. In verify mode two falling edges are required for each data sample. The data output signal levels at P1 can also be changed to 0V to 3.3V if the application circuit requires a higher voltage. This is accomplished by moving VCCIO (JP3) to the 3.3V position.

Reference

The default reference is the LTC6655 5V reference. If an external reference is used it must settle quickly in the presence of glitches on the REF pin. Referring to the reference circuit of Figure 7, desolder R37 and apply the external reference voltage to the V_{REF} terminal.

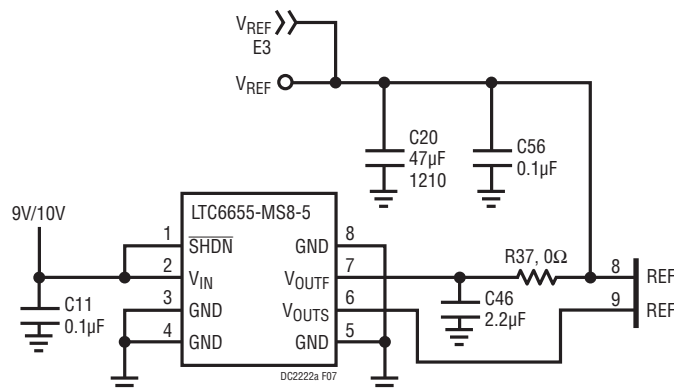


Figure 7. Reference Circuit

Analog Input

The default driver for the analog inputs of the ADC on the DC2222A is shown in Figures 8a and 8b. These circuits buffer the 0V to 5V input signal applied at A_{IN}^+ and A_{IN}^- . In addition, these circuits band limit the input signal at the ADC input. If the LTC2508-32 Figure 8a driver is to be used for AC applications it is recommended that capacitors C71 and C73 be removed and replaced with WIMA P/N SMDTC04470XA00KT00 $4.7\mu\text{F}$ thin film capacitors or equivalent in the C90 and C91 positions. This will provide the lowest distortion.

DC2222A SETUP

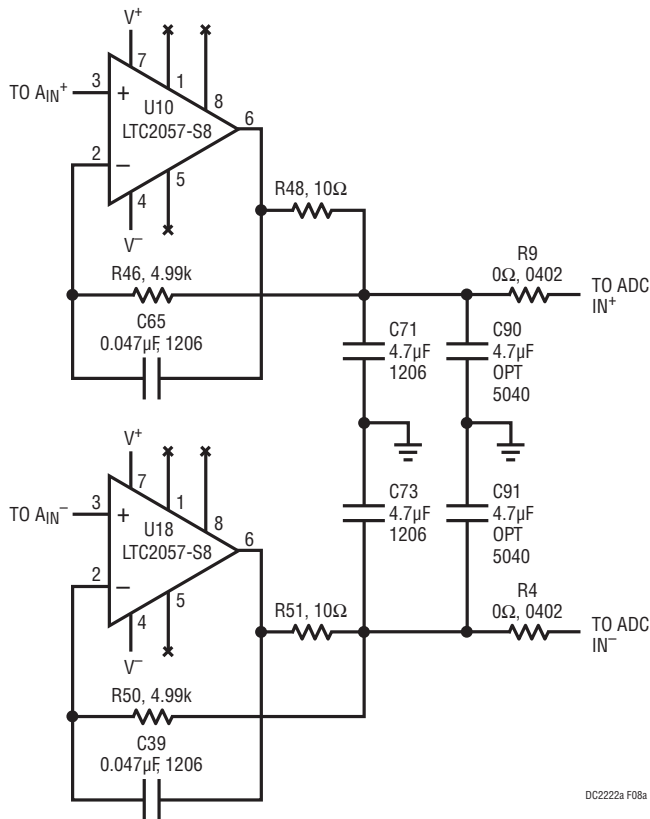


Figure 8a. LTC2508 Driver Circuit

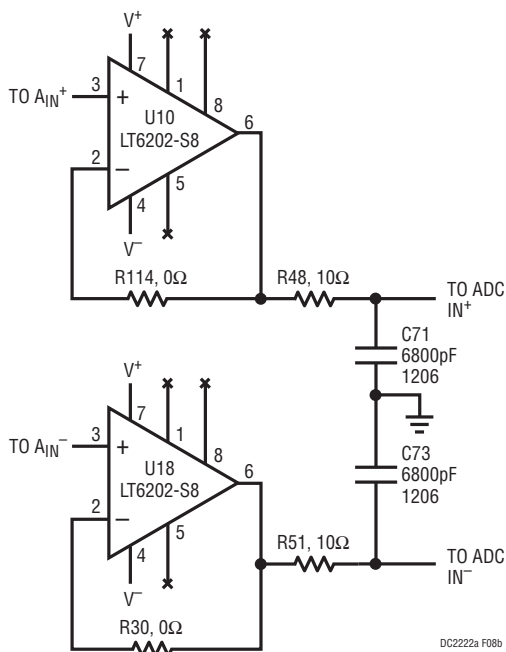


Figure 8b. LTC2500 and LTC2512 Driver Circuit

Data Collection

For SINAD, THD or SNR testing a low noise, low distortion differential output sine generator such as the Stanford Research SR1 should be used. A low jitter RF oscillator such as the Rohde & Schwarz SMB100A should be used as the clock source.

This demo board is tested in house by taking an FFT of a sine wave applied to the demo board's differential input. This involves using a low jitter clock source, along with a differential output sinusoidal generator at a frequency near 200Hz. The input signal level is approximately -1dBFS . The input is level shifted and filtered with the circuit shown in Figure 9. A typical FFT obtained with DC2222A is shown in Figure 4. Note that to calculate the real SNR, the signal level (F1 amplitude = -1dB) has to be added back to the SNR that PScope displays. With the example shown in Figure 4 this means that the actual SNR would be 123.54dB instead of the 122.54dB that PScope displays. Taking the RMS sum of the recalculated SNR and THD yields a SINAD of 117.75dB . The THD shown was obtained using the optional WIMA capacitors.

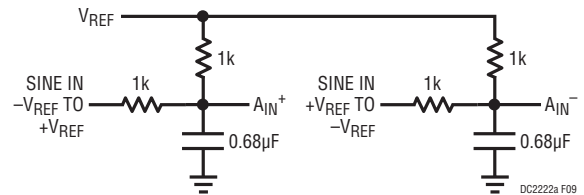


Figure 9. Differential Level Shifter

There are a number of scenarios that can produce misleading results when evaluating an ADC. One that is common is feeding the converter with a frequency, that is a sub-multiple of the sample rate, and which will only exercise a small subset of the possible output codes. The proper method is to pick an M/N frequency for the input sine wave frequency. N is the number of samples in the FFT. M is a prime number between one and $N/2$. Multiply M/N by the sample rate to obtain the input sine wave frequency. Another scenario that can yield poor results is if you do not have a sine generator capable of ppm frequency

DC2222A SETUP

accuracy or if it cannot be locked to the clock frequency. You can use an FFT with windowing to reduce the leakage or spreading of the fundamental, to get a close approximation of the ADC performance. If windowing is required, the Blackman-Harris 92dB window is recommended. If an amplifier or clock source with poor phase noise is used, windowing will not improve the SNR.

Layout

As with any high performance ADC, this part is sensitive to layout. The area immediately surrounding the ADC on the DC2222A should be used as a guideline for placement, and routing of the various components associated with the ADC. Here are some things to remember when laying out a board for the LTC2508-32. A ground plane is necessary to obtain maximum performance. Keep bypass capacitors as close to supply pins as possible. Use low impedance returns connected directly to the ground plane for each

bypass capacitor. Use of a symmetrical layout around the analog inputs will minimize the effects of parasitic elements. Shield analog input traces with ground to minimize coupling from other traces. Keep traces as short as possible.

Component Selection

When driving a low noise, low distortion ADC such as the LTC2508-32, component selection is important so as to not degrade performance. Resistors should have low values to minimize noise and distortion. Metal film resistors are recommended to reduce distortion caused by self heating. Because of their low voltage coefficients, to further reduce distortion NPO or silver mica capacitors should be used. Any buffer used for AC applications should have low distortion, low noise and a fast settling time such as the LTC6363 and LT6202. For DC accurate applications, the LTC2057 is also acceptable if adequate output filtering is applied.

DC2222A JUMPERS

Definitions

JP1: EEPROM is for factory use only. Leave this in the default WP position.

JP2: Coupling selects AC or DC coupling of A_{IN}^- . The default setting is DC.

JP3: VCCIO sets the output levels at P1 to either 3.3V or 2.5V. Use 2.5V to interface to the DC890 which is the default setting. Use 3.3V to interface to the DC590 or DC2026.

JP4: CM sets the DC bias for A_{IN}^+ and A_{IN}^- if the inputs are AC coupled. To enable AC coupling, R35 and R36 ($R = 1k$) shown in the schematic of Figure 10 must be installed. Installing these resistors will degrade the THD of the input signal to the ADC. $V_{REF}/2$ is the default setting. If EXT is selected the input common mode voltage can be set by driving terminal E5 (EXT_CM).

JP5: Coupling selects AC or DC coupling of A_{IN}^+ . The default setting is DC.

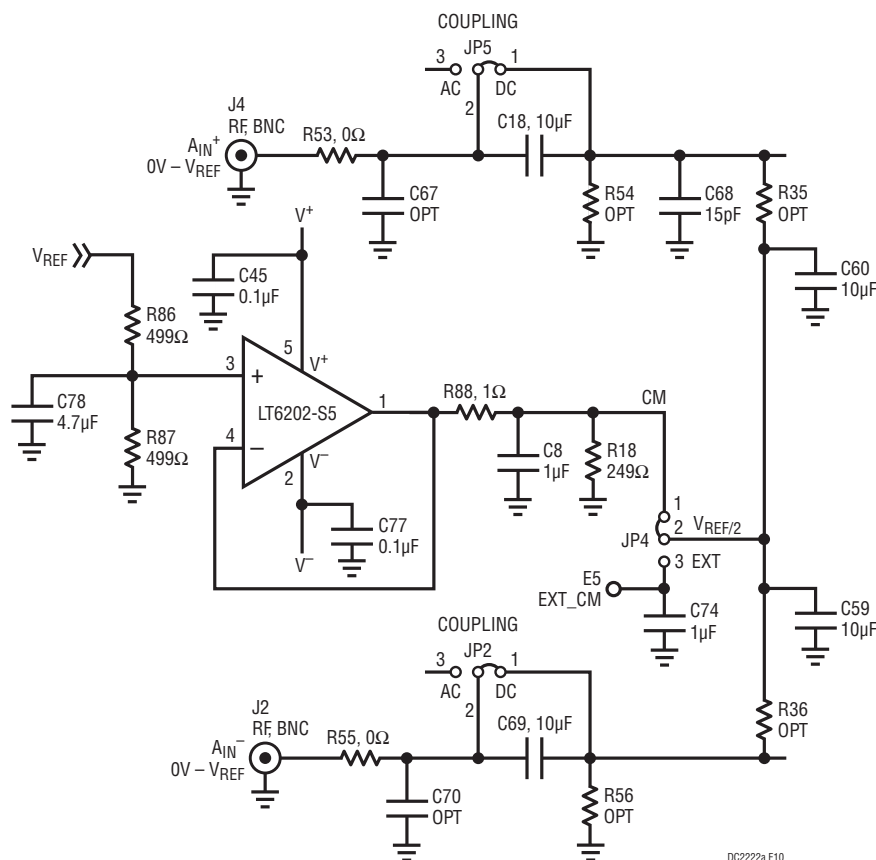


Figure 10. DC2222A Input Coupling

DEMO MANUAL DC2222A

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