TriCore™ AURIX™ Family

32-bit (TC26x, TC27x, TC29x)

PCB and High Speed Serial Interface (HSSI) design guidelines

AP32174

Application Note

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Microcontrollers

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Revision History

Version	Change Description
V1.0	Initial internal release for TC27x with simulation results in chp 4.
V1.1	Simulation results removed in chapter 4 and short description of high speed interfaces inserted
V1.2	Page 20/21; DC/DC SMPS layout example and table with recommended components inserted
V1.3	Page 14/Fig.13 updated (serial resistor inserted).
V1.4	Page 19; Layout example picture for BGA292 updated.
V1.5	Page8; Impedance calculation and formulas (Fig. 4) inserted, Page10; Fig.7 updated (differential impedance change with trace separation).
V1.6	Pages 18,20,22 (V1.6); Recommended decap value for VDDP supply net changed.
V1.7	Layout examples and content of the document extended to cover the TC26x, TC27x and TC29x AURIX products. Chapter 4.3 DAP interface layout recommendation and termination inserted. Text corrected and format of the document adapted to application note template.
V1.8	C16 added in Table 4 on page 37, Figure 24 updated, Corrections on Table 3 & 4

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Table of Contents

Revision History **4**

Table of Contents **5**

1 About this document **6**

2 High Speed Board Design **7**
2.1 Selection of stack-up for High Speed Board Design 7
2.2 Component Placement 8
2.3 Impedance Controlled Design of Traces 10
2.3.1 Estimating trace dimensions 13
2.4 Routing of High Speed Serial Signals 15
2.5 Correct Termination of Transmission Lines 16
2.6 Minimizing Crosstalk between Signal Channels 17
2.7 Board Level Filtering and Decoupling 18

3 Example Layouts for the AURIX Family **22**
3.1 Example Layouts 28
3.1.1 Example Layout for LQFP-144 Package 29
3.1.2 Example Layout for LQFP-176 Package 31
3.1.3 Example Layout for LFBGA-292 Package 33
3.1.4 Example Layout for BGA-416 Package 35
3.1.5 Example Layout for BGA-516 Package 37
3.2 Decoupling Capacitors for Different Supply Modes 39

4 HSSI on AURIX products **41**
4.1 2.5 Gbit/s HSSI 41
4.2 HSCT Interface 41
4.3 DAP Interface 41

5 References **43**

1 About this document

This document provides information for designing High Speed Serial Interfaces (HSSI) on the AURIX™ family of 32-bit microcontrollers from Infineon, covering the TC26x, TC27x and TC29x devices. The topics covered include PCB Design considerations regarding the routing of high speed signals, selecting stack-up of the PCB, impedance controlled design of the traces, and termination of high speed signal paths.

Also included in this document are layout proposals on escape routing for the available package types of the AURIX microcontroller family, such as TQFP and LFBGA Packages.

The document should be read in conjunction with Application Note “AN24026 - General Design Guideline for Microcontroller” (available from **www.infineon.com**).

Note: This application note contains design recommendations from Infineon Technologies point of view. Effectiveness and performance of the final application implementation must be validated by the customer, based on their specific implementation choices.

2 High Speed Board Design

The biggest challenges in high speed design are to minimize the crosstalk and achieve good signal integrity for the transmitted signal, and also to minimize the noise effects on the board. This must be guaranteed for both single ended and differential pair signaling (LVDS) signals, as these are typical high speed interface signal types.

Most of the recommendations are rules that help to avoid the problems but the design process itself must be treated as a trade-off process between the design guidelines. The designer must decide on parameters which have an effect on the performance, reliability and cost of the design.

With those considerations in mind, the following topics should be treated as critical in the design process:

1. Selection of stack-up for high speed board design
2. Component placement of signal transmitter and receiver circuits
3. Impedance controlled design of traces
4. Routing of high speed serial signals
5. Correct termination of the transmission lines
6. Minimizing crosstalk between the signal channels
7. Board Level Filtering and Decoupling

2.1 Selection of stack-up for High Speed Board Design

Selection of the correct stack-up for a high speed board should be done at the beginning of the board design because the selection can have an effect on the routing and impedance control of the traces. Impedance control of the traces is one of the main parameters of the high speed design.

The following issues must be considered:

- How can it be guaranteed that high speed lines have a solid GND reference without interruption of the impedance continuity.
- Signal lines must have minimum distance to reference the plane layer.
- Ensure, as much as possible, a plane capacitance for the supply domains.
- How to avoid vias or layer change on high speed signals.

Since the discrete board decoupling capacitors can only be effective up to 200MHz, the plane decoupling should be used where possible.

The stack-up should be selected so that you can build a power plane capacitance and have the benefit of the high frequency decoupling effect which could be effective above 200MHz.

The following are sample stack-up’s of 4-Layer and 6-Layer boards.

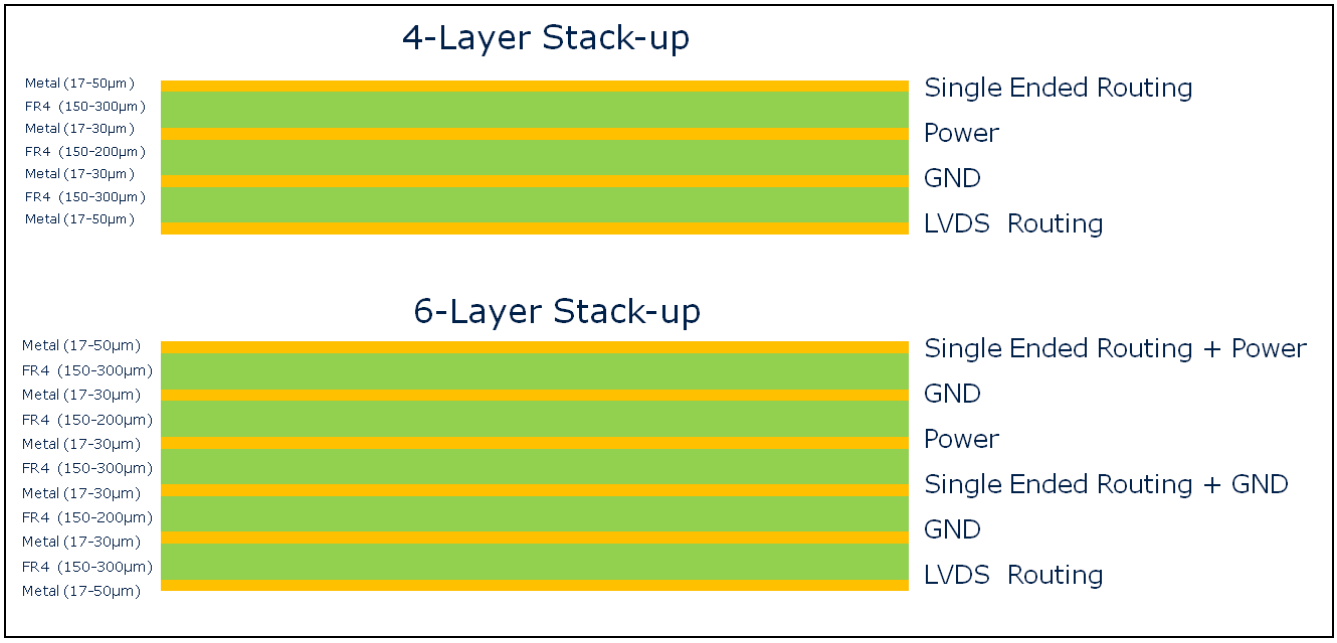


Figure 1 Sample stack-up´s for 4 and 6-Layer boards

2.2 Component Placement

- Place the µC and Connector with high speed signals first, to ensure minimal length of the traces
- Do not place other components between these Connectors and the µC
- Place possible noise sources away from the high speed signals
- Components that communicate with devices outside the board should be placed at the edge of the board

Table 1 Considerations for unused "Output, Supply, Input and I/O" pins

1. Supply Pins (Modules)	• See the User´s Manual.
2. I/O-Pins	• Should be configured as output and driven to static low in the weakest driver mode in order to improve EMI behaviour. Configuration of the I/O as input with pull-up is also possible. • Solder pad should be left open and not be connected to any other net (layout isolated PCB-pad only for soldering).
3. Output Pins including LVDS	• Should be driven static in the weakest driver mode. • If static output level is not possible, the output driver should be disabled. • Solder pad should be left open and not be connected to any other net (layout isolated PCB-pad only for soldering).
4.Input Pins without internal pull device	• For pins with alternate function see product target specification to define the necessary logic level. • Should be connected with high-ohmic resistor to GND (range 10k – 1Meg) wherever possible. No impact on design is however expected if a direct connection to GND is made. • Groups of 8 pins can be used to reduce number of external pull-up/down devices (keep in mind leakage current).
5. Input Pins with internal pull device	• For pins with alternate function see product specification to define the necessary logic level • Should be configured as pull-down and should be activated static low (exception: if the User´s Manual requires high level for alternate functions). No impact on design is expected if static high level is activated. • Solder pad should not be connected to any other net (isolated PCB-pad only for soldering)

2.3 Impedance Controlled Design of Traces

Design of traces for high speed signals is critical. They should be designed to have a trace impedance of 50 Ohm and differential impedance of 100 for LVDS signals.

There are two types of transmission lines for trace implementation:

- Microstrip
- Stripline

Depending on the selected stack-up for the design, calculate the characteristic impedance for either microstrip or stripline transmission line to have 50 Ohm trace impedance.

Microstrips

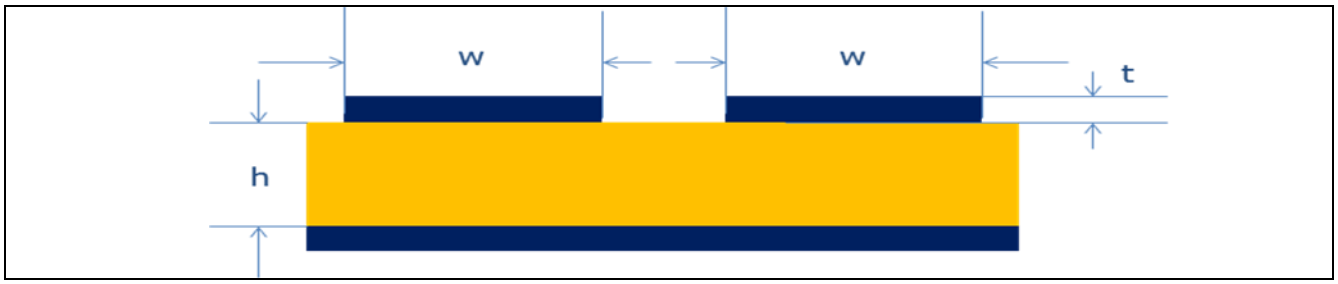


Figure 2 Microstrip Transmission line

Formula:

$$Z_o = \frac{87}{\sqrt{\varepsilon_r + 1.41}} * \ln\left(\frac{5.89 * h}{0.8 * w + t}\right)$$

(Formula is valid when 0.1<w/h<2.0 and 1<ε<15) [2]

Striplines

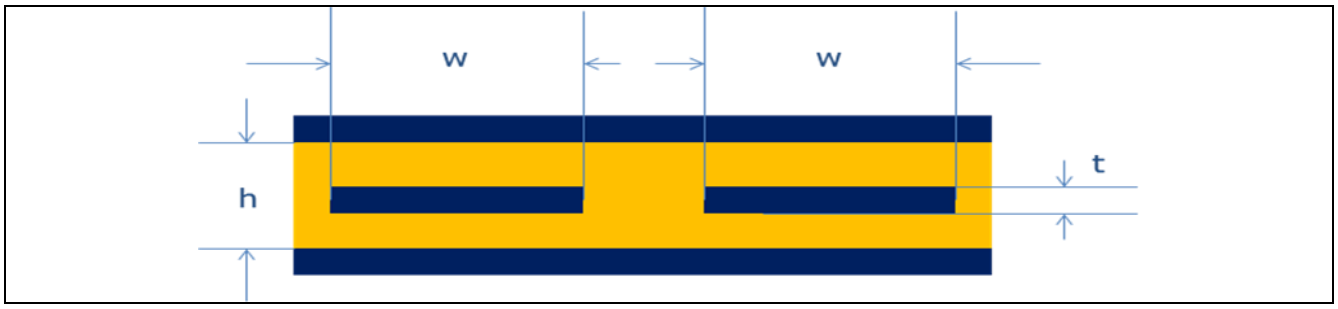


Figure 3 Stripline Transmission Line

Formula:

$$Z_o = \frac{60}{\sqrt{\varepsilon_r}} * \ln\left(\frac{1.9 * h}{0.8 * w + t}\right)$$

(Formula is valid when w/h<0.35 and t/h<0.25) [2]

Key to formulas

- **h**
  - for microstrip = Height over ground
  - for stripline = Separation between grounds
- **w** = trace width
- **t** = Line Thickness
- ε_r = Relative Permittivity of substrate (all distance units are Inches)

Transmission line parameter

It is possible to calculate the impedance of the traces by using the transmission line parameter. The parameter can be delivered by the PCB manufacturers.

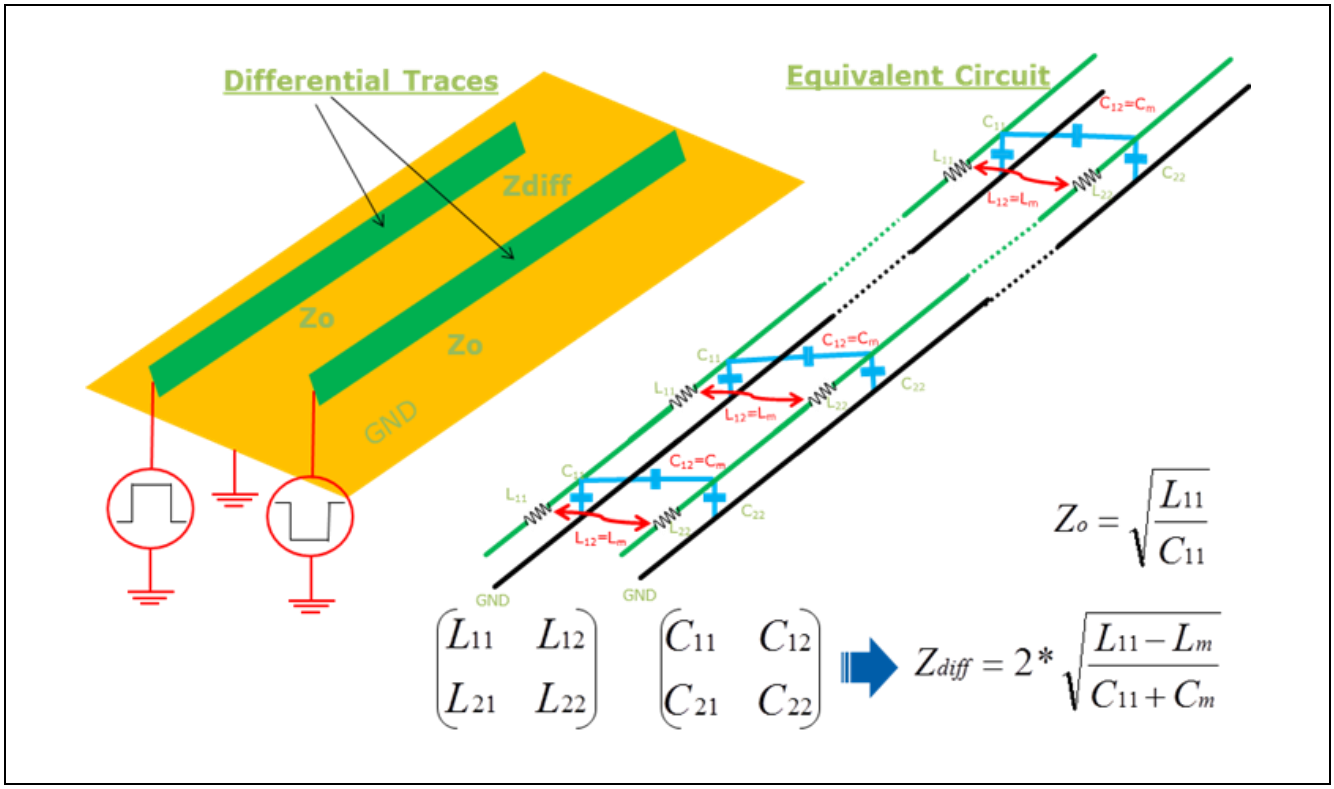


Figure 4 Calculation of the Impedance by using transmission line parameter

To determine if the trace has to be considered as controlled impedance trace (critical length), the following rule and calculation can be used:

- If the trace is longer than ¼ of the distance covered by the rise time of the signal, then the controlled impedance should be applied.

Sample calculation (for FR4 material and 500ps rise time):

Propagation velocity: $$v = \frac{c}{\sqrt{\varepsilon_r}} = \frac{3*10^{10}}{\sqrt{4.1}} = 14.8[cm/ns]$$

Distance at rise time: $$14.8[cm/ns]*0.5[ns] = 7.4cm$$

Critical Length: $$\frac{7.4}{4} = 1.85cm$$

From the EMI point of view it is recommended to use striplines, since they are placed on the inner layer where the traces cannot cause radiation to the outside of the board. But striplines require a layer change which can cause impedance discontinuity and this will result in reflections. It is also difficult to meet the impedance requirement of 50 Ohm for trace and 100 Ohm differential impedance because of different reference layers.

The differential impedance is dependent on:

- the distance between the lines
- the distance to the reference plane

For the correct calculation of the trace and differential impedance, 2D field solvers or the Signal Integrity capability of the layout tool can be used. Most of the tools on the market offer this. In this case it is possible to route the lines without worrying about the impedance calculation, since the tool calculates and adapts the parameter so that impedance controlled lines are always guaranteed.

The following rules must also be applied in the design and routing:

- Use traces that are as wide as possible
- Microstrip lines are recommended as the differential signaling cancels most of the radiation
- In there are still radiation problems, the stripline design can also be used
- Keep trace width/spacing ratio less that 0.8 to reduce the effect on trace impedance
- Ensure that 50 Ohm trace and 100 Ohm differential impedance with a tolerance of ±10% can be guaranteed by the manufacturer of the PCB

2.3.1 Estimating trace dimensions

The following diagrams (valid for 35µm thick Microstrips) can be used to estimate the trace dimensions in the early design phase before final impedance calculations are made.

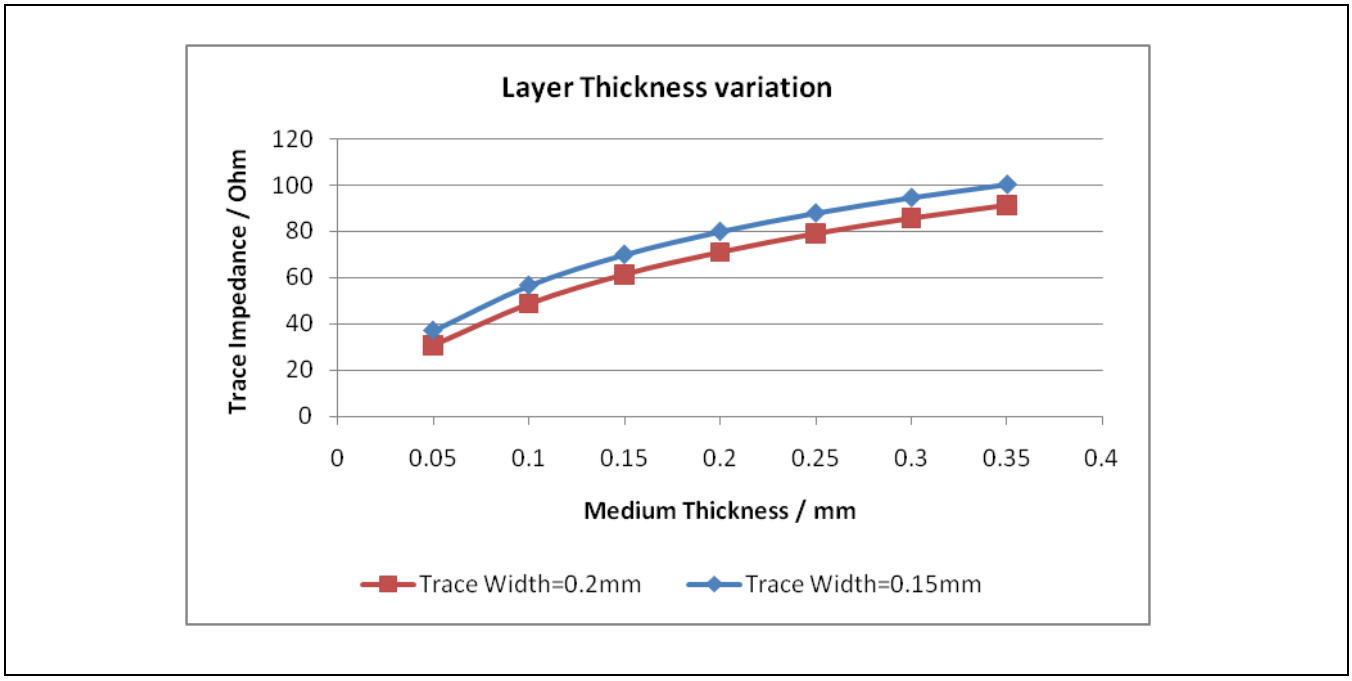


Figure 5 Trace Impedance change with Layer Thickness

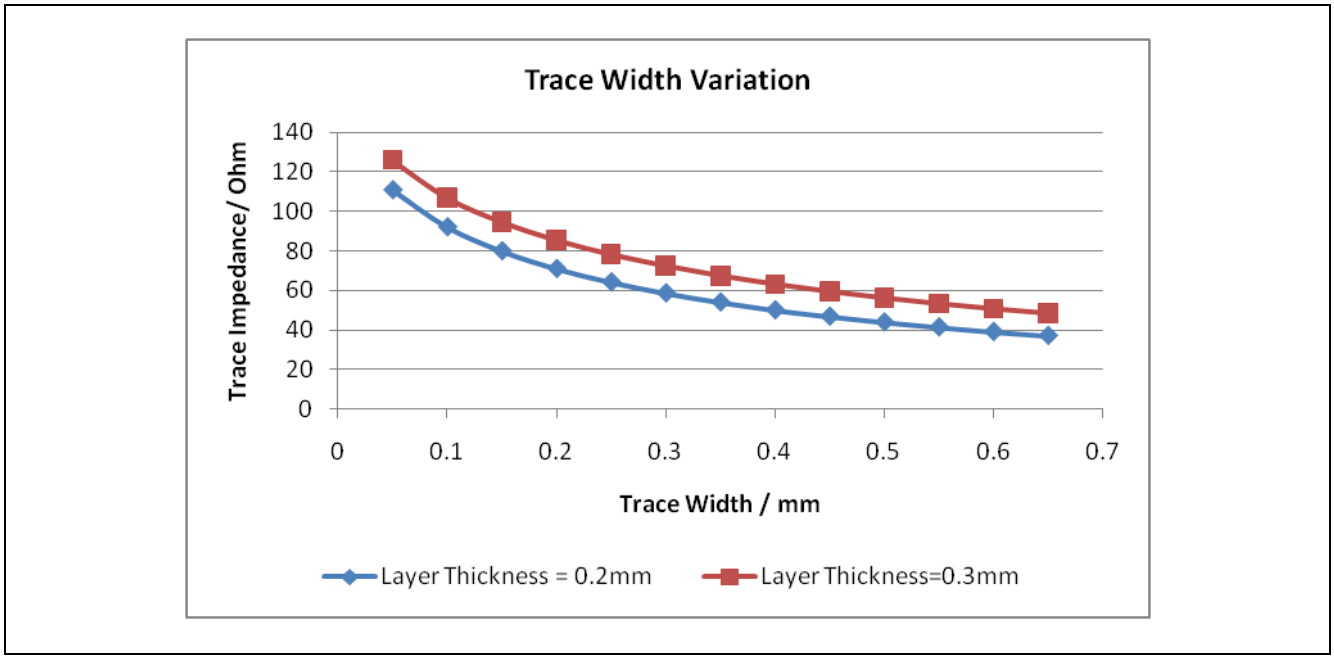


Figure 6 Trace Impedance change with Trace Width

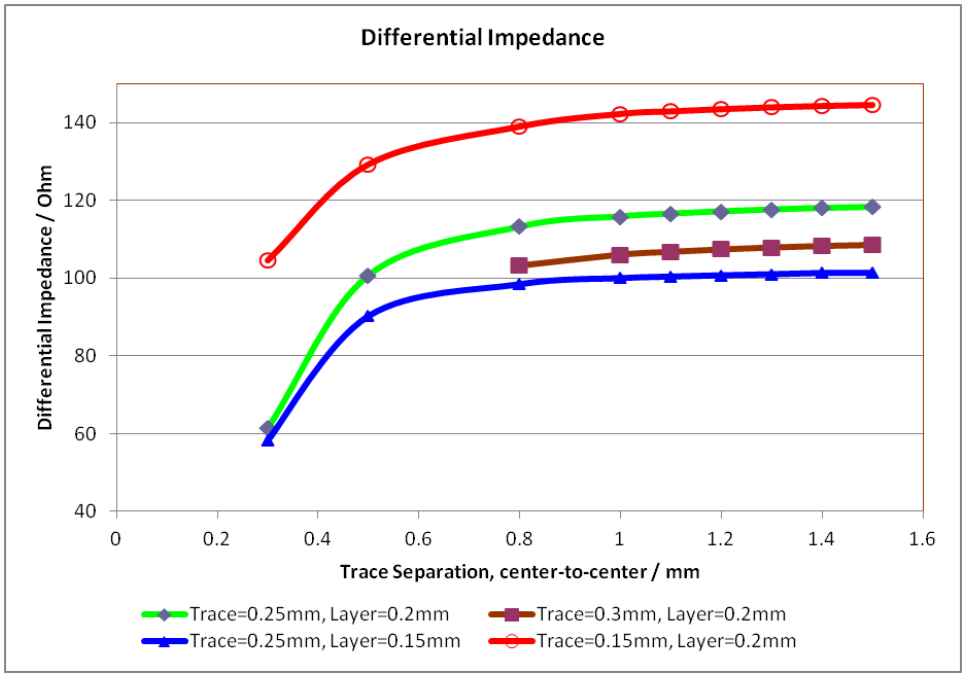


Figure 7 Differential Impedance change with Trace separation

2.4 Routing of High Speed Serial Signals

- High speed signals should be routed first to reach the required specification for impedance continuity, across a short distance and with optimal channel design.
- Do not place traces over split planes. Traces should have a solid reference GND plane over the whole length without interruption to avoid impedance discontinuity and reflections.
- Keep in mind that the return current path should be close to the signal line. The current loop should be as small as possible.
- Keep the traces as short as possible.
- Route traces straight. Point-to-point connections are required for differential lines and do not use daisy-chain routing. If required, do not use stubs along the daisy-chain connections.
- Do not used 90° bending instead of 45°, if it cannot be avoided.
- Don not use layer changes and avoid vias on traces.
- If a layer change is necessary, use a solid GND reference.
- Place GND vias near the signal lines (Differential via – GSSG) if a layer change cannot be avoided

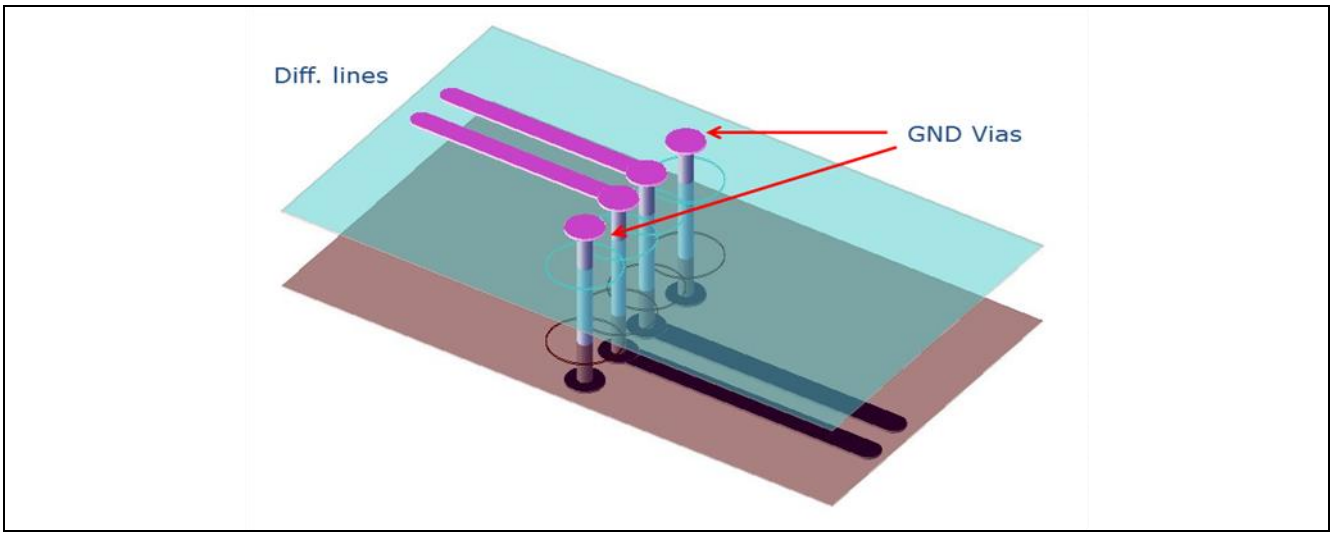


Figure 8 Differential Via

- All differential traces must be matched in length.
  - Length differences between differential traces can cause skew between the differential lines. Skew has an effect on common mode and reduces the voltage swing.
  - Keep the length difference of the differential traces less than 1mm for Gb/s Interface.
- Route single ended traces on different layers to the differential lines, or keep a minimum distance of 4 traces wide to each other, to minimize the crosstalk.
- Avoid impedance discontinuity along the trace.
  - SMT Pads of AC coupling capacitors which are referenced to GND planes can have different impedance to the required 50 Ohm. In that instance the GND plane underneath the pads can be removed, but it will be necessary to ensure field solver analysis on the resulting impedance.

2.5 Correct Termination of Transmission Lines

There are different types of termination techniques:

- Near End (source) Termination
- Far End Termination

Near End (Source) termination

This is normally used by the single ended lines where the output driver has lower impedance than the transmission line. In this case the series termination is added to the output of the driver to match the line impedance.

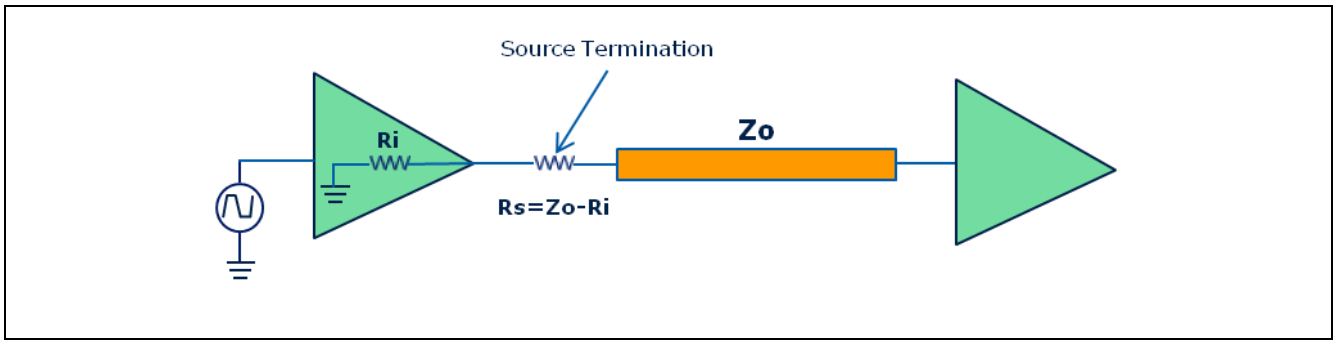


Figure 9 Near-End (Source) Termination for Single Ended Lines

- Place the resistor very close to the source driver.
- Use source termination in cases of point-to-point connection.
- Do not use daisy-chain topology.
- All loads must be at the end of the line.

Far End termination

The most common type of Far End termination for HSSI is Parallel or AC Termination.

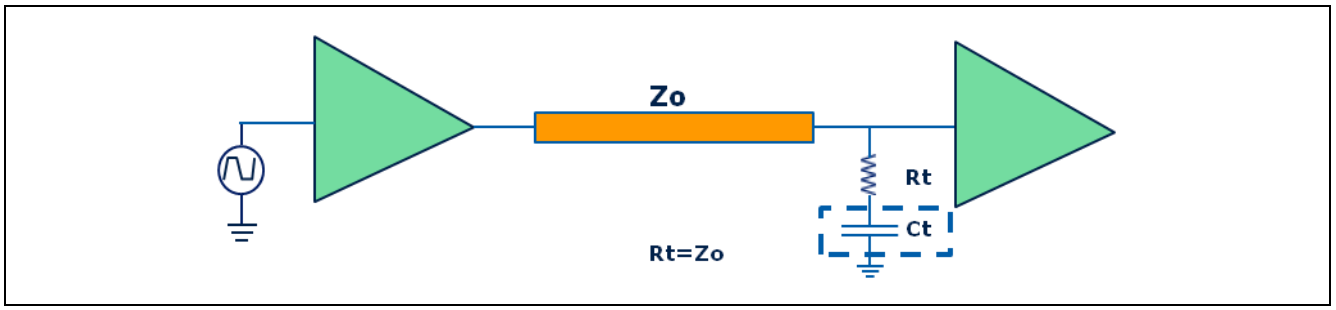


Figure 10 Parallel and AC Termination for Single Ended Lines

- Parallel termination resistance should be matched to the characteristic impedance of the line.
- Parallel termination causes power consumption due to the DC path at the end of the line for high signal level. The thermal treatment should be done by selection of the parallel termination resistor.
- The power consumption can be avoided with AC termination, where a capacitor is inserted in series to the termination resistor.
- The Capacitor value in AC termination should be in the range of 100-200pF.

- This termination technique increases the rising and falling times at load due to the capacitive load. Timing considerations should be made by selection of the value of C.
- Place the components close to the receiver pins so that no long stubs are required.

Termination of Differential lines

Special attention should be given to the termination of the differential lines.

The differential lines require more than 50 Ohm line impedance and 100 Ohm differential impedance between the lines. So the termination must be matched to the 100 Ohm.

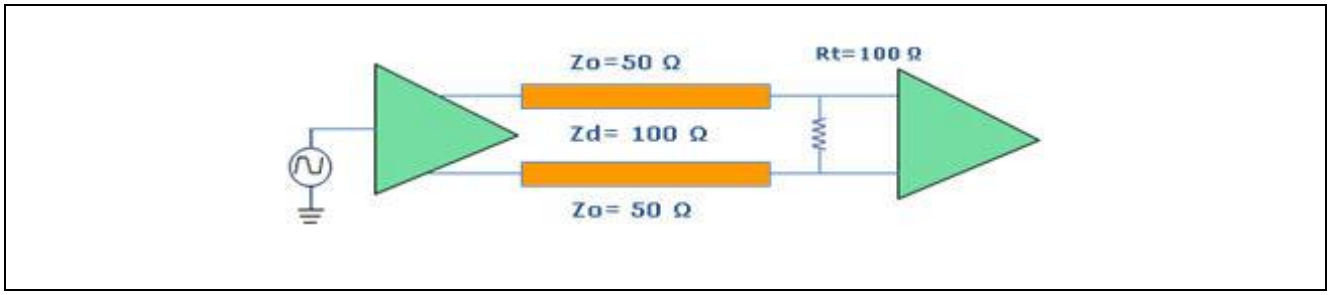


Figure 11 Terminations for Differential Lines

- Place termination after the connection of the trace to the pin of receiver so that no stubs are created before the receiver. This avoids reflections generated by the impedance discontinuity.
- Do not use layer change or a via for the placement of the termination.

2.6 Minimizing Crosstalk between Signal Channels

Coupling of the electrical signals occurs if lines are routed parallel for a long distance.

Coupling problems can be avoided with careful PCB design:

- Separate the routing layer for single ended and differential signals.
- Route all traces perpendicular if two adjacent layers have high speed lines.
- Do not route signals closer than 4 times the electrical height to the reference.
- Reduce the distance to the reference layer as much as possible.
- A transmission line which has lower distance to the reference plane has less coupling to the adjacent traces.
- Avoid parallel routing of high speed signals over long distances.
- For the differential signals, keep the distance constant along the length of the traces.
- If serpentine routing (to match the differential length of traces) is required, separate the parallel running traces 4 times the dielectric height.
- Apply serpentine routing for length matching at the transmitter side rather than the receiver side.
- Route critical signals on adjacent layers orthogonal to each other.

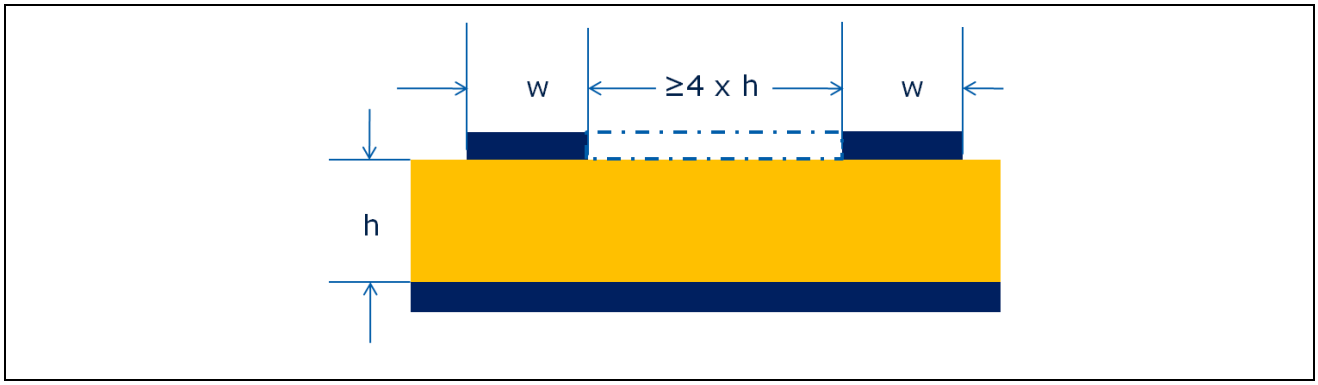


Figure 12 Rules for trace separation and serpentine routing

2.7 Board Level Filtering and Decoupling

Decoupling the Power Distribution Network of the microcontroller IC is critical to the PCB design process, because careful selection of the decoupling capacitors and placement has a big influence on the high speed performance of the board, and can reduce the emissions. The on-board decoupling capacitors have an effective range of 1MHz – 200MHz. The range above 200MHz can be covered by using power plane capacitance.

The effectiveness of the decoupling capacitors depends on the optimum placement and connection type.

- Place capacitors as close as possible to the µC.
- Keep the interconnection inductance of capacitors to the µC as low as possible.
- Use low effective series resistance and inductance (ESR and ESL) capacitors.
  - Since parasitic inductance is the limiting factor of the capacitor response to high frequency demand of current from the device, the ESL of the capacitor and the connection inductance should be selected so that the optimum value for the design is reached.
- Connect capacitors with vias close to the side of the pads.
  - Use side placement of the vias to reduce the current loop.

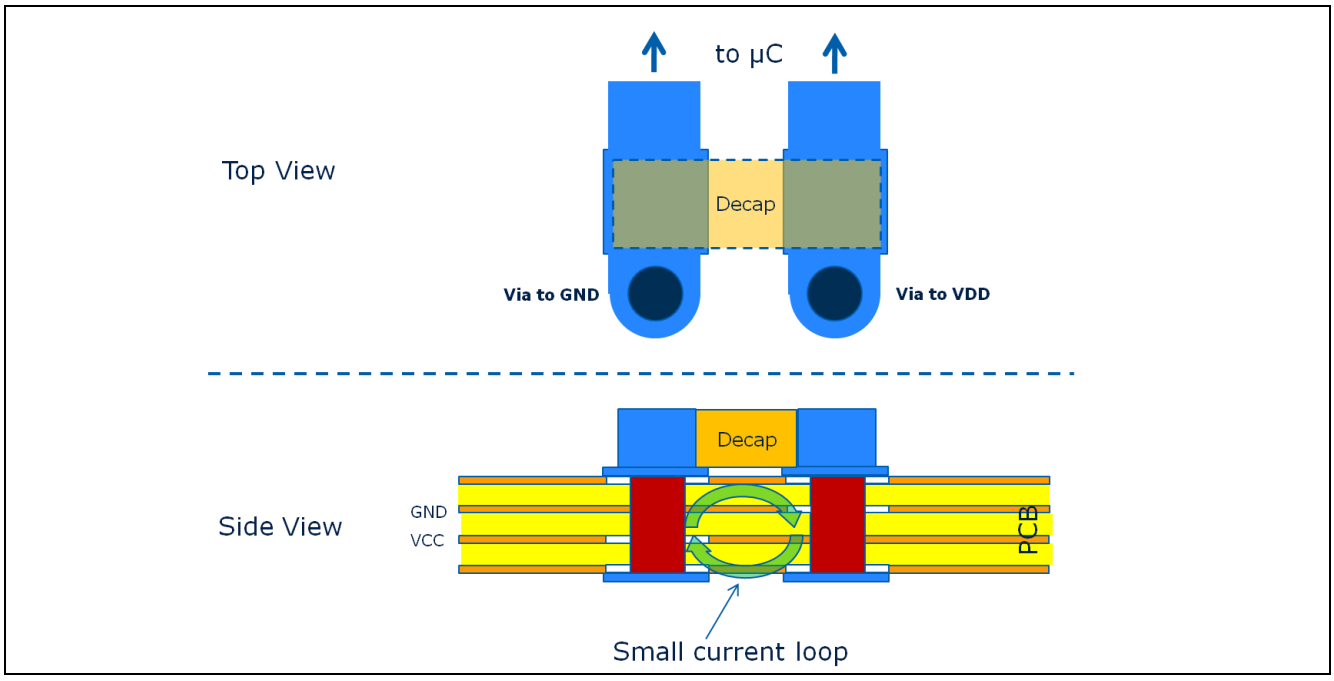


Figure 13 Connection of decaps

- Dual vias can be used to reduce the parasitic inductance.
- Solder lands, traces and vias should be optimized for capacitor placement.
- Do not use long traces to connect capacitors to GND or to VDD.
  - Always keep the return path of the high frequency current (lowest inductance path) small.
- Select the smallest package available for the capacitors.
  - Select capacitors of type: ceramic multilayer X7R or X5R.
- To reduce the radiation / coupling from the oscillator circuit, a separated ground island on the GND layer should be made. This ground island can be connected at one point to the GND layer.
  - This helps to keep noise generated by the oscillator circuit locally on this separated island.
  - The ground connections of the load capacitors and VSSOSC should also be connected to this island.
  - Traces for the load capacitors and Xtal should be as short as possible.

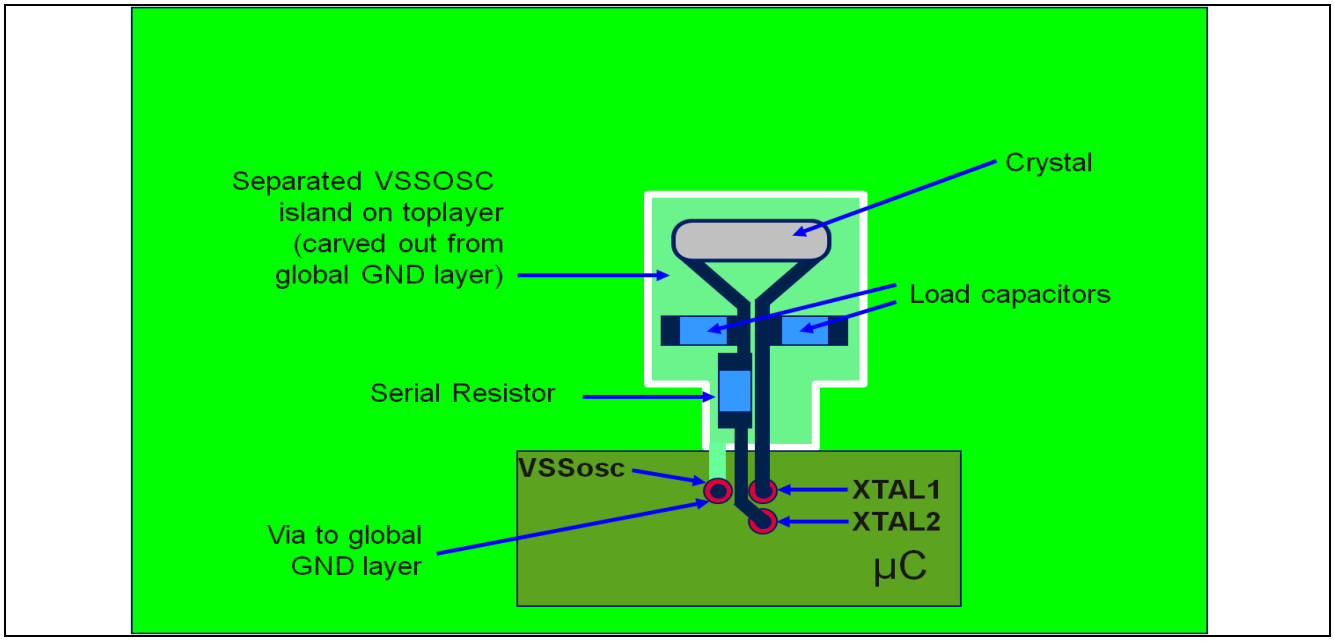


Figure 14 Layout proposals for Oscillator circuit (shown for BGA Package)

- To minimize the EMI radiation on the PCB, the following signals are to be considered as critical:
  - LVDS Pins (HSCT, MSC, QSPI, AGBT)
  - ERAY Pins
  - Ethernet Pins
  - QSPI Pins
  - MSC Pins
  - External Clock Pins
  - Supply Pins

Note:

1. *Route these signals with adjacent ground reference and avoid signal and reference layer changes.*
2. *Route them as short as possible.*
3. *Routing ground on each side can help to reduce coupling to other signals.*

- The ground system must be separated into analog and digital grounds. The analog ground must be separated into two groups:
  - Ground for OSC / PLL supply pins as common star point.
  - Ground for ADC (VSSM for VDDM) as common star point.
- The power distribution from the regulator to each power plane should be made over filters.
- RC Filters can be inserted in the supply paths at the regulator output and at the branching to other module supply pins like VDD and VDDP3 (for osc.), VDDFL3, and VDDM.
  - Using inductance or ferrite beads (5 – 10 µH) instead of the resistors can improve the EME behavior of the circuit and reduce the radiation up to ~10dBµV on the related supply net.
- OCDS must be disabled.
- Select weakest possible driver strengths and slew rates for all I/Os (see Scalable Pads Application Note AP32111).
- Use lowest possible frequency for SYSCLK.
- Avoid cutting the GND plane by via groups. A solid GND plane must be designed.

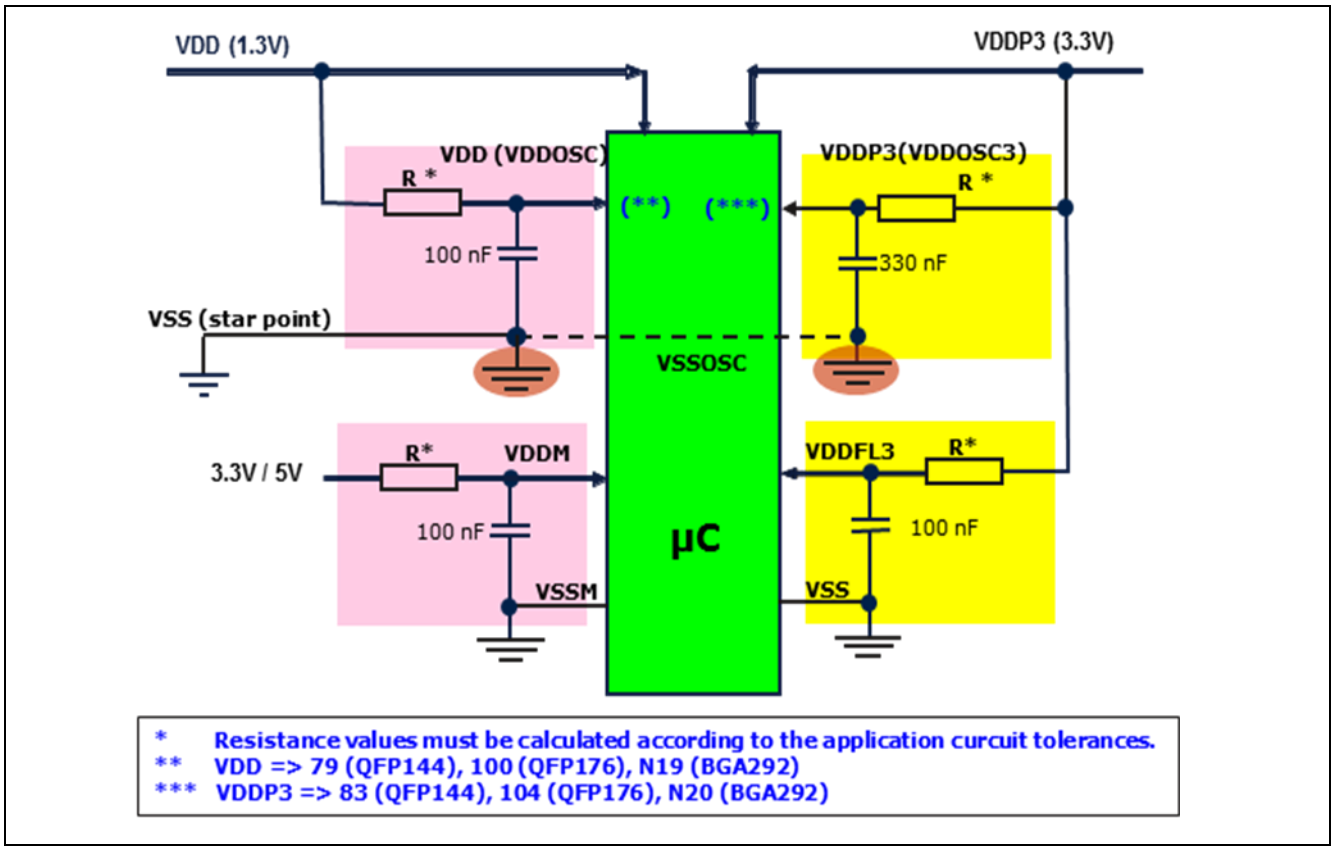


Figure 15 Filtering of VDD, VDDP, VDDFL3, VDDM supply pins for TC27x & TC26x

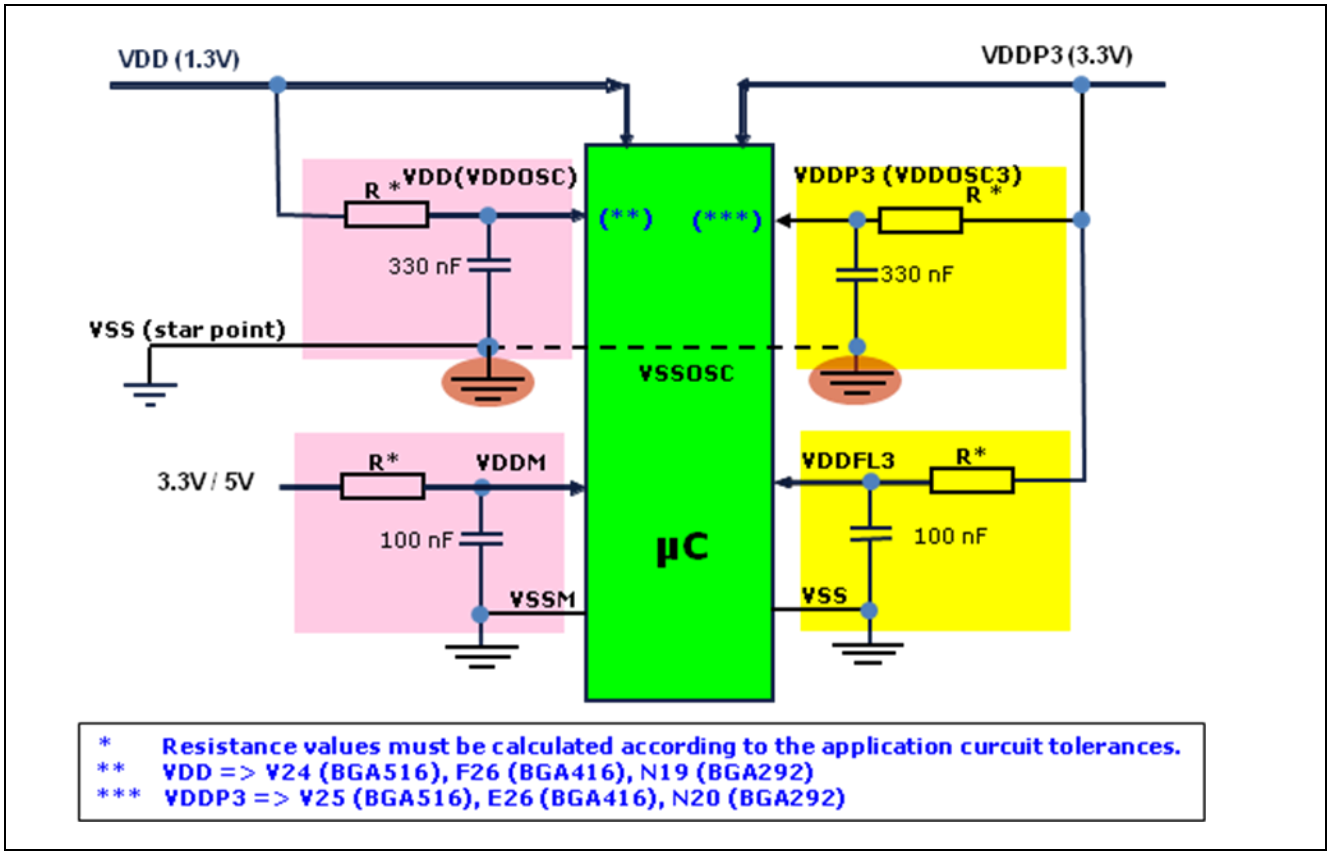


Figure 16 Filtering of VDD, VDDP, VDDFL3, VDDM supply pins for TC29x

3 Example Layouts for the AURIX Family

The AURIX TC26x, TC27x and TC29x 32-Bit microcontroller products are available in the following packages:

- LQFP-144
- LQFP-176
- BGA-292
- BGA-416
- BGA-516

The microcontrollers have the following supply domains:

- VDD=1.3V for Core
- VDDP=3.3V for I/O Pad
- VDDEBU=3.3V for EBU
- VDDM=3.3V or 5V for ADC
- VFLEX =3.3V or 5V for Flex port
- VFLEXE =3.3V or 5V for EBU Flex port
- VDDFL3=3.3V for Flash
- VEXT=3.3V or 5V for external supply option, which should be decoupled individually

The power supply feeding from the regulator outputs to each domain can be made on a supply layer (POWER).

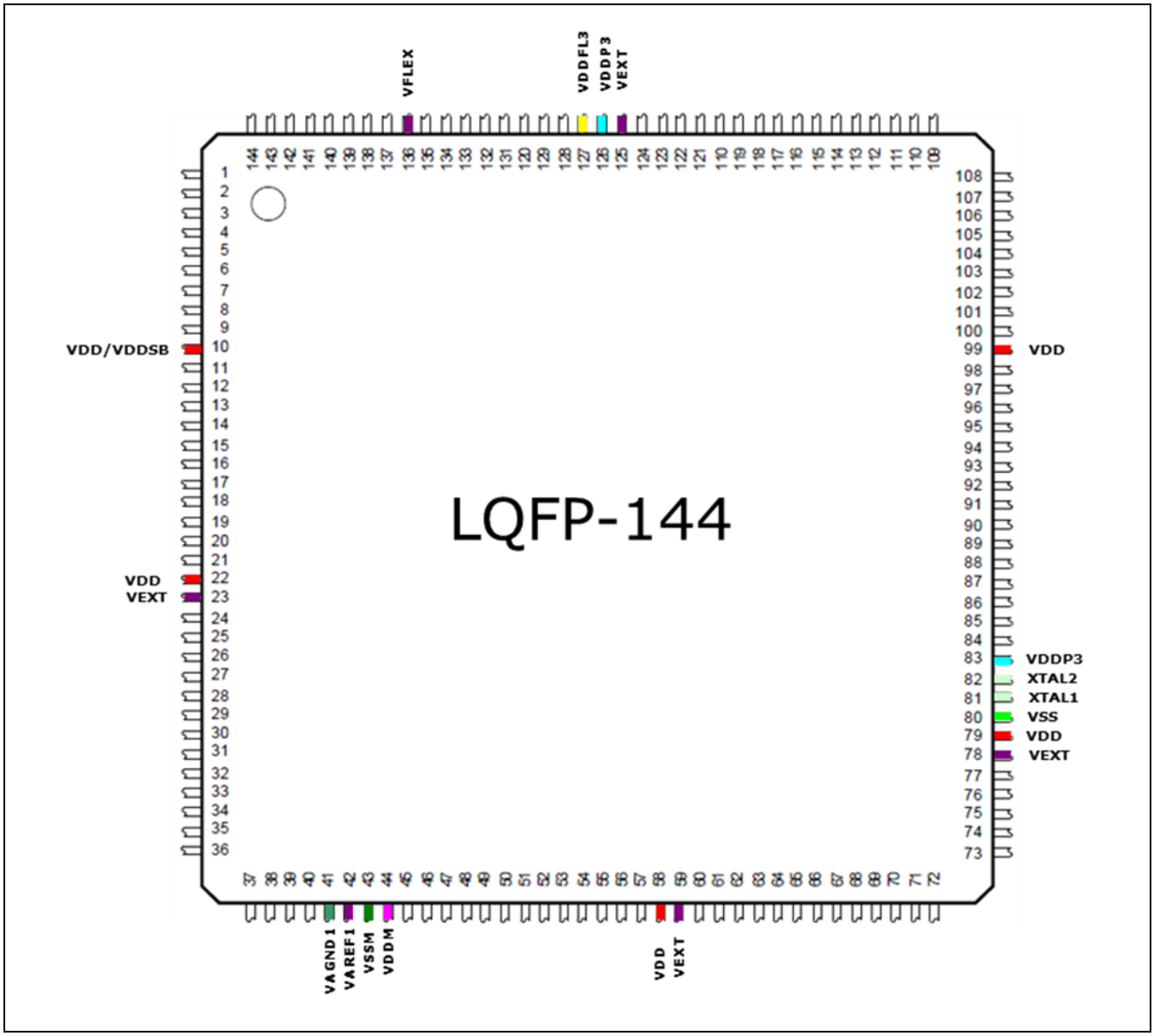


Figure 17 LQFP-144 Package

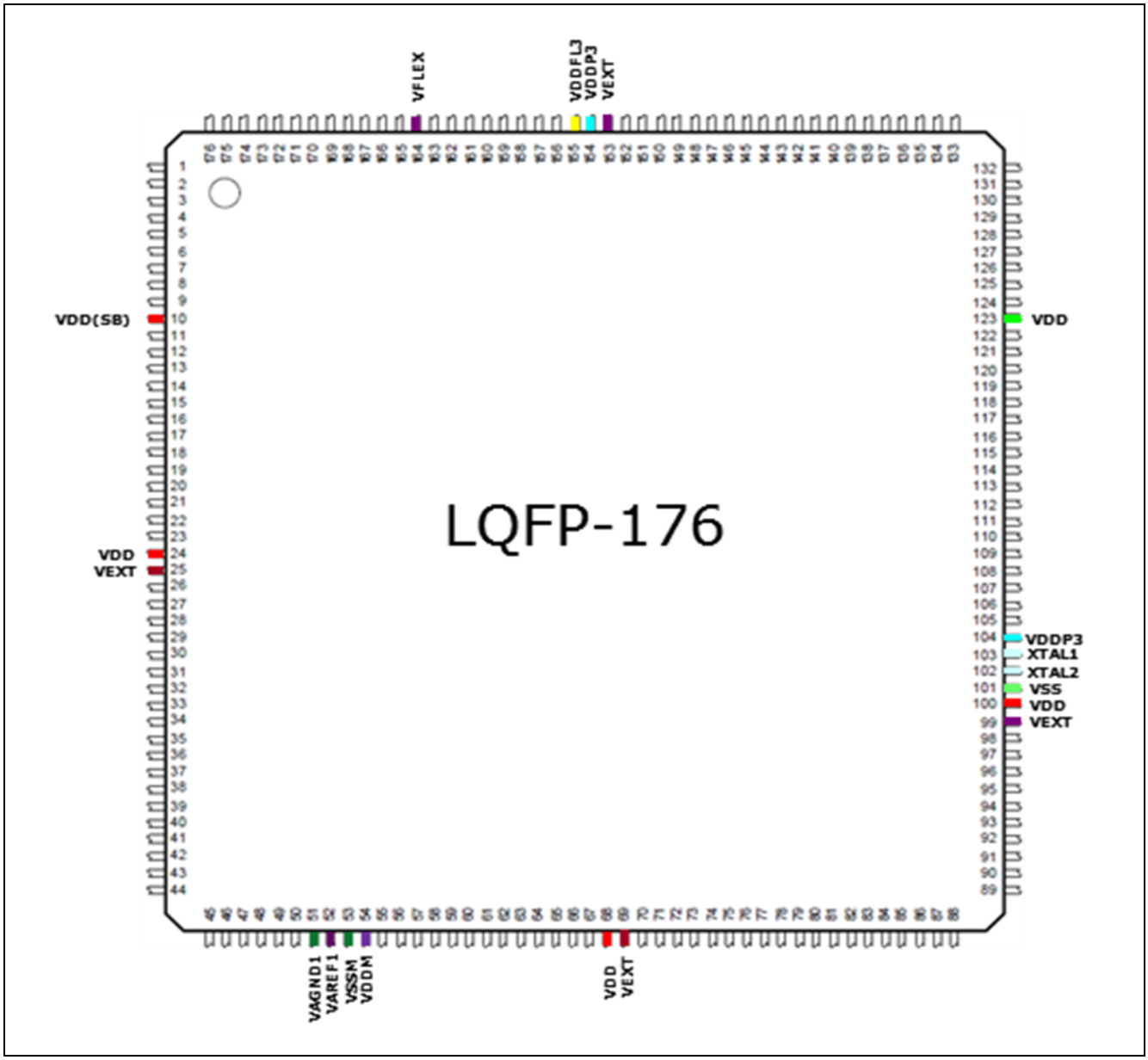


Figure 18 LQFP-176 Package

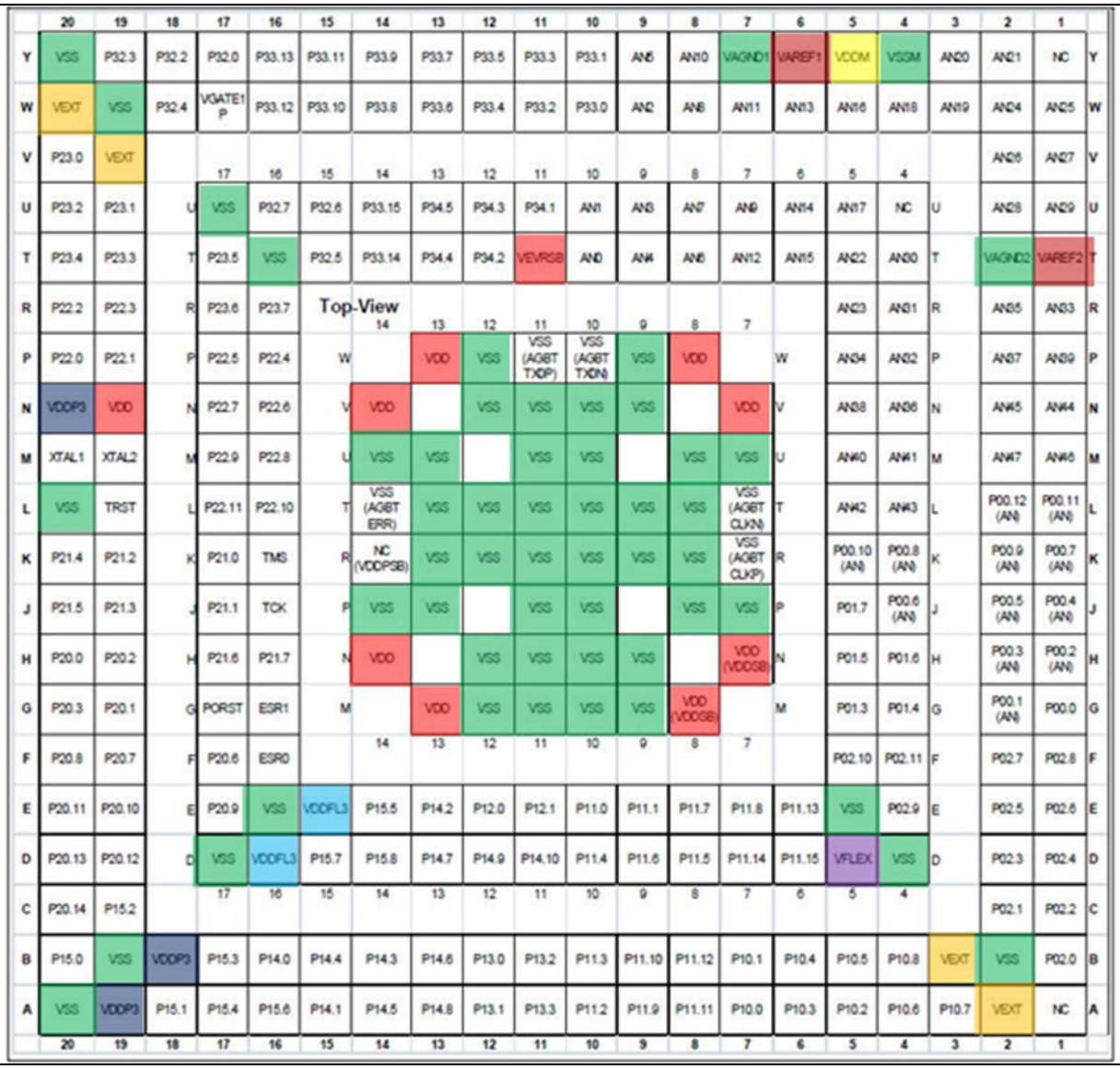


Figure 19 LFBGA-292

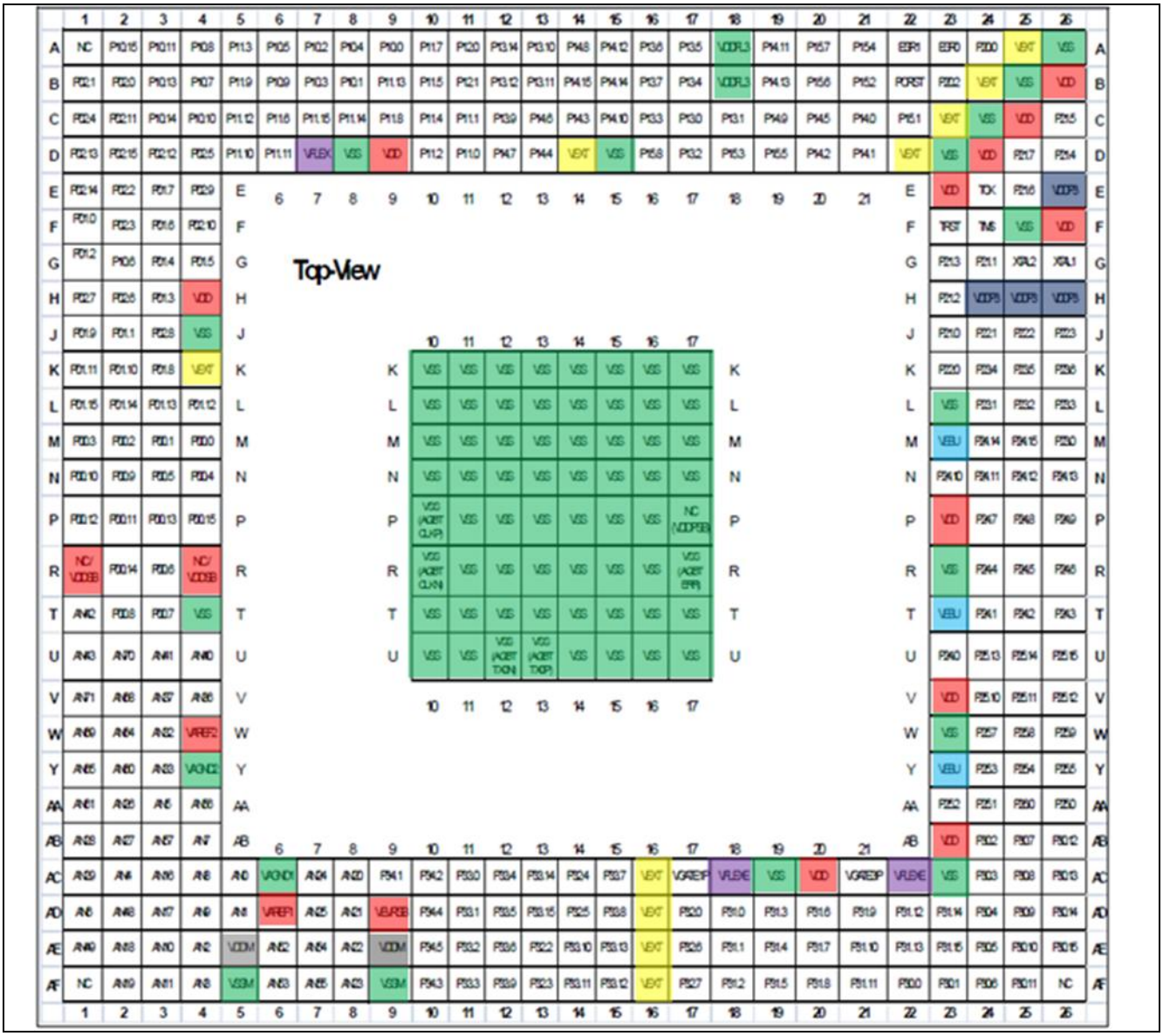


Figure 20 BGA-416

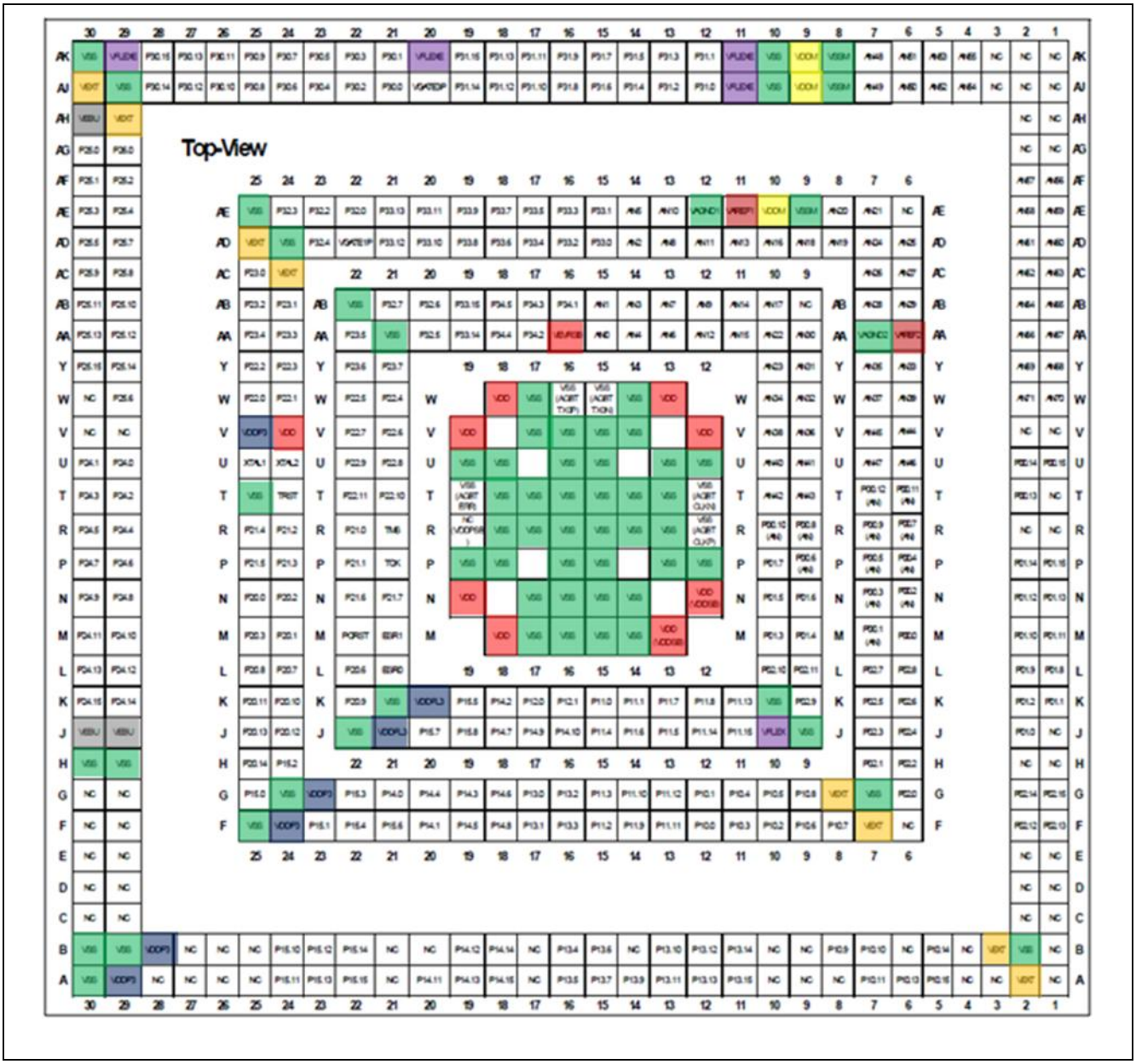


Figure 21 BGA-516

3.1 Example Layouts

Here we present some sample layout views for reference.

The sample layout designs were based on a stack-up given and the following design rules:

- Trace = 130µm, Via-drill/-pad 0.3/0.6mm
- 130µm clearance for signal-to-signal and signal-to-pad
- Top/Bottom Cu Thickness 50µm
- Inner layer Cu Thickness 30µm

3.1.1 Example Layout for LQFP-144 Package

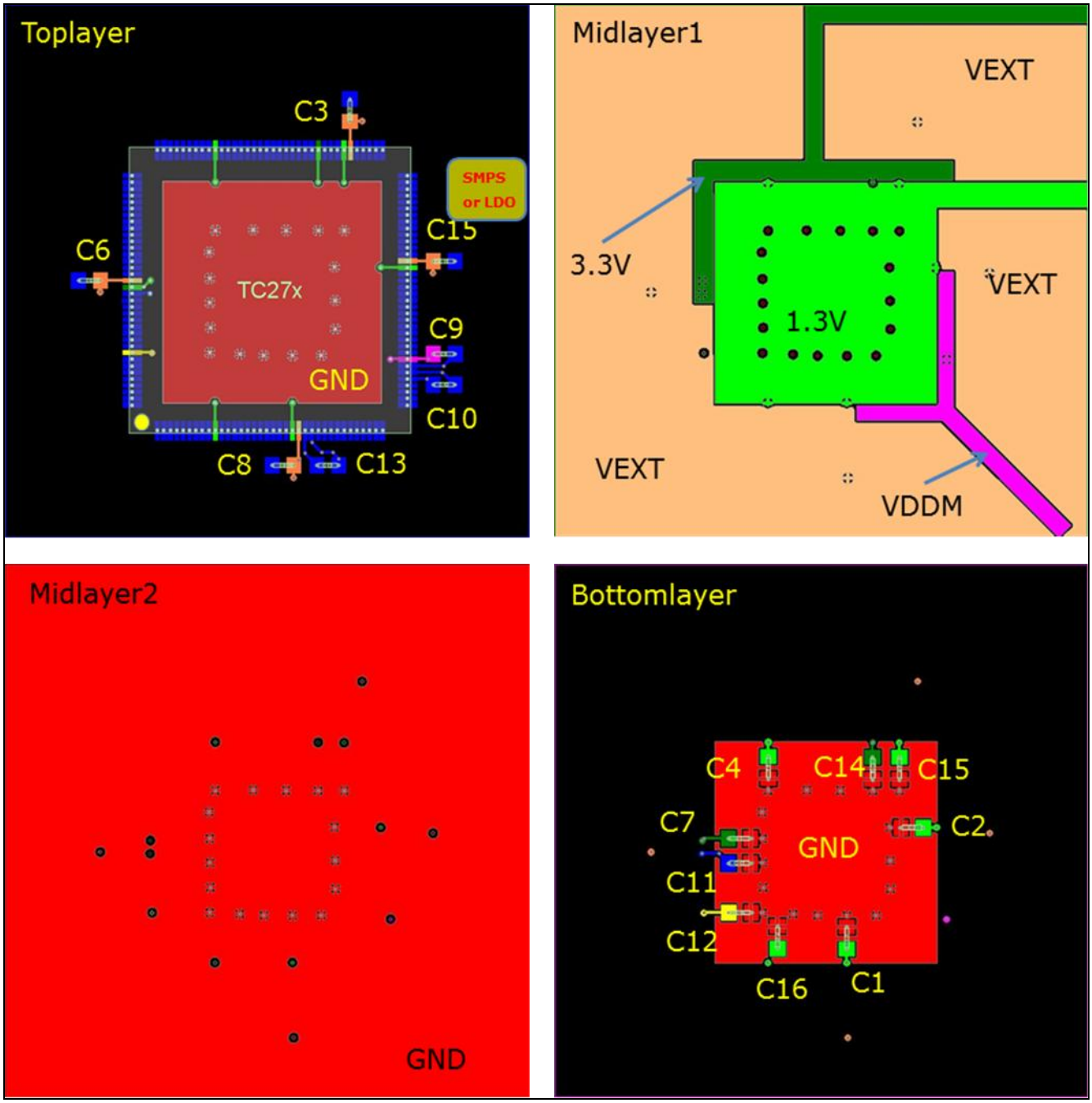


Figure 22 Example Layout for LQFP-144 Package

Table 2 Decoupling Capacitor List for LQFP-144 for External Supply Mode

Capacitor	Value	Supply	LQFP-144 Pin
C1,C2,C4,C5	4 x 100nF	VDD	22,58,99,79
C3,C6,C8,C15	4 x 100nF	VEXT	23,59,78,125
C7	1x 330nF-470nF in case of external supply or 1x 1µF-2µF in case of internal LDO EVR supply configuration	VDDP3	126
C14	1 x 330nF	VDDOSC3	83
C11	1 x 100nF	VDDFL3	127
C16	1 x 100nF	VDDSTBY	10
C9	1 x 100nF	VDDM / VSSM	44 / 43
C10	1 x 100nF	VAREF1 / VAGND1	42 / 41
C13	1 x 100nF	VAREF2 / VAGND2	24 / 25
C12	1 x 100nF	VFLEX	136

3.1.2 Example Layout for LQFP-176 Package

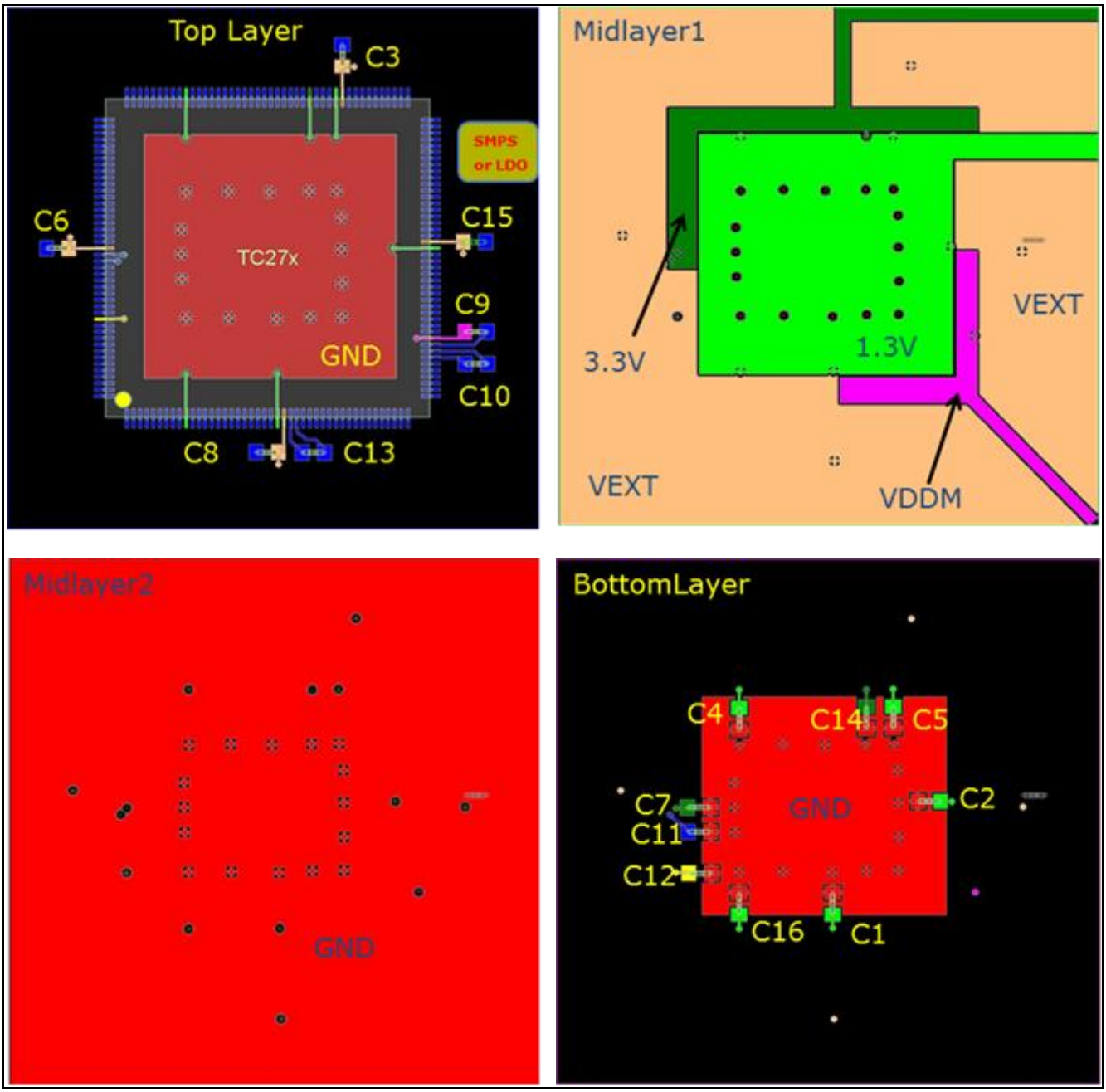


Figure 23 Example Layout for LQFP-176 Package

Table 3 Decoupling Capacitor List for LQFP-176 Package for External Supply Mode

Capacitor	Value	Supply	LQFP-176 Pin
C1,C2,C4,C5	4 x 100nF	VDD	24,68,123,100
C3,C6,C8,C15	4 x 100nF	VEXT	25,69,99,153
C7	1x 330nF-470nF in case of external supply or 1x 1µF-2µF in case of internal LDO EVR supply configuration	VDDP3	154
C14	1 x 330nF	VDDOSC3	104
C11	1 x 100nF	VDDFL3	155
C16	1 x 100nF	VDDSTBY	10
C9	1 x 100nF	VDDM / VSSM	54 / 53
C10	1 x 100nF	VAREF1 / VAGND1	52 / 51
C13	1 x 100nF	VAREF2 / VAGND2	26 / 27
C12	1 x 100nF	VFLEX	164

3.1.3 Example Layout for LFBGA-292 Package

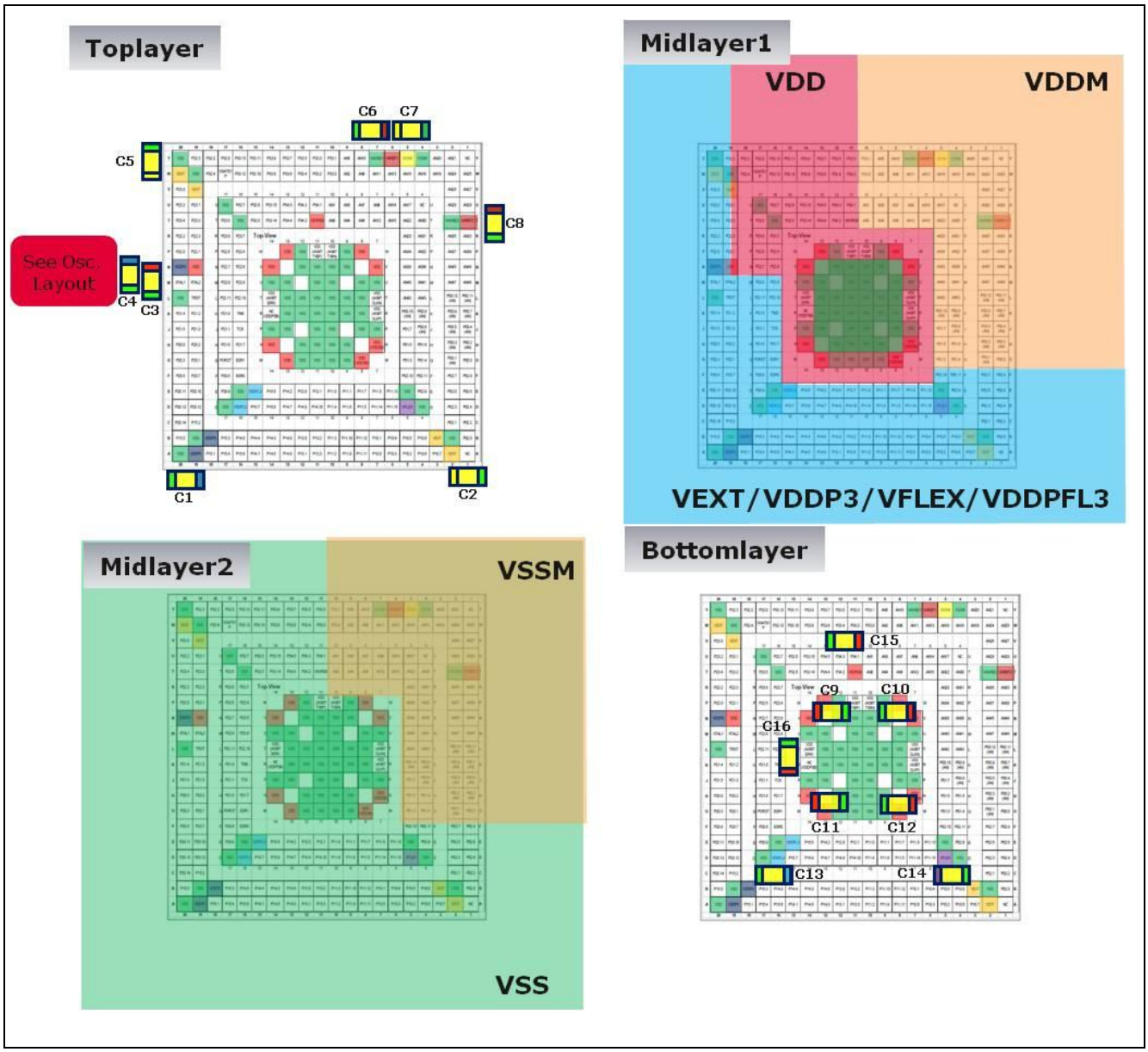


Figure 24 Example Layout for LFBGA-292 Package

Table 4 Decoupling Capacitor List for LFBGA-292 Package for External Supply Mode

Capacitor	Value	Supply	BGA-292 Pin
C9,C10,C11	3 x 100nF	VDD	P13//N14, P8//N7, H14//G13
C12	1 x 100nF	VDD/VDDSTBY (PD/ED)	H7//G8
C13	1 x 100nF	VDDFL3	D16//E15
C14	1 x 100nF	VFLEX	D5
C2, C5	2 x 100nF	VEXT	A2//B3, V19//W20
C1	1x 330nF-470nF in case of external supply or 1x 1µF-2µF in case of internal LDO EVR supply	VDDP3	A19//B18
C3	1 x 330nF	VDD (VDDOSC)	N19
C4	1 x 330nF	VDDP3 (VDDOSC3)	N20
C7	1 x 100nF	VDDM / VSSM	Y5
C6	1 x 100nF	VAREF1 / VAGND1	Y6
C8	1 x 100nF	VAREF2 / VAGND2	T1
C15	1x 100nF	VEVRSB	T11
C16	1 x 100nF	VDDPSB (only for ED)	K14

3.1.4 Example Layout for BGA-416 Package

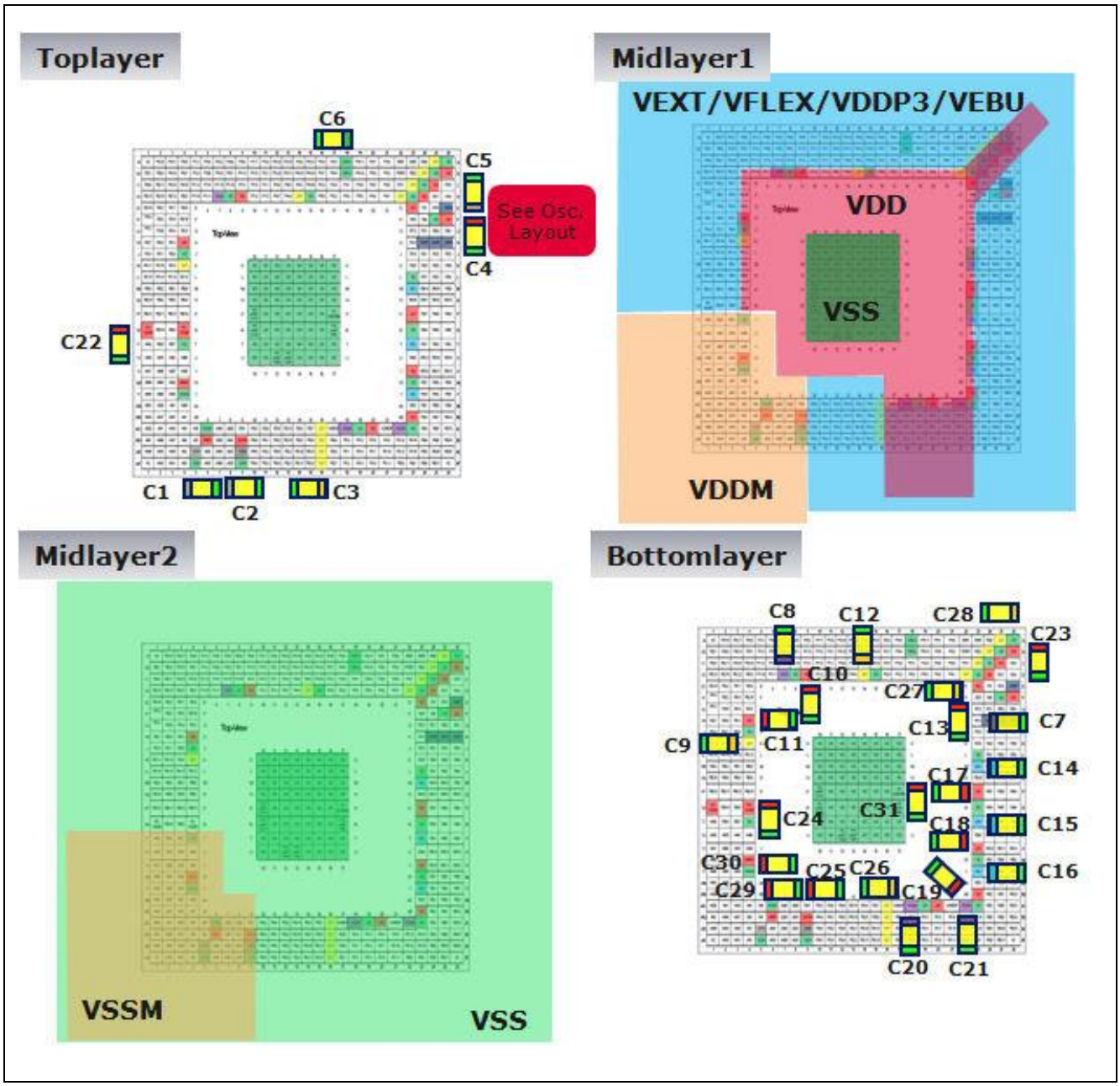


Figure 25 Example Layout for BGA-416 Package

Table 5 Decoupling Capacitor List for BGA-416 for External Supply Mode

Capacitor	Value	Supply	BGA-416 Pin
C17, C18, C19, C13, C23, C10, C11	7 x 100nF	VDD	P23, V23, AB23//AC20, E23//D24, C25//B26, D9, H4
C22, C24	2 x 100nF	VDDSTBY (only for ED)	R1, R4
C9, C12, C3, C26, C27, C28	6 x 100nF	VEXT	K4, D14, AC16//AD16, AE16//AF16, D22//C23, B24/A25
C7	1x 330nF-470nF in case of external supply or 1x 1µF-2µF in case of internal LDO EVR supply	VDDP3	H24//H25//H26
C14, C15, C16	3 x 100nF	VEBU	M23, T23, Y23
C20, C21	2 x 100nF	VFLEXE	AC18, AC22
C8	1 x 100nF	VFLEX	D7
C6	1 x 100nF	VDDFL3	A18//B18
C5	1 x 330nF	VDDP3	E26
C4	1 x 330nF	VDD	F26
C1, C2	2 x 100nF	VDDM	AE5, AE9
C25	1 x 100nF	VDDEVRSB	AD9
C29	1 x 100nF	VAREF1	AD6
C30	1 x 100nF	VAREF2	W4
C31	1 x 100nF	VDDPSB	P17

3.1.5 Example Layout for BGA-516 Package

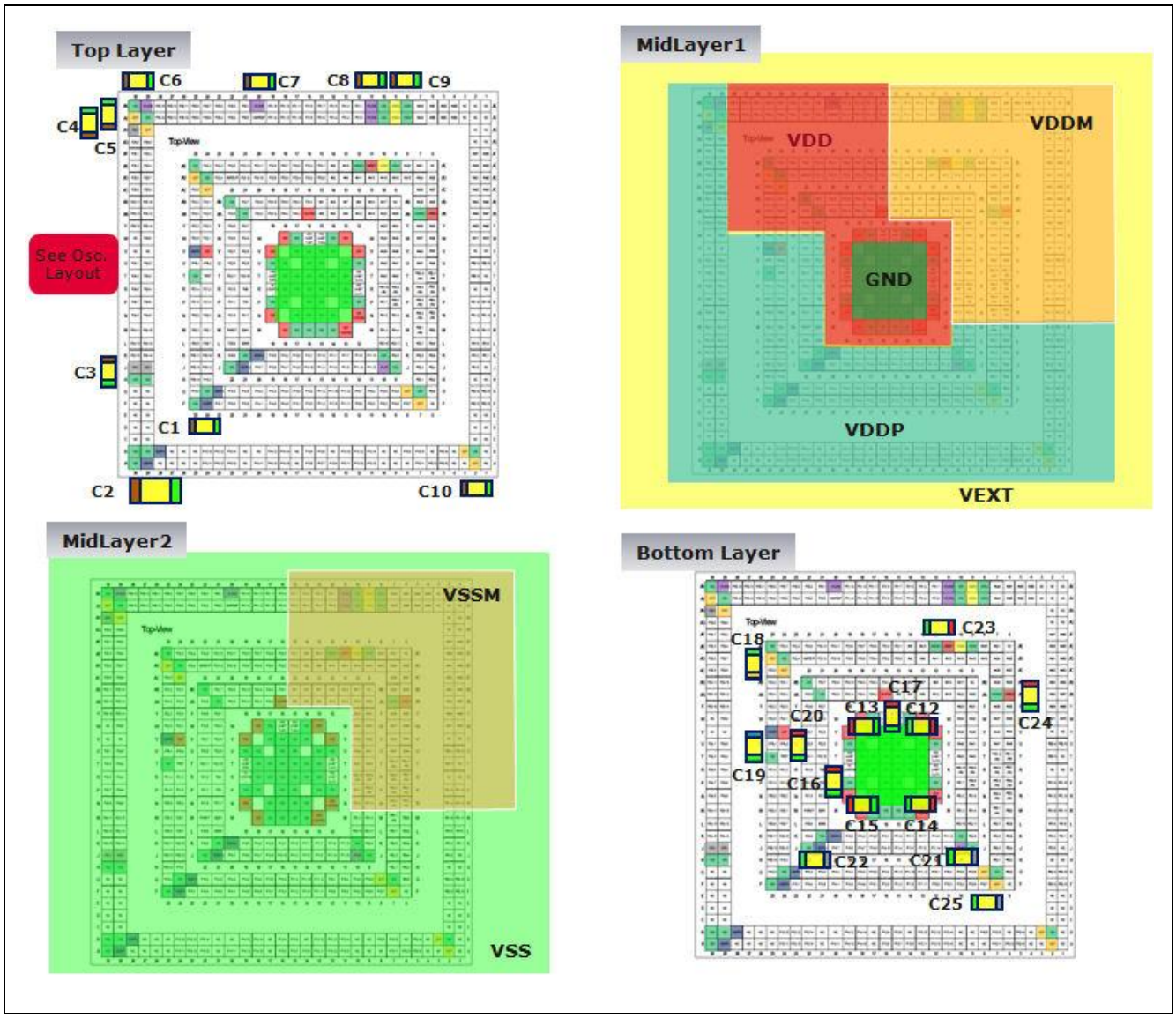


Figure 26 Example Layout for BGA-516 Package

Table 6 Decoupling Capacitor List for BGA-516 for External Supply Mode

Capacitor	Value	Supply	BGA-516 Pin
C12, C13, C15	3 x 100nF	VDD	V19//W18, V12//W13, M18//N19
C14	1 x 100nF	VDD/VDDSB (PD/ED)	M13//N12
C6, C7, C8	3 x 100nF	VFLEXE	AK29, AK20, AK11//AJ11
C21	1 x 100nF	VFLEX	J10
C5, C18, C10, C25	4 x 100nF	VEXT	AJ30//AH29, AD25//AC24, A2//B3, F7//G8
C4, C3	2 x 100nF	VEBU	AH30, J30//J29
C22	1 x 100nF	VDDFL3	J21//K20
C16	1 x 100nF	VDDPSB (only for ED)	R19
C1	1 x 100nF	VDDP3	F24//G23
C2	1 x 330nF-470nF in case of external supply or 1 x 1µF-2µF in case of internal LDO EVR supply	VDDP3	A29//B28
C23	1 x 100nF	VAREF0 / VAGND0	AE11
C24	1 x 100nF	VAREF2 / VAGND2	AA6
C9	1 x 100nF	VDDM	AK9//AJ9//AE10
C19	1 x 330nF	VDDP3	V25
C20	1 x 330nF	VDD	V24
C17	1 x 100nF	VEVRSB	AA16

3.2 Decoupling Capacitors for Different Supply Modes

Here we show a sample layout with SMPS/DC-DC regulator mode.

The component references are the same in the table with recommended component values for identification.

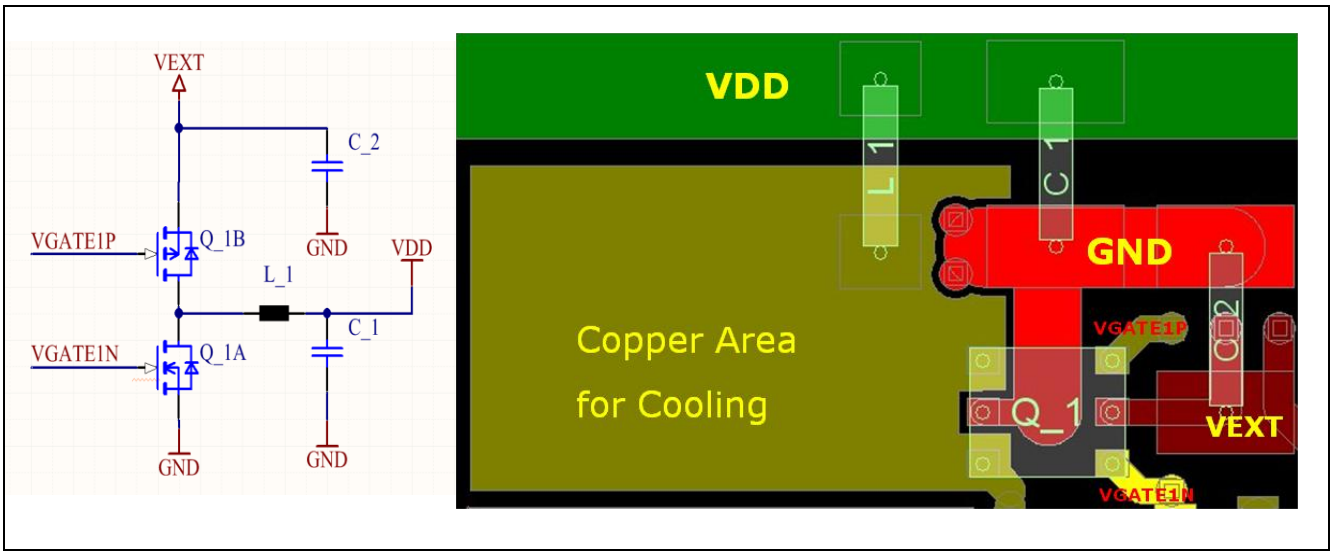


Figure 27 Example Layout of SMPS/DC-DC Regulator

Table 7 Decoupling Capacitors for different Supply Modes:

Number	Conditions/Usecase	MOSFETs (Package)	Inductors / Capacitors (Package) ➔ Component Reference
EVR13 SMPS/DC-DC Regulator			
1.	I_{DD} <400 mA f_{DC} = 1.5 MHz	Complementary MOSFET BSL215C (TSOP-6) => Q_1	1. Inductor LTF3020T-3R3N-H/D[1] **=> L_1** 2. Output Capacitor CGA6M3X7R1C106K (1210) **=> C_1** 3. Input Capacitor CGA5L1X7R1C685K (1206) **=> C_2**
2.	I_{DD} <400 mA f_{DC} = 1 MHz	Complementary MOSFET BSL215C (TSOP-6) => Q_1	1. Inductor LTF3020T-4R7N-H/D **=> L_1** 2. Output Capacitor CGA6M3X7R1C106K (1210) **=> C_1** 3. Input Capacitor CGA5L1X7R1C685K (1206) **=> C_2**
3.	I_{DD} <1 A f_{DC} = 1.5 MHz	Complementary MOSFET BSZ15DC02KD (S3O8) => Q_1	1. Inductor LTF5022T-3R3N2R5-H/D[1] **=> L_1** 2. Output Capacitor CGA6P1X7R1C226M (1210) **=> C_1** 3. Input Capacitor CGA6M3X7R1C106K (1210) **=> C_2**
4.	I_{DD} <1 A f_{DC} = 1 MHz	Complementary MOSFET BSZ15DC02KD (S3O8) => Q_1	1. Inductor LTF5022T-4R7N2R0-H/D **=> L_1** 2. Output Capacitor CGA6P1X7R1C226M (1210) **=> C_1**

			3. Input Capacitor CGA6M3X7R1C106K (1210) **=> C_2**
EVR13 LDO with an external P-Channel MOSFET as pass devices			
5.	I_{DD} < 300 mA	P-Channel MOSFET SPD04P10PL (TO-252)	Output Capacitor C3216X7R1C475K (1206)
EVRx3 LDO with internal pass devices – Buffer Capacitors			
6.	I_{DDX} < 100 mA	-	C3216X7R1C105K (1206) **=> C_2**
7.	I_{DDX} < 200 mA	-	C3216X7R1C225K (1206) **=> C_2**
8.	I_{DDX} < 300 mA	-	C3216X7R1C475K (1206) **=> C_2**

1) If I_{DD} current ripple needs to be further reduced, a higher inductance (LTFx02yT-4R7N-H/D) maybe required.

4 HSSI on AURIX products

For general information about microcontroller PCB design guidelines please refer to the Infineon document AP24026.

4.1 2.5 Gbit/s HSSI

2.5Gb/s HSSI is an LVDS interface with a maximum voltage drive level of ±400mV. The routing of the signals should be treated as critical and the designer should give maximum attention to the routing. The 50 Ohm trace impedance and the differential impedance of 100 Ohm are the most important requirements of this interface.

4.2 HSCT Interface

HSCT Interface is an LVDS interface with a maximum data rate of 320 Mb/s. It requires 50 Ohm trace and 100 Ohm differential impedance.

4.3 DAP Interface

For DAP interface signals, it is recommended to apply the serial termination method on both Ends for the DAP1 signal, since this is a bi-directional line (same for DAP2 if used).

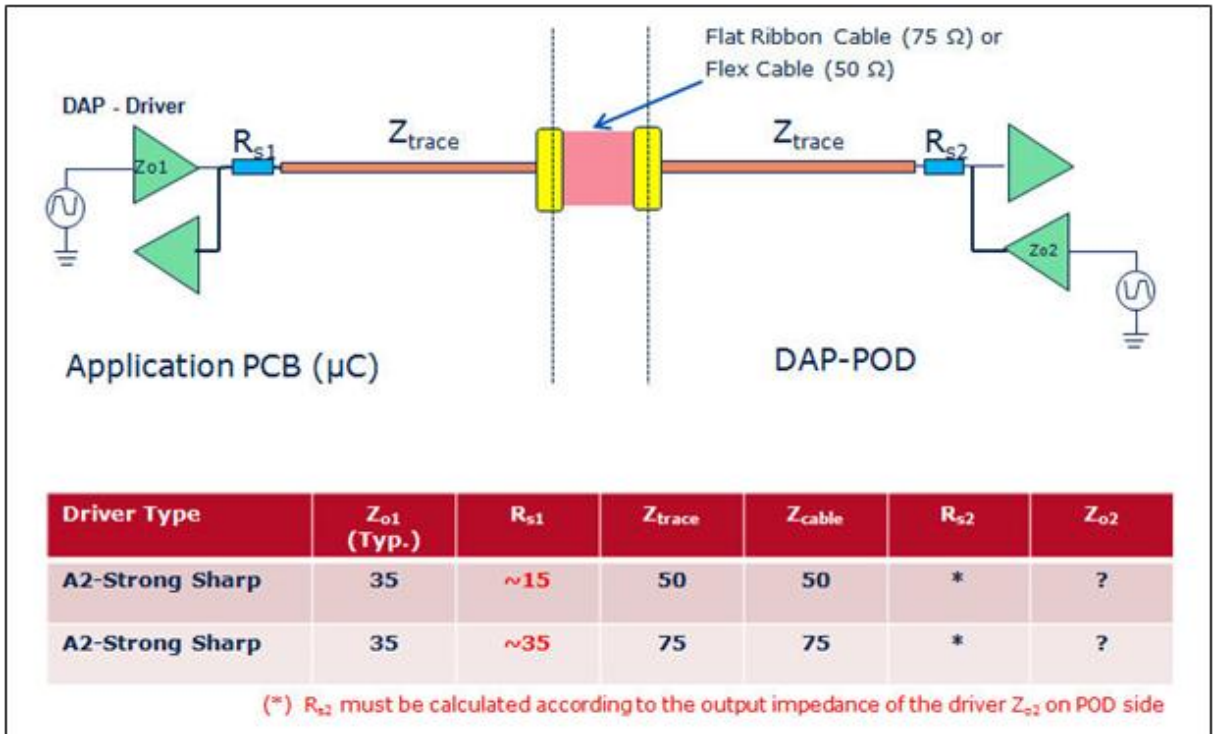
Keep the trace length of DAP1 and DAP2 equal.

The DAP0 signal can be terminated only at source (depending on the capability of the DAP0 driver). The terminations must accordingly match to the line impedance.

It is recommended to use a total trace length less than 10cm for this interface on the boards (load parasitic of the cable has also to be considered).

The following are important rules for single-ended signal design for the DAP interface:

- Do not use multiple signal layers to route the clock signal (DAP0).
- Use a reference layer below the signal lines and avoid reference changes.
- If possible, place the clock signal between two reference layers (GND // DAP0 // GND).
- Route first the clock line DAP0 and use a straight line for connection.
- Minimize the via count on signal lines (if possible, do not use any).
- Keep an appropriate distance between the single-ended lines.
- If daisy-chain routing is required, avoid stubs at connection points.
  - If stubs cannot be avoided, use optional placement resistors to de-couple the chain to get well defined line impedance.
- Design line impedance according to the selected operating driver strength of the DAP interface.
- Use a series termination method if necessary and calculate the value of series resistance depending on the selected driver strength.
  - For example: For the strongest driver setting (for A2 Type) the output impedance is typically 35R, so the series termination resistance value can be selected as 15R. For the case that a flat ribbon cable is used (75R), select 35R. For both cases the PCB trace impedances on both sides must be designed accordingly.



Driver Type	Z_{o1} (Typ.)	R_{s1}	Z_{trace}	Z_{cable}	R_{s2}	Z_{o2}
A2-Strong Sharp	35	~15	50	50	*	?
A2-Strong Sharp	35	~35	75	75	*	?

(*) R_{s2} must be calculated according to the output impedance of the driver Z_{o2} on POD side

Figure 28 Series Termination of DAP1 and DAP2 (recommendation for 160MHz)

Note: For the specification of the recommended cable assembly see Infineon Document "AP24003 - DAP Connector".

5 References

[1] Infineon Application Note, AP24026 - EMC Design Guidelines for Microcontroller Board Layout

[2] High Speed Digital Design, A Handbook of Black Magic, H.Johnson and M. Graham

[3] High-Speed Digital System Design, A Handbook of Interconnect Theory and Design Practices, S.H. Hall, G.W. Hall, J.A. McCall

[4] Xilinx, “Spartan-6 FPGA PCB Design and Pin Planning Guide”, UG393 (v1.2) July 15, 2010
http://www.xilinx.com/support/documentation/user_guides/ug393.pdf

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